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April 2016

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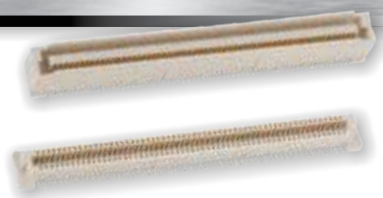

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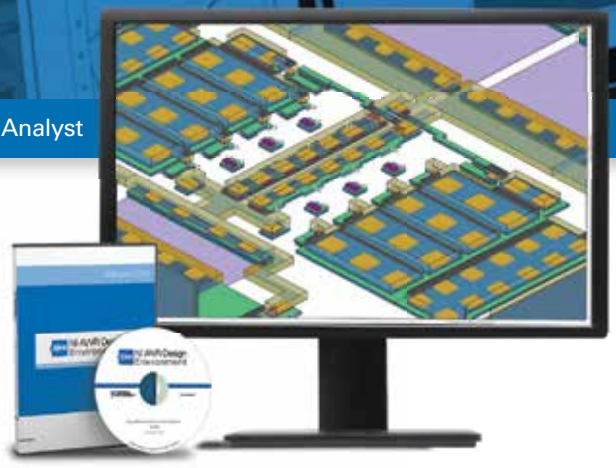

NATIONAL INSTRUMENTS™

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IDT's easy-to-use reference boards and comprehensive design support collateral eliminate traditional design and support barriers regardless of application volume.

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New-Tech Europe

Read To Lead

April 2016

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About New-Tech Magazines Group

'New-Tech Magazines' A world leader in publishing high-tech and electronics, producing top quality publications read by tens of thousands professionals from all over the world especially from Europe, innovative electronics, IoT, microwave, homeland security, aerospace, automotive and technological industries.

Our specialized target audiences prefer New-Tech Europe because they know that our publications are a reliable source of the latest information in their respective fields. Our multidimensional editorials, news items, interviews and feature articles provide them with a full, well-rounded picture of the markets in which they operate - an essential asset for every technological leader striving to stay ahead, make the right decisions, and generate the next global innovation.

Moreover, as an attractive platform for advertisers from around the world, New-Tech Europe has become a hub for bustling international commercial activity. Here, through ads and other promotional materials, Israeli readers obtain crucial information about developers and manufacturers worldwide, finding the tools, instruments, systems and components they need to facilitate their innovative endeavors.

Targeting the needs of both the global and european industries and global advertisers, New-Tech Magazines Group constantly expands and upgrades its services. Over the years, the company has been able to formulate a remarkably effective, multi-medium mix of offerings, combining magazine publications with useful online activities, newsletters and special events and exhibitions.

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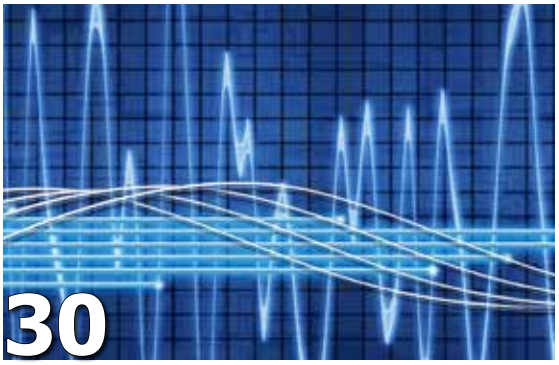

Latest News

Samsung Knox Now Leading the Next Evolution of the Enterprise

Samsung is expanding Knox as a suite of purpose-built business tools that go beyond mobile

Samsung Knox, the award winning, defense-grade security platform, is expanding to offer a suite of purpose-built, innovative and intuitive business tools designed for the ways people want to work. The new Samsung Knox is taking the platform beyond mobile to serve as the foundation for all Samsung enterprise solutions and services.

"As we move closer each day to a world where all things are connected, strength of security has never been more important," said DJ Koh, President of Mobile Communications Business, Samsung Electronics. "As a renowned mobile security platform with notable government certifications, placing Samsung Knox at the foundation of all solutions and services will deliver the infrastructure needed to advance Samsung's commitment to the enterprise."

Secure Compatibility with More Devices

An important step in the expansion of Samsung Knox is its security coverage for Samsung devices from flagship devices to many mid-tier devices including select smartphones and tablets. Additionally, Samsung Knox is available on wearable devices such as the Samsung Gear S2. This means many more Samsung device owners will be able to benefit with Samsung Knox's defense-grade protection.

Platform Expansion to Drive Interoperability

Samsung Knox is designed with multi-platform interoperability to work with existing IT assets. This commitment to interoperability will now be extended beyond the Android operating system to include Samsung's Tizen operating system. Samsung Knox also works seamlessly between Internet of Things solutions with a collection of open APIs and SDKs. In addition, Knox is supported by over 120 enterprise mobility management (EMM) providers worldwide, and performs with all popular single sign-on (SSO) and virtual private network (VPN) solutions to preserve enterprise legacy IT investments.

Beyond Security, Beyond Mobile

Since its launch in 2013, Samsung Knox has become a trusted and robust mobile security platform, protecting the device at every layer from hardware through software to application. With this next evolution, all Samsung enterprise solutions and services including healthcare, automotive, finance and other segments will be built on the Samsung Knox platform. "Samsung Knox allows us to offer our customers a better way to manage security and increase productivity," said Robert Schukai, Head of Applied Innovation, Thomson Reuters. "By partnering with Samsung, we can take advantage of a networked world by empowering people to see connections, use insights and make decisions when it counts. Samsung Knox is pushing forward our connected future."

GXV-T Revs up Research into Nimbler, Faster, Smarter Armored Ground Vehicles

Eight organizations get the greenlight to develop potentially groundbreaking technologies that would make future fighting vehicles more mobile, effective, safe and affordable

Today's ground-based armored fighting vehicles are better protected than ever, but face a constantly evolving threat: weapons increasingly effective at piercing armor. While adding more armor has provided incremental increases in protection, it has also hobbled vehicle speed and mobility and ballooned development and deployment costs. To help reverse this trend, DARPA's Ground X-Vehicle Technology (GXV-T) program recently awarded contracts to eight organizations.

DARPA has awarded contracts for the Ground X-Vehicle Technology (GXV-T) program to eight organizations. The program seeks to develop technologies that would make future armored fighting vehicles significantly more mobile, effective, safe and affordable. (DARPA)

"We're exploring a variety of potentially groundbreaking technologies, all of which are designed to improve vehicle mobility, vehicle survivability and crew safety and performance without piling on armor," said Maj. Christopher Orlowski, DARPA program manager. "DARPA's performers for GXV-T are helping defy the 'more armor equals better protection' axiom that has constrained armored ground vehicle design for the past 100 years, and are paving the way toward innovative, disruptive vehicles for the 21st Century and beyond."

Redefining Automated Test

with open software and modular hardware

How we interact with devices is changing. As the world becomes more software oriented, what we can accomplish increases exponentially. This shift should apply to our test equipment, too. Unlike traditional instruments with predefined functionality, the NI automated test platform provides the latest technologies to build complex systems while reducing development time and cost.

Through an intuitive graphical programming approach, NI LabVIEW reduces test development time and provides a single environment that simplifies hardware integration and reduces execution time.

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NATIONAL INSTRUMENTS

Latest News

DARPA has awarded contracts for GXV-T to the following organizations:

- Carnegie Mellon University (Pittsburgh, Pa.)
- Honeywell International Inc. (Phoenix, Ariz.)
- Leidos (San Diego, Calif.)
- Pratt & Miller (New Hudson, Mich.)
- QinetiQ Inc. (QinetiQ UK, Farnborough, United Kingdom)
- Raytheon BBN (Cambridge, Mass.)
- Southwest Research Institute (San Antonio, Tex.)
- SRI International (Menlo Park, Calif.)
- GXV-T is pursuing research in the following four technical areas:
- Radically Enhanced Mobility-Ability to traverse diverse off-road terrain, including slopes and various elevations. Capabilities of interest include revolutionary wheel/track and suspension technologies that would enable greater terrain access and faster travel both on - and off-road compared to existing ground vehicles.
- Survivability through Agility-Autonomously avoid incoming threats without harming occupants through technologies that enable, for example, agile motion and active repositioning of armor. Capabilities of interest include vertical and horizontal movement of armor to defeat incoming threats in real time.
- Crew Augmentation-Improved physical and electronically assisted situational awareness for crew and passengers; semi-autonomous driver assistance and automation of key crew functions similar to capabilities found in modern commercial airplane cockpits. Capabilities of interest include high-resolution, 360-degree visualization of data from multiple onboard sensors and technologies to support closed-cockpit vehicle operations.

Signature Management—Reduction of detectable signatures, including visible, infrared (IR), acoustic and electromagnetic (EM). Capabilities of interest include improved ways to avoid detection and engagement by adversaries.

The U.S. Army and U.S. Marine Corps have expressed interest in future GXV-T capabilities.

New Tools for Human-Machine Collaborative Design

Advanced materials are increasingly embodying counterintuitive properties, such as extreme strength and super lightness, while additive manufacturing and other new technologies are vastly improving the ability to fashion these novel materials into shapes that would previously have been extremely costly or even impossible to create. Generating new designs that fully exploit these properties, however, has proven extremely challenging. Conventional design technologies, representations, and algorithms are inherently constrained by outdated presumptions about material properties and manufacturing methods. As a result, today's design technologies are simply not able to bring to fruition the enormous level of physical detail and complexity made possible with cutting-edge manufacturing capabilities and materials.

To address this mismatch, DARPA today announced its TRAnsformative DESign (TRADES) program. TRADES is a fundamental research effort to develop new mathematics and algorithms that can more fully take advantage of the almost boundless design space that has been enabled by new materials and fabrication methods.

"The structural and functional complexities introduced by today's advanced materials and manufacturing methods have exceeded our capacity to simultaneously optimize all the variables involved," said Jan Vandenbrande, DARPA program manager. "We have reached the fundamental limits of what our computer-aided design tools and processes can handle, and need revolutionary new tools that can take requirements from a human designer and propose radically new concepts, shapes and structures that would likely never be conceived by even our best design programs today, much less by a human alone."

For example, designing a structure whose components vary significantly in their physical or functional properties, such as a phased array radar, and an aircraft skin, is extremely complicated using available tools. Usually the relevant components are designed separately and then they are joined. TRADES envisions coming up with more elegant and unified designs-in this case, perhaps embedding the radar directly into the vehicle skin itself-potentially reducing cost, size and weight of future military systems. Similarly, existing design tools cannot take full advantage of the unique properties and processing requirements of advanced materials, such as carbon fiber composites, which have their own shaping requirements. Not accounting for these requirements during design can lead to production difficulties and defects, and in extreme cases require manual hand layup. Such problems could be mitigated or even eliminated if designers had the tools to account for the characteristics and manufacturing and processing requirements of the advanced materials.

Ixia, Marvell and NXP Delivered the First Successful Multivendor Interoperability Demonstration of the AVnu AVB Automotive Profile

a leading provider of network testing, visibility, and security solutions, partnered with Marvell Technology Group, a global leader in providing complete silicon solutions, and NXP Semiconductors, the world leader in secure connectivity solutions for embedded applications, to deliver the first public interoperability demonstration of the AVnu Audio Video Bridging (AVB) profile dedicated for automotive usage at the Automotive Ethernet Congress held in Munich, Germany, February 3rd and 4th, 2016.

What is AVB/TSN?

Audio Video Bridging/Time Sensitive Networking (AVB/TSN) guarantees reliable transmission of audio, video, and control data over standard Ethernet. AVB/TSN assures not only a minimum bandwidth, but a maximum guaranteed latency, which is crucial for real-time media. The technology enables car makers to use the same Ethernet network for real-time and non-real-time communications, at much higher speeds than previous automotive busses. AVB/TSN allows for more advanced entertainment and Advanced Driver Assistance Systems (ADAS) features even on lower end car models.

What was demonstrated at the Automotive Ethernet Congress?

The demonstration showcased the automotive Ethernet specific physical layer, IEEE 100BASE-T1 (Ethernet running at 100Mbps over a single twisted pair), a milestone that reflects that automotive AVB/TSN is a technology that is ready for use in production. AVB/TSN allows time-sensitive application traffic to be carried over Ethernet reliably and is a common name for the set of technical standards developed by the Institute of Electrical and Electronics Engineers (IEEE) Audio Video Bridging Task Group of the IEEE 802.1 standards committee.

The demonstration included a complex scenario of real and emulated AVB talkers and listeners from NXP and Ixia communicating over a network of AVB bridges from Marvell and NXP. The term 'talker' denotes a stream source while 'listener' denotes a stream destination.

The benefits of the joint solution were observed on the real endpoints, as precisely measured by the Ixia AVB tester, and include:

Verification of synchronization and timely delivery of time-sensitive streams

Validation of bandwidth, QoS, priority remapping, and latency guarantees

Checking that both AVB and best effort traffic are handled appropriately at the same time through the AVB system

Validation of AVB Network boundaries in time-sensitive networks

Panasonic and Siemens to cooperate for next-generation electronic equipment assembly plants

•Signing of Memorandum of Understanding at the Hannover Messe

•Agreement on potential for the joint development of automation standards for the electronics industry

•Partners intend to cooperate in line integration and automation concepts

Panasonic and Siemens strive for the common advancement of digital production for the electronics industry. Against the backdrop of the Hannover Messe, Hiroyuki Aota, Director in charge of Factory Solutions Business and Executive Officer of Panasonic Corporation, and Anton S. Huber, CEO of the Digital Factory Division at Siemens AG, signed a Memorandum of Understanding setting out the intention of the two companies to work more closely together in the future in the fields of automation concepts for the electronics industry. The focus lies on standardized line integration concepts, which the partners plan to develop not only for individual production lines but also as overarching integration concepts for all process steps at the factory level, and as company-wide automation standards for globally distributed production networks.

Over recent years, Panasonic and Siemens have both worked independently on pioneering concepts linking digitalization and automation. In essence, the Smart Factory offering from Panasonic encompasses automatic assembly systems and the Manufacturing Execution System application PanaCIM. With the Digital Enterprise, Siemens is bringing to the table a portfolio encompassing the →

core elements of industrial software and automation, industrial communication, security and services. The contribution Siemens aims to make to the jointly developed concepts will be first and foremost its expertise in control and automation technology.

At the signing of the Memorandum of Understanding, Hiroyuki Aota said: "To significantly improve the productivity and quality of electronic equipment assembly, it is vital to connect all the equipment of any vendor in order to control the entire factory floor in real time. So concluding the memorandum for collaboration with Siemens, a company which has excellent technologies based on control devices and optimization software, will enable us to enhance our smart factory at the global level."

Anton S. Huber added: "Electronic production offers enormous potential for digitalization. The use of integrated automation solutions paves the way for substantial increases in both productivity and quality. Cooperation with Panasonic offers an exciting opportunity to selectively advance our Digital Enterprise portfolio for companies in the electronics industry."

Brian Krzanich: Our Strategy and The Future of Intel

Last week I shared how Intel is making broad changes to accelerate our transformation by aligning every segment of our business – our people, our places and our projects – to our strategy.

Brian Krzanich is the chief executive officer of Intel Corporation

Our strategy itself is about transforming Intel from a PC company to a company that powers the cloud and billions of smart, connected computing devices. We head into that future with tremendous assets and advantages: our spirit of innovation, our technology and manufacturing leadership, and the trust of our customers. But what does that future look like? I want to outline how I see the future unfolding and how Intel will continue to lead and win as we power the next generation of technologies.

There are five core beliefs that I hold to be undeniably true for the future.

The cloud is the most important trend shaping the future of the smart, connected world – and thus Intel's future.

The many "things" that make up the PC Client business and the Internet of Things are made much more valuable by their connection to the cloud.

Memory and programmable solutions such as FPGAs will deliver entirely new classes of products for the data center and the Internet of Things.

5G will become the key technology for access to the cloud and as we move toward an always-connected world.

Moore's Law will continue to progress and Intel will continue to lead in delivering its true economic impact.

Intel-virtuous-cycle

Our strategy is based on these premises, and the unique assets that only Intel brings to them. There is a clear virtuous cycle here – the cloud and data center, the Internet of Things, memory and FPGAs are all bound together by connectivity and enhanced by the economics of Moore's Law.

This virtuous cycle fuels our business, and we are aligning every segment of our business to it. Let me lay out how the parts of our strategy interact together and reinforce our growth.

Putting it all together, Intel is uniquely positioned to power the cloud and drive the increasingly smart, connected world. We see tremendous opportunity in the growth of this virtuous cycle - the cloud and data center, the Internet of Things, memory and FPGAs all bound together by connectivity and enhanced by the economics of Moore's Law - which will provide a strong and dynamic future for Intel.

We are in a time when technology is valued not just for the devices it produces, but for the experiences it makes possible. Intel will lead in this new era by remaining true to our history as inventors and makers, as a global leader in manufacturing, as world class innovators. We will also lead by becoming a company with a broader focus, and with sharper execution. In doing so, we will create lasting value for our customers, partners and shareholders, and achieve our mission to lead in a smart, connected world.

It is an incredibly exciting time for Intel as we accelerate our strategy, and our impact. The work we do at Intel today will change this company, our industry and the world.

Brian Krzanich is the chief executive officer of Intel Corporation.

Nokia plans to acquire Withings to accelerate entry into Digital Health

Nokia plans to acquire Withings to accelerate entry into Digital Health

Nokia has announced plans to acquire Withings S.A., a pioneer and leader in the connected health revolution with a family of award-winning digital health products and services to help people all over the world lead healthier, happier and more productive lives. Withings will be part of our Nokia Technologies business.

"We have said consistently that digital health was an area of strategic interest to Nokia, and we are now taking concrete action to tap the opportunity in this large and important market," said Rajeev Suri, president & CEO of Nokia. "With this acquisition, Nokia is strengthening its position in the Internet of Things in a way that leverages the power of our trusted brand, fits with our company purpose of expanding the human possibilities of the connected world, and puts us at the heart of a very large addressable market where we can make a meaningful difference in peoples' lives."

World Health Organization figures show cardiovascular disease as today's number one cause of death, with more than a billion adults around the world living with uncontrolled hypertension. Diabetes now affects more than one in twelve adults worldwide, a four-fold increase since 1980. Healthcare is expected to be one of the largest vertical markets in the Internet of Things, with analysts forecasting that mobile health, with a CAGR of 37%, will be the fastest growing health care segment from 2015-2020.

The combination of innovative products from Withings and the Digital Health business will also ensure the ongoing renewal of Nokia Technologies' world class IPR portfolio.

Withings was founded by Chairman Eric Carreel and CEO Cedric Hutchings in 2008 and is headquartered in France, with approximately 200 employees across its locations in Paris, France, Cambridge, US and Hong Kong. Withings' portfolio of regulated and unregulated products includes activity trackers, weighing scales, thermometers, blood pressure monitors, home and baby monitors and more, and is built on a sophisticated digital health platform, providing insights to empower people to make smarter decisions about the health and wellbeing of themselves and their families. Withings' own products are complemented by an ecosystem of more than a hundred compatible apps.

The Nokia brand continues to be recognized, valued and trusted by consumers, built on a heritage of beautifully designed, innovative and reliable technology in the service of people around the world to help real human needs.

VersaSense presents MicroPnP: the world's first plug-and-play Internet of Things platform based on SmartMesh IP from Linear Technology

VersaSense will present live demonstrations of its award-winning MicroPnP product range at Hannover Messe, Linear Technology Stand H23, Hall 9. MicroPnP is based on SmartMesh IP™embedded networking and uses Internet of Things (IoT) technologies to realize zero-configuration wireless sensing and actuation at a significantly lower price point than traditional wired solutions.

VersaSense ImageMicroPnP is a complete IoT hardware and software platform that dramatically reduces the total cost of ownership for sensing and control systems. MicroPnP provides a unique value proposition:

True plug-and-play identification of sensors and actuators at 10 million times lower power than USB.

Ultra-reliable networking through SmartMesh IP™ from Linear technology (>99.999% end-to-end reliability).

Industry-grade security from the embedded sensor to

the cloud.

A decade of battery lifetime, with accurate real time tracking of energy reserves across the entire network.

Flexible usage models: integrate MicroPnP in your network through 'sensing as a product', or consume data through 'sensing as a service'.

These features have been achieved through a decade of industrial and academic research. MicroPnP won third place in the 2015 IPSO challenge and was nominated for the 2016 IoT hardware awards.

UW undergraduate team wins $10,000 Lemelson-MIT Student Prize for gloves that translate sign language

Two University of Washington undergraduates have won a $10,000 Lemelson-MIT Student Prize for gloves that can translate sign language into text or speech.

The Lemelson-MIT Student Prize is a nationwide search for the most inventive undergraduate and graduate students. This year, UW sophomores Navid Azodi and Thomas Pryor - who are studying business administration and aeronautics and astronautics engineering, respectively - won the "Use It" undergraduate category that recognizes technology-based inventions to improve consumer devices.

Sign language translating gloves

Their invention, "SignAloud," is a pair of gloves that can recognize hand gestures that correspond to words and phrases in American Sign Language. Each glove contains sensors that record hand position and movement and send data wirelessly via Bluetooth to a central computer. The computer looks at the gesture data through various sequential statistical regressions, similar to a neural network. If the data match a gesture, then the associated word or phrase is spoken through a speaker.

They honed their prototype in the UW CoMotion MakerSpace - a campus space that offers communal tools and equipment and opportunities for students to tinker, create and innovate. For Azodi and Pryor, that meant finding a way to translate American Sign Language into a verbal form instantaneously and in an ergonomic fashion.

"Many of the sign language translation devices already out there are not practical for everyday use. Some use video input, while others have sensors that cover the user's entire arm or body," said Pryor, an undergraduate researcher in the Composite Structures Laboratory in the Department of Aeronautics & Astronautics and software lead for the Husky Robotics Team.

"Our gloves are lightweight, compact and worn on the hands, but ergonomic enough to use as an everyday accessory, similar to hearing aids or contact lenses," said Pryor.

The duo met in the dorms during their freshman year and discovered they both had a passion for invention and problem solving. Azodi has technical experience as a systems intern at NASA, a technology lead for UW Information Technology and a campus representative for Apple. His long history of volunteer work - which includes organizing dozens of blood drives and working with Seattle Union Gospel Mission, Northwest Harvest and Ethiopia Reads - gave motivation to build a device that would have real-world impact.

"Our purpose for developing these gloves was to provide an easy-to-use bridge between native speakers of American Sign Language and the rest of the world," Azodi said.

The team received support and mentoring from Mike Clarke, who manages the CoMotion MakerSpace and met the students after one asked for help with some soldering equipment that turned out to be broken.

Pryor and Azodi's first target audience is the deaf and hard-of-hearing community and those interested in learning and working with American Sign Language. But the gloves could also be commercialized for use in other fields, including medical technology to monitor stroke patients during rehabilitation, gesture control and enhanced dexterity in virtual reality.

Their "Use It" Student Prize is one of seven awarded by the Lemelson-MIT Program this year. Each winning team of undergraduates will receive $10,000, and each graduate student winner will receive $15,000. The winners of this year's competition were selected from a diverse and highly competitive applicant pool of students from 77 colleges and universities across the country.

"This year's Lemelson-MIT Student Prize winners have outstanding portfolios of inventive work," said Lemelson-MIT Program faculty director Michael Cima. "Their passion for solving problems through invention is matched by their commitment to mentoring the next generation of inventors."

SOLAR IMPULSE LANDS IN THE SILICON VALLEY COMPLETING THE CROSSING OF THE PACIFIC OCEAN WITH SEVERAL WORLD RECORDS

Solar Impulse 2 (Si2) – the first solar airplane capable of flying day and night without using a drop of fuel – left Hawaii on 21 April at 6:15 am local time (UTC-10) and landed at the Moffett Airfield on 23 April at 11:44 pm local time (UTC-7), completing the crossing of the Pacific Ocean with several world records.

By attempting the first solar flight around the world, pushing back the boundaries of the possible, and taking on a project deemed impossible by industry experts, Bertrand Piccard and André Borschberg want to support concrete actions for sustainability and show that the world can be run on clean technologies.

Solar Impulse 2 (Si2)

At the controls of Si2, Bertrand Piccard touched down at the Moffett Airfield, home to NASA's Ames Research Centre and to Google's Planetary Ventures, after a flight of three days and two nights and 2'810 miles (4'523 km) arriving from Hawaii and completing the crossing of the Pacific Ocean, while breaking several world records (pending FAI approval). Those include distance, speed, duration and altitude in the electric airplane category and altitude (gain of height) in the solar airplane category. The first part of the Pacific was accomplished by André Borschberg in a world record flight of five days and five nights from Japan to Hawaii last July.

A tandem achievement without a single drop of fuel. Bertrand Piccard initiated Solar Impulse to attractively promote a pioneering and innovative spirit, particularly in the fields of renewable energy and clean technologies.

On 22 April, on the occasion of Earth Day and the second consecutive day flying over the Pacific Ocean, Piccard spoke with UN Secretary-General Ban Ki-moon and 175 heads of states, directly from the cockpit of Si2, during a video conference with the United Nations in New York for the signature of the Paris Agreement on Climate Change: a symbolic milestone for the solar airplane in the air, the launch of a clean revolution on the ground, and a strong message sent to the world. The flight from Hawaii to California was the ninth leg of the Round-The-World Solar Flight that will continue onward to New York, Europe or North Africa and Abu Dhabi in the United Arab Emirates where the adventure started in March 2015. By flying around the world with Si2, propelled solely by the energy of the sun, Bertrand Piccard and André Borschberg are making history with clean technologies. Their adventure proves that change is possible and that there is reason to hope for a sustainable world. Solar Impulse's energy efficient solutions can already be used, not only in the air, but also on the ground, and have the potential to change lives, societies and future markets in an unprecedented way.

Siemens and Valeo join forces for global leadership in powertrains for electric cars

Form a 50:50 joint venture in high-voltage powertrains for electric cars

Strong partners with complementary scope and portfolio

New joint venture becomes strong player in the fast growing market of automotive electrification

Focus to provide innovative and affordable high-voltage components and systems for electric cars in global mass markets

Siemens and Valeo have signed an agreement to form a joint venture in high voltage powertrains. With this move the companies create a global leader of innovative and affordable high-voltage components and systems for the entire range of electric vehicles including hybrids, plug-in hybrids and full electric vehicles. Building upon their complementary scope and portfolio, the joint venture will provide substantial synergies in manufacturing and sourcing and create a base for sustained growth and profitability. The electric vehicle components market is expected to grow with a compound annual growth rate of more than 20% until 2020. According to the agreement, Siemens and Valeo will each hold a 50% stake in the joint venture, have joint control and account for their respective stake using the equity method.

"We are delighted at the perspective of combining our strengths with Siemens in electrified powertrain systems," said Jacques Aschenbroich, Chairman and Chief Executive Officer of Valeo. Valeo will be contributing its high-voltage power electronics

business, including 200 employees of which 90 are based in France, and which is part of the Powertrain Systems Business Group (PTS), Siemens will be contributing its E-Car Powertrain Systems Business Unit, employing around 500 people of which 370 are based in Germany and 130 in China.

The joint venture will have full business responsibility for the development, the sales and the production of high-voltage electric motors and power electronics products above 60V, required for electrified passenger cars and light commercial vehicles. The joint-venture will be able to provide an extended range of products from hybrid drive-train modules and solutions, including electric motors, range-extenders, DC/DC converters, inverters and chargers, to a fully electrified powertrain.

Siemens and Valeo strongly complement one another with regard to their product portfolios, production know-how and geographical spread. As a leading automotive player with strong market intimacy, Valeo has a strong industrial expertise, providing a worldwide customer base in powertrains with competitive and advanced high-voltage electronics produced by automotive certified production lines. Siemens' e car unit leverages the Group's system design competences in electric drivetrains, its strong engineering and validation base with an excellent experience in traction motor products.

The company's structures will be lean and adapted to global market requirements and the international competitive environment. Its headquarters will be located in Erlangen, Germany.

The joint-venture will have a global focus and cost-efficient regional set-up, providing access to key markets for automotive electrification, such as Europe and China: headquartered in Germany, with facilities in France, Norway, Poland, Hungary and China.

The joint-venture will offer its 700 employees the opportunity to participate in the uptake of a global leader. Merging activities of two employers of choice, the joint-venture will become a solid, committed and reputable employer. As a high-tech automotive company, it will offer its employees attractive international careers, in the fields of electrification and digitalization.

The project is subject to consultation of the employee representatives. Subject to approval of the relevant authorities, the joint venture is expected to start operations in the last quarter of calendar year 2016.

TactoTek reveals mass producible injection molded structural electronics innovations

TactoTek, a spin-off company from VTT Technical Research Centre of Finland, is a leading manufacturer of 3D injection molded structural electronics (IMSE) solutions. It will present production innovations that deliver mass production scalability at the IDTechEx Printed Electronics Europe conference in Berlin, Germany on 27-28 April.

TactoTek combines flexible printed circuitry and discrete electronic components to build fully integrated 3D injection molded 'smart surfaces.' The TactoTek solution can be applied to diverse markets and use cases, from automotive to household appliances and wearable technology.

According to TactoTek CTO and co-Founder, Antti Keränen, materials innovations in the injection molded electronics ecosystem, including advances in conductive inks and in-mold labeling films, have expanded use cases and improved yield for 3D injection molded structural electronics (IMSE) solutions. Meanwhile, TactoTek "has developed unique combinations of design methods, materials and manufacturing processes that enable mass manufacturing economies using industry standard equipment, some of which are referenced in TactoTek patent filings."

TactoTek innovations enable key processes, such as electronic component surface mounting, to be done in two dimensions using standard SMT equipment and electronic components—one key to cost effective mass production.

DuPont, the leading supplier of conductive inks, will also present its conductive ink capabilities and performance at Printed Electronics Europe.

TactoTek's solutions can integrate printed circuitry, printed touch controls and discrete electronic components, such as LEDs and ICs, into light, 3D injection molded plastics as thin as 2mm. By incorporating circuitry and electronics directly into plastic structures, TactoTek enables brands to design innovative form factors and consolidate electronics into a single 3D structure while minimizing electrical and mechanical assembly inherent to traditional electronics designs.

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The 3 Pain Points of the Mil/Aero Test Engineer

by Reggie Rector, NI

We all have our pains and struggles within our team or organization - whether it's the junior engineer that couldn't possibly be wrong about anything - ever, the dreaded consensus building meetings that do anything but, or a nearly impossible deadline (maybe for an article?) – we all have them.

The life of the aerospace test engineer is no different. They may be supporting depot-level test systems with 30-year old technology or racing to be first to market with the latest and greatest radar technology, but inevitably they have their share of challenges to tackle.

While unloading all our pains and struggles may be therapeutically beneficial, this article will focus on overcoming the challenges of the aerospace test engineer that have the biggest impact on the organization's success and, in concert, their own career growth.

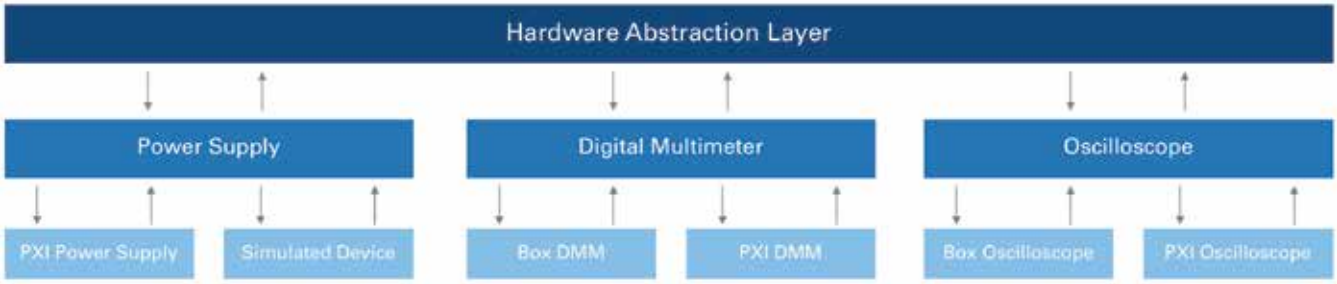
Legacy Test Program Set Support

The first, and most obvious, challenge the average test engineer faces is the need to support legacy Test Program Sets (TPSs). Commercial and military aerospace programs are extending well beyond their intended lifecycles, and support teams must carry these fleets forward into the next wave of technology lifecycles. When looking to upgrade a test system (or subsystem) for one of these programs, test engineers cannot only consider the technology insertion, they must also consider the hundreds or thousands of TPSs that have been developed for the system and the ripple effect that technology insertion will inevitably have on the program as a whole.

The most motivating and technologically savvy approach is for the test engineer to develop a completely new test system with exciting new instruments, instrumentation test adapters (ITAs), and fixtures while rehosting as many legacy TPSs as possible. Unfortunately, these test engineers ultimately have to answer to a budget and usually end up refurbishing existing test systems to replace the obsolete pieces through planned maintenance.

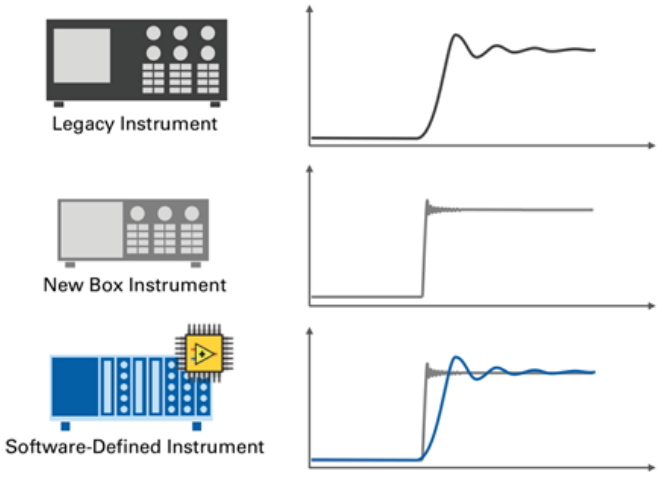
Let's take the example of refurbishing an existing system by replacing an obsolete oscilloscope with the objective of minimizing TPS migration costs. Sounds simple, right? On the surface, the test engineer's job sounds relatively straightforward – find an oscilloscope that can perform as well as, if not better than, the existing scope in the system. After all, most scopes in 2015 are going to pale in comparison to the dinosaurs that were designed into the system 10, 15, or 20 years ago.

The first bump in the road is form-factor. The new instrument needs to take up the same or less space in the 19 inch rack so as not to warrant a reconfiguration of the rack layout. Because there is a significant amount of system-level documentation, changing the layout of the rack



Hardware Abstraction Layers (HALs) significantly mitigate the impact of hardware obsolescence, but are difficult to justify in the absence of a long-term support strategy.

While difficult to accomplish, emulating legacy instrument capabilities greatly reduces the risk of TPS migration issues. Software-Designed, or Synthetic Instruments, offer a unique approach to test equipment emulation



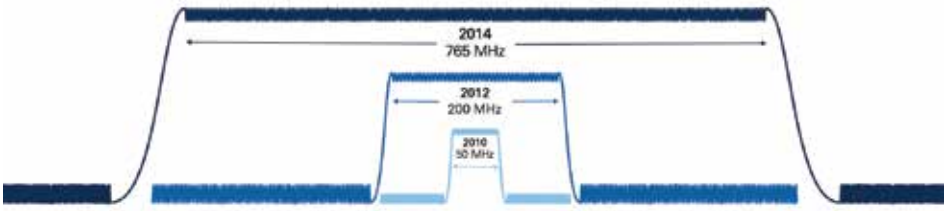
will introduce a massive amount of documentation changes (not to mention any possible signal integrity issues with changing cable lengths to the mass interconnect). This form-factor challenge is one of the many reasons that modular platforms like PXI (and formerly VXI) have dominated the Aerospace/Defense ATE market for the last 30 years. By following the strict guidelines of the PXI specification, a scope from vendor A will be the same size and utilize the same backplane power as vendor B, giving test engineers an easier upgrade path for their systems.

The second hurdle in the road is hardware abstraction layer (HAL) integration. Any test system that is expected to last for five to 10+years will inevitably have planned maintenance and operational costs. These are significantly reduced by abstracting vendor-specific hardware and drivers into a HAL or measurement abstraction layer (MAL). The test engineer is also tasked with evaluating the driver stack of the new instruments to ensure they plug into the HAL to mitigate the risk when migrating the thousands of TPSs still to come. Many HALs utilize the IVI driver class where possible and supplement with Plug-and-Play drivers. Since this example is an oscilloscope, we'll make a blanket claim that the test engineer has it "easy" and gets a pass on software because there is an existing IVI class specified for oscilloscopes.

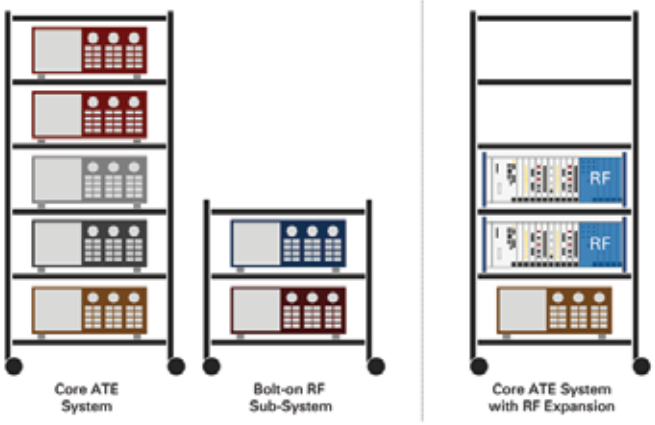
Hardware Abstraction Layers (HALs) significantly mitigate the impact of hardware obsolescence, but are difficult to justify in the absence of a long-term support strategy.

A third and often hidden hurdle is the answer to the question: is better really better?The specifications of this new oscilloscope are multiple generations of technology ahead of the obsolete equipment, so where's the issue? The issue comes when, for example, you insert this new oscilloscope into the system and the rise time or settling time measurements change significantly because you're sampling at three, five, or 10times the rate of the previous instrument, which results in dozens of incompatible TPSs that previously provided great system utilization. Another issue arises when legacy TPSs require trigger functionality that instrument vendors made obsolete years or decades prior. In this situation, the test engineer is challenged with looking across the entire database to identify which TPSs will be broken by inserting a new instrument that does not support the legacy trigger functionality - a database which often doesn't exist and requires weeks or months of manual effort to identify.

In order to minimize the unknown risks of TPS rehosting, many test engineers are taking advantage of software-designed instruments (SDIs) to give more flexibility in the rehosting process. Software-designed (also known as synthetic) instruments combine core analog and digital front-end technology with powerful, user-programmable FGPAs to provide the most flexible instruments on the



The evolution of NI vector signal analyzer bandwidth is one example of how aerospace ATE systems can scale to support the latest radar, communications, and signal intelligence systems.



Traditional ATE systems commonly used the "bolt-on" RF sub-system strategy due to the cost of RF equipment. As RF technology becomes more prevalent in LRUs and RF test equipment costs come down, we'll see RF test equipment become integrated into the core system.

market. If we apply the SDI approach to the oscilloscope challenges above, the test engineer (or TPS developer) can easily implement custom trigger functionality on the FPGA of the SDI to emulate legacy trigger technology. Some go further and use digital signal processing to emulate the analog performance of the legacy instrument's analog-to-digital converter technology.

While difficult to accomplish, emulating legacy instrument capabilities greatly reduces the risk of TPS migration issues. Software-Designed, or Synthetic Instruments, offer a unique approach to test equipment emulation.

Rapid RF Evolution

On the other side of the spectrum (literally and figuratively) is the challenge of keeping pace with the rapid evolution of RF technologies engineered into radars, signal intelligence systems, communications equipment, and other line-replaceable units (LRUs). This rapid pace of innovation keeps test engineers on their toes in terms of building scalable architectures that can not only test the technologies of today, but scale to support the next "wave" of RF capabilities.

The evolution of NI vector signal analyzer bandwidth is one example of how aerospace ATE systems can scale to support the latest radar, communications, and signal intelligence systems.

Historically, most high-mix test systems in aerospace/defense haven't included RF ATE subsystems as part of the core configuration due to the cost/benefit analysis of adding high-performance (high-price) RF test equipment to cover a small set of LRUs. The asset utilization simply couldn't justify the expense. As the number of RF-capable LRUs increases and RF instrumentation becomes more cost effective, it's becoming more common for RF equipment to be part of core high-mix test system configurations.

Traditional ATE systems commonly used the "bolt-on" RF sub-system strategy due to the cost of RF equipment. As RF technology becomes more prevalent in LRUs and RF test equipment costs come down, we'll see RF test equipment become integrated into the core system.

To illustrate the complexity facing the test engineer, let's use an example of a test system for a direction-finding, multi-antenna radar subsystem. In the manufacturing environment, it's reasonable to assume that each antenna will be tested serially using a high-performance signal source and a wide-band vector signal analyzer, along with some high-speed serial communication for controlling the UUT. Saying this is easy would be a massive overgeneralization, but when you compare this to the capabilities of the maintenance test system, it sounds like a walk in the park. So whose job is it to develop that complex test system for planned maintenance and field defective units? That's right, the test engineer.

When performing maintenance tests or analyzing a returned unit from the

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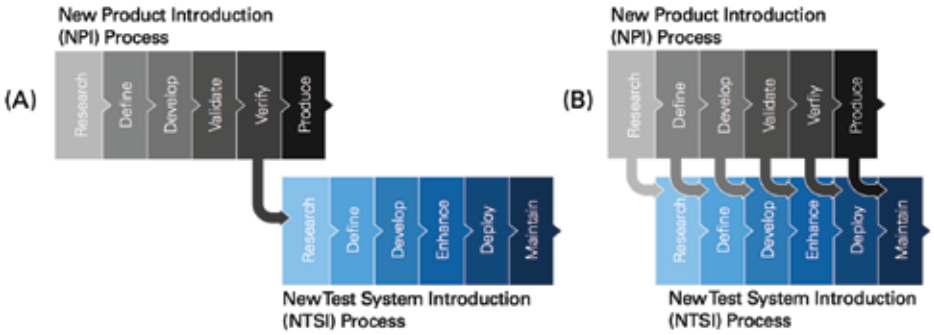
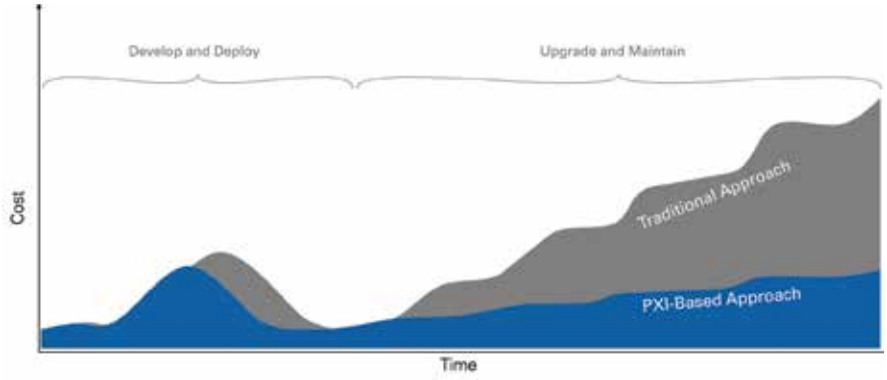


There are inefficient and costly flaws with the traditional approach of engaging test engineering late in the NPI process. Engaging earlier in the design cycle can lead to faster time-to-market, lower manufacturing cost, and improved yield.



Many organizations have different business units for the develop/deploy and support/maintain costs of a test system. Test engineers can greatly impact the operational costs of supporting a system, but must expand their influence beyond their own organization to understand and implement solutions to mitigate the long-term costs of supporting an ATE system.

field, your test cases are far more inclusive than the "did we build it right" manufacturing test case. You will need to emulate the real-world environment with highly synchronized signal sources including closed-loop control between the sources and analyzers to stress the DSP engine and measure the phase-coherency of the system. To address the synchronization and data transfer challenges, test engineers need to look beyond traditional boxed instrumentation to a platform-based approach such as PXI. To emulate the real-world environment with closed-loop control, engineers need flexible RF instrumentation architecture that combines data streaming architectures, FPGA-based signal processing, and high-performance, high-instantaneous bandwidth RF front-end technology to capture and process the incoming pulses.

It's also no secret that operational costs are high when sending units back to the intermediate- (I-) or depot- (D-) Level centers for maintenance or repair. As RF test equipment becomes easier to adopt in field test, these operational costs greatly improve. Not only does the organization benefit from the decrease in operational cost, but they can get better IP leverage between the depot and field testers for in-situ troubleshooting and diagnostics.

As you can imagine, the RF challenges of scalability, synchronization, and latency create complex system-level test architectures for the test engineer and are quite different than replacing the legacy oscilloscope and mitigating TPS rehosting costs, though both technology elements are great opportunities for the test engineer to provide significant value to the organization.

Increasing Sphere-of-Influence to Reduce the Cost of Test

A third, and maybe more subtle, pain point for test engineers is justifying short-term spend to mitigate long-term operational costs. Market pressures are as high as they have ever been, so test engineers are opting for point-solutions that neither provide the scalability for evolving technology demands nor have an architecture that simplifies maintenance for future upgradeability.

Furthering this problem is the fact that this short-term spend may not actually come directly from the test engineering budget. Looking upstream, we all know how difficult it can be to get a design engineer to modify a design once it meets the design specifications, but organizations can see significant improvements to their bottom line by engaging the test engineering group early as part of a Design For Test (DFT) or Design for Manufacturability (DFM) strategy. When yields improve and asset utilization increases, these optimizations typically go directly to the gross margin of the product.

Beyond DFM, it's also critical that the test engineers be involved early in the new product introduction (NPI) process. By actively engaging in every stage-gate of NPI, the test engineer can be developing product-

specific test code along the way and collaborating with validation engineers on automated code modules to simplify the validation and ease the transition into production. This is actually a process that NI went through in the early 2000's as we released 200+ products a year with increased complexity per generation. By bringing test engineering to the conversation early, we saw over 40% reductions in release to manufacturing (RTM) time, which directly shortened our time-to-market.

There are inefficient and costly flaws with the traditional approach of engaging test engineering late in the NPI process. Engaging earlier in the design cycle can lead to faster time-to-market, lower manufacturing cost, and improved yield.

If we look downstream, the test engineering budgets and the operations budgets are often decoupled, so the test engineering organization is not inherently incentivized to architect the system in a way that minimizes long-term operational costs. This is where siloed organizations struggle and strong communicators differentiate. At the heart of these negotiations and tradeoffs is the inherent knowledge of the test engineer about the suite of UUTs supported, the stability of the test system, and the areas to optimize or improve. While it can be painful for the test engineer, expanding their sphere-of-influence to the entire design-cycle makes them a truly valuable asset to the organization.

Many organizations have different business units for the develop/deploy and support/maintain costs of a test system. Test engineers can greatly impact the operational costs of supporting a system, but must expand their influence beyond their own organization to understand and implement solutions to mitigate the long-term costs of supporting an ATE system.

While the challenges of obsolescence management, rapidly evolving RF requirements, and influencing DFM are by no means all-encompassing, these challenges represent tremendous opportunity for the test engineer to impact the bottom line of the organization and showcase the value the test engineering team can deliver.

Reggie Rector is a Senior Product Manager for PXI and ATE Systems at NI with a special focus on Aerospace ATE. His job functions include product management and lifecycle planning, inbound product definition, and market development for PXI-based ATE systems. He holds a bachelor of science in Biological Systems Engineering from the University of Nebraska-Lincoln.

Sub-Threshold Design - A Revolutionary Approach to Eliminating Power

Ambiq Micro

Low energy consumption has replaced performance as the foremost challenge in electronic design. Performance is important, but it must now accede to the energy capacity of batteries and even the minimal output of energy harvesters. Performance at all costs no longer works; energy consumption is now the dominant requirement. While reducing energy consumption is critically important throughout the electronics industry, the question is: how should that goal be achieved? Ambiq Micro's approach moves beyond the incremental improvements that other semiconductor companies have taken and makes revolutionary advances through a unique approach to the problem: sub-threshold circuit design.

Energy is consumed in two fundamental ways: as leakage, when a circuit's state isn't changing, and dynamically as internal nodes are charged up and down. For realistic circuits in operation, dynamic power dominates – especially for the higher power supply voltages used in most designs today (see Figure 1 below). Because dynamic energy varies as the square of the operating voltage, that voltage becomes the biggest lever for reducing dynamic energy consumption (while also having a tangible, but less dramatic, impact on leakage). For example, when compared to a typical circuit operating at 1.8V, a "near-threshold"

Energy Per Operation (J)

circuit operating at 0.5V can achieve up to a 13X improvement in dynamic energy. An even more aggressive "sub-threshold" circuit operating at 0.3V can achieve up to a 36X improvement!

Traditional digital designs use the transistor state – "on" or "off" – as a critical concept for implementing logic. Analog designs likewise assume that a transistor is "on" to some controlled degree, using it for amplification. But sub-threshold operation means that none of the voltages in the chip rise above the threshold voltage (Vth), so the transistors never turn on. Even a logic "high" voltage keeps the transistors "off." This means that completely new design approaches are required.

This whitepaper examines the challenges of sub-threshold design, looking in particular at what's required to overcome the differences from traditional super-threshold design. These considerations drove the development and commercialization of Ambiq's patented Sub-threshold Power Optimized Technology (SPOTTM) platform, which Ambiq uses to build reliable, robust circuits that consume dramatically less energy on a cost-effective, mainstream manufacturing process.

Sub-threshold was proven decades ago

Sub-threshold design isn't a new concept. As far back as the 1970s, Swiss watchmakers noticed the potential of operating select transistors in the sub-threshold regime. The idea was picked up for pacemakers and RFID

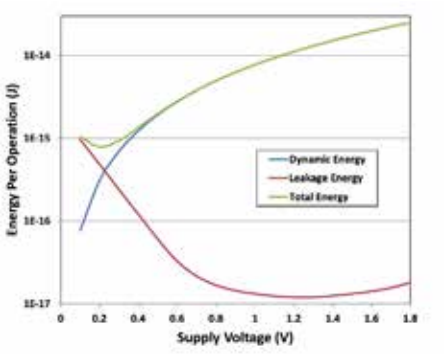


Figure 1 - Dynamic current dominates with higher operating voltage

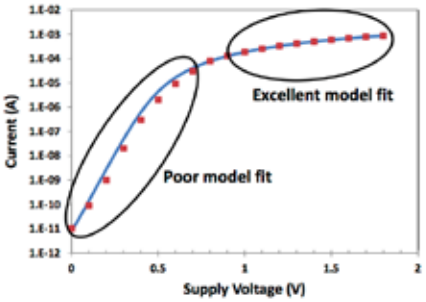


Figure 2 - Transistors haven't been well modeled below threshold

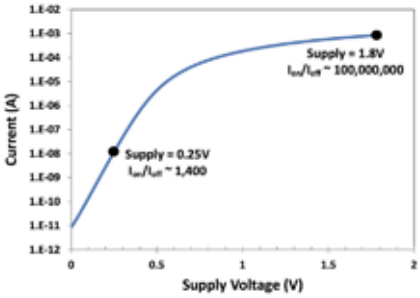


Figure 3 - The on/off current ratio is orders of magnitude smaller in the sub-threshold regime

tags, but never saw much acceptance beyond that.

After a lull that lasted a couple of decades, the topic regained some academic status in the late 1990s and early 2000s. By that time, the upcoming primacy of energy consumption was evident, and research started into ways that commercial circuit designers could reduce energy consumption. Sub-threshold design techniques were among those ideas.

The founders of Ambiq were part of that academic revival, working at the University of Michigan to develop the technology more thoroughly. That effort was spun out so that it could be fully commercialized. Ambiq is the only company utilizing sub-threshold design as a primary approach to reducing energy consumption.

It would be obvious to ask why, if this technology was developed in the 70s, it never caught on. One might even suspect that some flaw might have been uncovered that kept sub-threshold out of the mainstream. It begs the question, "If this is so easy, why isn't everyone doing it?"

The answer to that question is, "Because it's not so easy." There is no fatal flaw, but the transition from super-threshold techniques has not been trivial. Ambiq's founding team started their work at Michigan in 2004 and worked until 2010 to make the technology usable on a broad, commercial scale.

One might also ask what's changed since the 70s, when the first commercial sub-threshold devices were created. The difference is scale: Designs of the past used a few critical sub-threshold transistors – on the order of 10. At that level, each transistor can be optimized by hand. By contrast, Ambiq creates entire chips that primarily use sub-threshold transistors. That makes hand-crafting completely impractical. Designing millions of such transistors is possible only by using standard design tools and flows – preferably the same as those that have been used for super-threshold design. This is the work that Ambiq has done to commercialize sub-threshold circuits.

The challenges of modern sub-threshold

Adapting the standard super-threshold flows and infrastructure for sub-threshold design presents numerous detailed challenges. These start with the very transistors themselves.

1. Poor transistor models

The transistor model forms the basis of everything in an integrated circuit design. All of the simulations, all of the abstractions and automation, the very process of design closure: they all rely on an accurate transistor model. Most transistor modeling has focused on the "on" characteristics of the device, with little attention given to "off." The entire region between 0 V and Vth typically does not get modelled as accurately, and so existing models are inadequate for sub-threshold design, as shown in Figure 2.

2. Logic swings and noise

The output response of a transistor in the sub-threshold regime is subtle; detecting it requires great sensitivity. Currents change exponentially in response to changing voltages, but they're exceedingly small currents. In addition, the ratio of "on" to "off" current is on the order of 1000, orders of magnitude less than what super-threshold designs experience (see Figure 3). As can be expected, external noise can much more easily interfere with clean operation.

3. Sensitivity to operating conditions

Sub-threshold designs are also far more susceptible to process and environmental variation than are super-threshold designs. For example, the current in a slow process corner can be 10-100 times less than that for a nominal process. Given that the on/off current ratio (above) is only on the order of a thousand, this cannot be ignored.

Variations in temperature provide a good example of how environmental conditions create a challenge for the designer. Vth depends on temperature,

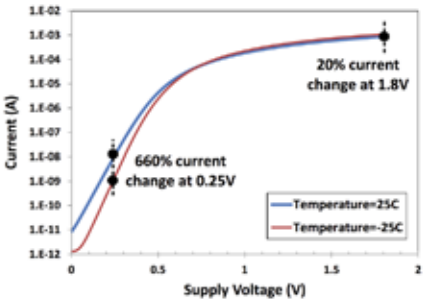


Figure 4 - Sub-threshold circuits are exponentially sensitive to temperature

and Ion depends exponentially on Vth (as shown in Figure 4 below). As a result, the "off" current at elevated temperature is similar in value to the "on" current at reduced temperature for an uncompensated circuit. Sub-threshold circuit design therefore requires extra effort to ensure that the circuits will operate as expected under all specified operating conditions.

4. Logistical challenges

Much of the manufacturing flow is based upon assumptions that are reasonable for super-threshold designs but break down for sub-threshold designs. One obvious such challenge can be found in the testers used to validate the silicon during production. The parametric measurement units (PMUs) that test voltages and currents are designed to measure microamps, not nano- or picoamps.

Even something as straightforward as device characterization has to be rethought simply because of the sensitivities that sub-threshold circuits have that super-threshold circuits don't have. Typical characterization flows may not be thorough enough to prove that the circuits operate properly under all conceivable conditions.

The fundamental nature of these challenges, combined with the fact that few engineers are skilled in dealing with sub-threshold issues, explains the challenge of commercializing sub-threshold-based circuits.

Current (A)

Ambiq's solutions

The development of Ambiq's SPOT technology, which addresses all of these challenges, has been a multi-year effort involving multi-faceted solutions, starting with a better understanding of the transistors themselves.

Ambiq recharacterized selected transistors from mainstream processes in the sub-threshold regime. It was important to start with standard low-power transistors, since the goal was to build these circuits on standard processes to keep costs down. This recharacterization effort required building numerous devices in order to capture the effects of variation and to better understand the process and environmental corners, thereby enabling the design of robust circuits.

Once the transistors were better understood, cells and circuits had to be modified to operate with sub-threshold voltages. Before doing this, the cell library was carefully surveyed and pared down. Commercial libraries tend to undergo cell proliferation as variants of standard circuits are created for different circumstances. So the first job was to select which cells from the library were to be adapted to sub-threshold operation. Once the critical cells were identified, they were then redesigned as sub-threshold circuits.

There are two goals behind these circuit design efforts. One is to manage the extreme sensitivity to changes in threshold voltage and operating condition, and the other is to optimize operation for minimal energy consumption. There are a number of techniques that can be employed in both cases, and all of them are important components of the SPOT platform.

Analog circuits, meanwhile, have required additional work. While existing super-threshold digital cells could often be modified for sub-threshold use, analog circuits typically required a fresh start. A disproportionate effort was put into creating and verifying analog circuits that were substantially different from their super-threshold versions.

None of the approaches taken is enough on its own, and none is appropriate in all cases. Ambiq's circuits are successful because they pick and choose from amongst different techniques, applying some or all of them in different parts of the integrated circuit. There is no magic formula that dictates what to use where; it takes solid engineering and good design to pull together the right combination that provides the required performance with the lowest energy, while at the same time paying attention to chip area and cost.

This need to use different techniques even applies to the type of transistor and the regime within which it will operate. In some cases, super-threshold transistors can make sense. Since super-threshold circuits are simpler, using them where they don't affect energy consumption can be beneficial.

A good example of this is the non-volatile memory (NVM) that can be used to store settings or calibration values while the device is powered down. At power-up, those values need to be loaded into active registers. Those registers will likely use sub-threshold transistors, but the NVM and the transfer

circuits can be designed with standard super-threshold transistors since they operate only at power-up and then are shut down.

The general approach Ambiq uses is to start with sub-threshold transistors as the default approach, and then to review to see if any parts of the circuit can be operated at super-threshold levels without impacting energy

consumption. Super-threshold design is simply easier, so it's preferred if power permits. In most cases, however, power does not permit it; super-threshold circuits are the exception.

There are also occasions when critical sub-threshold circuits don't achieve the required performance. In those select cases, the operating voltage for that island may be raised into the near-threshold region. To date, no circuits have had to go to super-threshold levels to get to the required performance.

So the overall strategy is to use sub-threshold circuits throughout by default, use super-threshold in those few cases where it's possible, and use near-threshold in those few cases where required for speed or bandwidth.

Ambiq Micro is successful with its sub-threshold circuits because it leverages all of these techniques as needed; this diversity of options is a critical characteristic of the SPOT platform. In particular, Ambiq's circuits involve the extensive use of dynamic, adaptive strategies that keep the circuits operating optimally even as conditions change. Sub-threshold design can be frustrating, with solutions to one problem creating new problems in whack-a-mole fashion. To some extent, it's simply hard work done by engineers skilled in sub-, near-, and super-threshold design that has allowed Ambiq to be the first company to design circuits that overwhelmingly rely on sub-threshold circuits.

Design and logistics impact

A great deal of effort has gone into ensuring that Ambiq's sub-threshold circuits leverage existing established flows wherever possible. Custom processes might make life easier, but they're not required, and Ambiq's focus is on using what is already known to work well.

The design flow was impacted based on the number of custom cell libraries and the sheer number of corners to be verified, given the various design techniques available to manage the circuit sensitivities. These design flow challenges are being encountered in the super-threshold world at the 28-nm process nodes, so solutions exist. It's just that Ambiq has leveraged those solutions at more widely available process nodes. Importantly, Ambiq's SPOT technology can also be scaled to lower geometry processes for even more energy savings as those nodes become more mainstream.

Testing challenges such as the need to measure low currents were addressed by creating complex custom probe cards and on-chip test circuitry. Those cards include specific custom current-measuring circuits that handle the measurements that the tester itself cannot manage.

Finally, the characterization flow had to be much more thorough than what would typically be done for a super-threshold design. It necessitated more detailed measurement under many more conditions and combinations of conditions than would typically be done. The impact of this is greater confidence in the robustness of the product.

In general, no step of the design and manufacturing flow has escaped scrutiny. Where elements of the standard flows have fallen short, Ambiq has modified them to ensure that the resulting product is indistinguishable from something built using super-threshold techniques - with the exception of energy consumption.

Proven reliability

Creating novel circuits means not only building something that works now, but also ensuring that the circuits will operate correctly for the life of the chip. For a system designer, reliability expectations will be the same regardless of the particular circuit techniques involved.

For that reason, sub-threshold circuits built on Ambiq's unique SPOT platform have been subjected to the usual battery of reliability tests, involving multiple lots exposed to extreme conditions over extended time periods as well as other standard tests such as electrostatic discharge (ESD). The circuits have proven themselves to be robust, and reliability reports detailing the results of these tests are available.

Conclusions

The use of sub-threshold techniques can be a powerful way to create circuits that consume dramatically less energy than those built using standard design practices. It's a fact that sub-threshold design is difficult. But, given the right experience and diligence, it is a solvable problem, and one that Ambiq continues to solve via their patented SPOT technology.

The result of these efforts are circuits that provide the same functions as more traditional ones using a fraction of the energy. There is no compromise in performance, robustness, or reliability; Ambiq's chips can operate alongside their traditional counterparts with no externally-visible difference – except for the amount of energy required to drive them. They can provide important energy savings to designers building energy-efficient systems.

Because of the fundamental nature of these innovations, sub-threshold design techniques can be applied to virtually any type of IC device. For example, Ambiq demonstrated the viability of this innovative approach with the introduction of the world's lowest power real-time clock (RTC) in 2013. The upcoming release of the world's lowest power 32-bit ARM-based microcontroller (MCU) further demonstrates the viability of extending these techniques to a completely different platform. Ambiq Micro is committed to expanding the SPOT Platform - and to giving batteries a better life.

The Changing Face of Test

› Jerry Janesch, Keithley Instruments, Inc.

Many aspects of the test and measurement business are different from the way they were relatively few years ago. Perhaps the most obvious example is the people who are using test and measurement instrumentation. A recent industry study shows that 20 percent of electrical engineers now in the global workforce started their careers within the last decade.

There have also been other significant changes in the industry; for example, manufacturing companies once typically had large staffs of dedicated test engineers; today, these companies are often outsourcing test system development and have drastically cut the size of their test engineering departments. Shrinking in-house staffs and shortened test design schedules mean that engineers have far less time available to focus on becoming instrumentation experts.

A Look Back

Test instrument design is undergoing some striking changes as instrument user expectations have evolved right along with the users themselves. For perspective on how instruments and users interactions have changed, it may be useful to look back at how instrument interface designs have evolved over the last six decades.

In the 1950s, interacting with instruments was often a laborious process. Configuring a measurement typically required twisting dials to select the desired functions and set ranges. "Taking data" often involved transcribing readings from an analog dial manually or measuring traces from a printout from a strip chart recorder with a ruler.

When digital instrumentation began to replace analog designs, the new user interface designs began to employ LED and LCD digital readouts (Figure 2). Function and range setting knobs were increasingly replaced with push-button controls. Engineers no longer needed a clipboard or notebook to record data when early communications interfaces like RS-232 and GPIB were added to instruments to support system integration and triggering, remote programming and control, as well as transfer of data to an external PC for analysis and display.

By the 1990s, users had begun to demand increasingly detailed information on their measurements, which eventually led instrument makers to begin developing brighter, easier-to-read, vacuum fluorescent displays that could display multiple measurements simultaneously from a single measurement connection. To allow users to configure the display settings and performance options,

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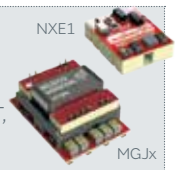

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Figure 1. Early instruments with analog interfaces required multiple front panel dials to configure measurements and results had to be transcribed manually.

Figure 2. Starting in the 1960s and continuing through the 1980s, LED and LCD digital displays and pushbutton controls increasingly replaced analog dials and knobs.

Figure 3. Vacuum fluorescent displays and multi-function buttons became increasingly common in the next stage of user interface evolution.

vendors often assigned multiple functions and performance options to the same front panel button (Figure 3).

A Look Forward

Over the last decade, instrument vendors have been striving to develop user interfaces that offer their customers more information faster. Due to shrinking design cycles, many engineers are under greater time-to-market pressure than ever before, so they need to acquire reliable data on experimental devices and circuits as quickly as possible. Although digital multimeters (DMMs), for example, have long been fixtures on every electrical engineer's benchtop, they haven't always provided the type or depth of information users need to do their jobs. To get the answers they need, DMM users have had to turn to other kinds of instruments to go "beyond the numbers."

At the same time, changes in user characteristics and expectations about ease of use have led instrument manufacturers to create user interfaces that incorporate many of the same control and display innovations that have revolutionized consumer products like tablets, smartphones, and cameras. The most prominent of these innovations is the use of advanced capacitive touchscreens with multi-point, pan-pinch-zoom-swipe operation, which simplifies interacting with data. By providing immediate visual feedback and a more content-rich display, touchscreens support faster learning than other control and display approaches and give users greater confidence in what they're doing. This can substantially reduce user learning curves and training requirements while improving measurement integrity and testing efficiency.

The intuitive nature of touchscreen interfaces allows users at all levels of testing sophistication to become experts quickly. They also offer the advantage of providing instant access to context-sensitive help, which eliminates the need to consult a user manual to get an instrument up and running. For those relatively new to testing, these instruments can speed up the measurement process by helping users test accurately and get results quickly, and allows them to focus on their next breakthrough rather than on learning how to configure the instrument. With simplified setups configured from the front panel (Figure 4), such instruments support faster time to measurement and significant improvements in test

Figure 4. The latest benchtop instruments combine intuitive touchscreen operation with functions rarely found in a single instrument. For example, Keithley's Model DMM7510 graphical sampling multimeter integrates a high speed digitizer that supports displaying and analyzing voltage and current waveforms and transients precisely.

productivity.

Simplifying the User Experience

Instruments with touchscreen interfaces aren't just for novice or infrequent users. Touchscreens allow displaying results using larger, more legible characters, provide more details about the measurement, and support on-screen data display and analysis capabilities never before available (Figures 5 and 6). The flexibility to present data graphically as well as numerically helps users explore results in a way that goes beyond the numbers. Because touchscreen displays are software defined, they are easily changed to reflect the different controls and indicators required for different applications, freeing up valuable "real estate" on the instrument's front panel.

Conclusion

As time-to-market pressures increase, more and more users will demand that their instrumentation deliver more in-depth answers quickly and without compromising measurement integrity. Fortunately, instrument vendors are coming to understand that helping their customers do their jobs with greater confidence is a prerequisite to creating successful products. To learn more about how new interface designs are redefining how users of all levels of experience interact with their instruments, visit touchtestinvent.com.

Biographical Note

Jerry Janesch is a senior market development manager at Keithley Instruments, headquartered in Cleveland, Ohio, which is part of the Tektronix test and measurement portfolio. He earned a bachelor's degree in electrical engineering from Fenn College of Engineering and a master's of business administration from John Carroll University. He has been with Keithley since 2000.

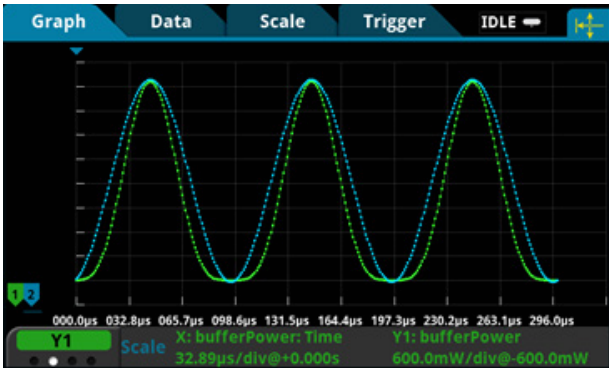

Figure 5. DMMs that combine built-in graphing utilities and a large screen make it easier to display and compare stored test results because the users are no longer so dependent on an external PC to analyze measurements.

Figure 6. Instruments with full graphical plotting windows make it easy to convert raw data into useful information easily and display it immediately. The touchscreen supports "pinch and zoom" operation to allow examining data on the graph in detail.

Modeling Grounding and Substrate Effects in Broadband Miniature Surface Mount Attenuators

› Larry Dunleavy and Isabella Delgado, Modelithics, Inc. and Harvey Kaylie, Mini-Circuits

Modelithics and Mini-Circuits have collaborated to create Microwave Global Models™ for Mini-Circuits' YAT and RCAT broadband surface mount attenuator families. These attenuators can be used to reduce signal levels, increase isolation, or improve impedance-match and retur-loss performance. Both the plastic QFN package style YAT Series and the hermetic, ceramic cavity RCAT Series are available in a tiny 2mm x 2mm footprint. The key to Mini-Circuits' YAT and RCAT attenuators' small size, excellent uniformity, and 2W power rating is the GaAs semiconductor fabrication process having through-wafer Cu metallization vias to realize low thermal resistance and wideband operation. Available values range from 0 to 30 dB and these components are well matched to 50 ohms over the entire DC to 18/20 GHz specification range.

Although these attenuators are specified to 18/20 GHz for the same configurations, measurement and model data from Modelithics shows excellent broad-band performance to 30 GHz in some cases. The Microwave Global Models demonstrated in this paper using Keysight Adbanced Design System (ADS) software, are equivalent circuit based and developed to capture component performance on both grounded coplanar waveguide (GCPW) and microstrip footprints. Not only are the models attenuation value scalable (Figure 1), but microstrip versions of the model are also substrate scalable. This means that using a single Microwave Global Model, the designer can simulate an entire family of components, experiment with substrate and ground configuration effects, and choose the most appropriate attenuation value.

Also, thanks to Mini-Circuits' sponsorship as part of the Modelithics Vendor Partner program, all attenuators models discussed here are available for free download from the Modelithics website.

Also, thanks to Mini-Circuits' sponsorship as part of the Modelithics Vendor Partner program, all attenuators models discussed here are available for free download from the Modelithics website. These attenuator Models are also included in Modelithics SELECT+ free model library.

Effect of Layout and Substrate on Performance

Layout continues to be a critical aspect of circuit design. Decisions as seemingly simple as board selection and how components are grounded can have a major impact on broad-band performance. In the creation of both attenuator models, three different ground configurations were studied - GCPW, microstrip, and "larger ground" microstrip (Figure 2). The microstrip ground configuration can be advantageous when minimizing the size and complexity of the layout is a priority. However, as seen in the performance comparison of Figure 3, the microstrip layout performance quickly deteriorates

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[i] See datasheet for suggested application circuit.
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Model	Nominal attenuation (dB)	Typical attenuation (dB)		
		DC to 5 GHz	5 to 15 GHz	15 to 18 GHz
YAT-0+	0	0.05	0.18	0.26
YAT-1+	1	1.05	1.20	1.35
YAT-2+	2	2.06	2.24	2.45
YAT-3+	3	3.05	3.25	3.51
YAT-4+	4	4.0	4.3	4.4
YAT-5+	5	5.0	5.4	5.5
YAT-6+	6	6.06	6.33	6.71
YAT-7+	7	7.1	7.4	7.5
YAT-8+	8	8.0	8.4	8.5
YAT-9+	9	9.1	9.4	9.5
YAT-10+	10	10.05	10.41	10.81
YAT-12+	12	12.0	12.4	12.5
YAT-15+	15	15.0	15.5	15.7
YAT-20+	20	20.0	20.6	21.1
YAT-30+	30	30.0	30.5	30.9

Model	Nominal Attenuation (dB)	Typical attenuation (dB)		
		1 GHz	10 GHz	20 GHz
RCAT-00+	0	0	0.2	0.5
RCAT-01+	1	1	1.3	1.7
RCAT-02+	2	2	2.4	2.7
RCAT-03+	3	3	3.4	3.9
RCAT-04+	4	4	4.4	5.1
RCAT-05+	5	5	5.5	6.2
RCAT-06+	6	6.1	6.5	7.5
RCAT-07+	7	7	7.6	8.6
RCAT-08+	8	8	8.6	9.8
RCAT-09+	9	9	9.7	11.1
RCAT-10+	10	10.1	10.7	12.3
RCAT-12+	12	12	12.8	14.8
RCAT-15+	15	15.1	16	19
RCAT-20+	20	20.1	21.4	27
RCAT-30+	30	30	30.3	29.5

Figure 1: Available values in the YAT series (left) and RCAT series (right) attenuator families.

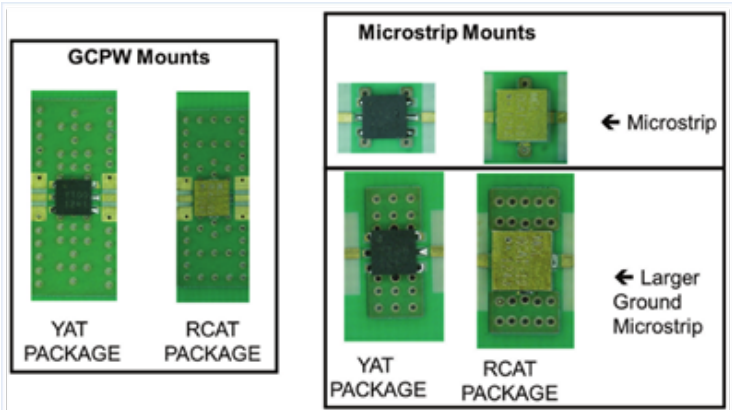

Figure 2: Three different ground layouts are shown in GCPW (left, microstrip (top right), and "larger ground" microstrip (bottom right). Designed for fixtures on to-mil Rogers 4350B

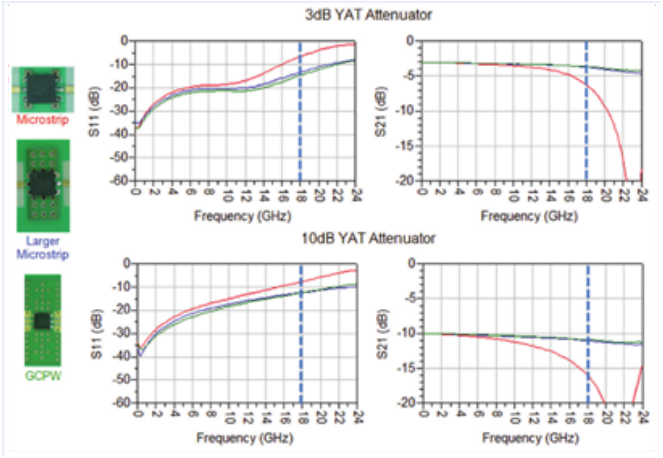

Figure 3: Measurement data comparison of microstrip (red), "larger ground" microstrip (blue), and GCPW (green) measurements for a 3 dB (top) and 10 dB (bottom) YAT attenuator. Data on 10-mil Rogers 4350B (reference planes are at the pad edge). Dashed line markes the Mini-Circuits specification limit of 18 GHz.

past 6 GHz. Note that the usable range of the attenuators can be extended by using the GCPW and the "larger ground" microstrip layouts. Both offer very similar broad-band performance.

Similar to the performance differences seen due to different ground layouts, simply changing the substrate on which parts are mounted can have a major impact on the performance observed. Figure 4 shows the changes in performance of a 10 dB YAT attenuator depending on which Rogers substrate us used for mounting. The best return loss and insertion loss are seen using a 4mil Rogers 4350B substrate, but as substrate height is increased, a reduction in broadband performance can be seen. This is likely due to the increase in via inductance with increases in board thickness.

Model Information

Four separate models were developed as a result of this collaborative effort: RCAT GCPW, YAT GCPW, RCAT Microstrip and YAT Microstrip. THE GCPW models (ATT-MCL-YAT-001-S and ATT-MCL-RCAT-001-S) are validated to 30 GHz and are also valid for the "larger ground" microstrip layout because the measurement results were effectively identical. The microstrip models (ATT-MCL-YAT-002-S and ATT-MCL-RCAT-002-S) are validated to 10 GHz and are for use with space conservative layouts and low frequency applications. These models accurately emulate all attenuator values within the family,

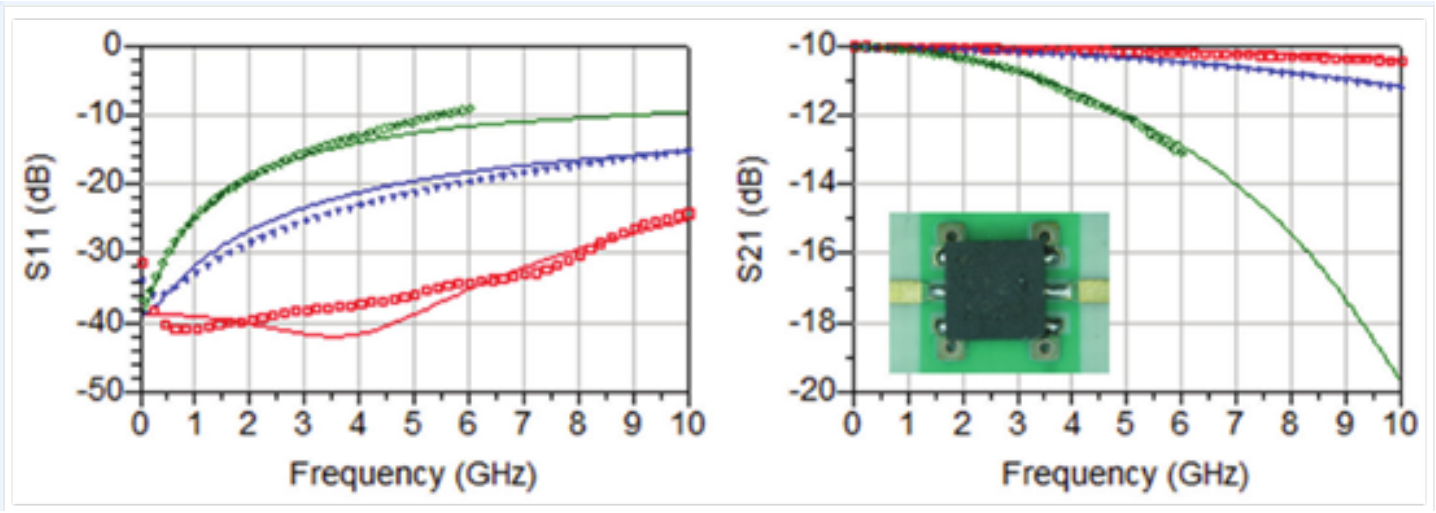

Figure 4: Substrate effects on attenuator performance. Data using microstrip configuration of 10 dB YAT attenuator: Red - 4mil Rogers 4350B, blue - 10mil Rogers 4350B, green - 60mil Rogers 4003C. Solid lines - Model data, Symbols - Measured data.

capture the effects of layout on performance for the configurations shown, and are valid for a wide range of substrates. An example of the excellent model to measurement agreement achieved by both the GCPW and microstrip models can be seen in Figure 5.

Summary

Mini-Circuits YAT Series and RCAT Series attenuators cover an attenuation range of 0 to 30 dB and are capable of broad-band performance from DC to 18.20 GHz and beyond. However, layout and board selection can strongly influence this performance. Neglecting to fully account for layout or substrate effects can lead to performance degradation and may even lead to failure meeting design specifications. This is where simulation-based design and the flexibility and accuracy of Microwave Global Models become integral in the designer's tool kit. Free, accurate simulation models for these attenuators that scale with substrate, part value, and address multiple layout configurations are now available.

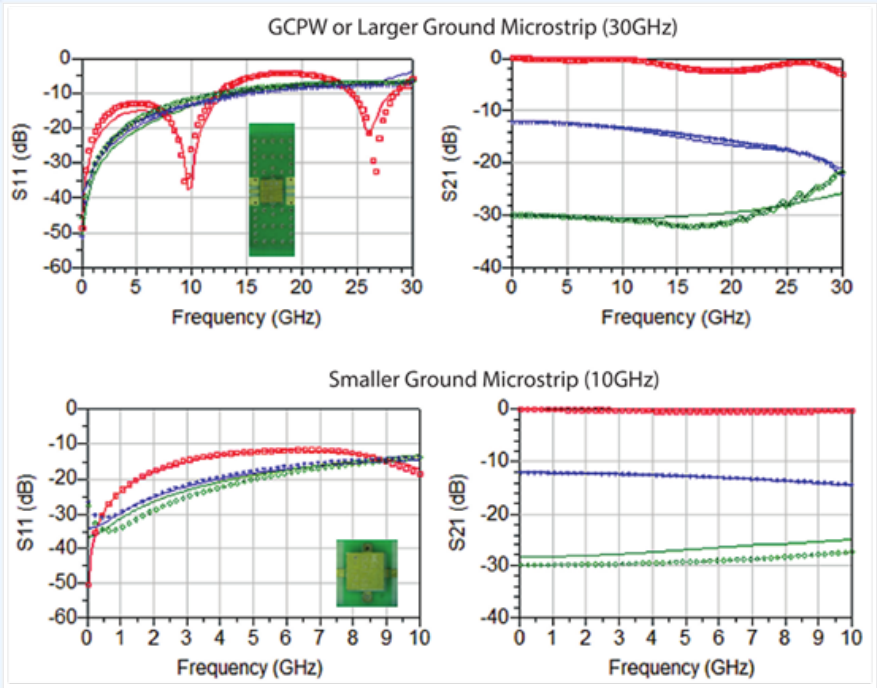

Figure 5: Modeled to measurement comparison of RCAT attenuator on GCPW or "larger ground microstrip" layout to 30 GHz (top), versus small ground microstrip performance to 10 GHz (bottom). Data shown on 4mil Rogers 4350B. Red - 0 dB, blue - 12 dB, green - 30 dB attenuator. Solid lines - Model data, Symbols - Measured data.

Acknowledgements

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The authors would like to thank Ted Heil of Mini-Circuits and Hetvi Patel, Hugo Morales and Laura Levesque of Modelithics for their important contributions to the described work.

Op Amp Input Over-Voltage Protection: Clamping vs. Integrated

› by Daniel Burton, Analog Devices Inc.

High-precision op amps enable system designers to create circuits that condition signals (amplify, filter, buffer, etc.) while maintaining the precision of the original signal. When information is contained in very small variations of the signal, it is critical that op amps in the signal path perform their operation while contributing very little DC and AC error. The performance of the total system depends on maximizing the precision and accuracy of the original signal throughout the path.

In some applications, a situation may occur in which the inputs of the op amp get driven by voltages outside the level of the supply voltages — called an over-voltage condition. For example, if an op amp is configured to run with its positive supply at +15V and its negative supply at -15V, any time an input pin goes more than one diode drop beyond those supply rails (say, ±15.7V), the op amp's internal ESD-protection diodes can be forward biased and start conducting current. Excessive input current over long periods of time (or even short periods of time if the current is high enough) can damage the op amp. This damage can result in a shift in the electrical specification parameters beyond the datasheet guaranteed limits; it can even cause a permanent failure of the op amp. When system designers are faced with this possible situation, they often add over-voltage protection (OVP) circuits at the inputs to the amplifier. The challenge then is to add OVP circuitry without adding errors (loss of system precision).

How Over-Voltage Conditions Occur

Over-voltage conditions can be caused by a number of different situations. Consider a system where a remote sensor is located in the field (for example, measuring fluid flow in a refinery) and sending its signal through a cable to data-acquisition electronics which reside at a different physical location. The first stage in the data-acquisition electronics signal path can often be an op amp configured as a buffer or a gain amplifier. The input to that op amp is exposed to the outside world and therefore can be subjected to any over-voltage incidents like a short circuit from a damaged cable or incorrectly connecting the cable to the data-acquisition electronics.

Similarly, a situation that can cause an over-voltage condition is when an input signal that is usually within the input voltage range of the amplifier suddenly receives an external stimulus which causes a transient spike that exceeds the op amp supply voltages.

A third scenario that can result in an input over-voltage condition comes from the power-on sequence of the op amp and other components in the signal path. For example, if the signal

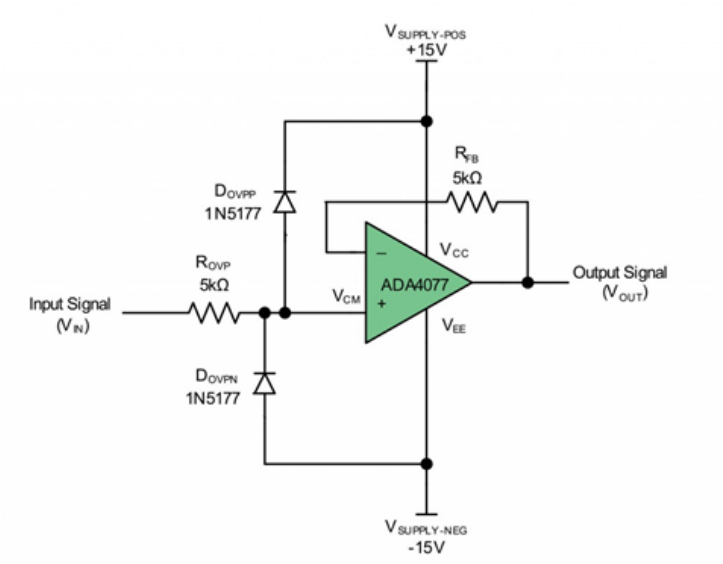

Figure 1:
Classic clamping circuit for over-voltage protection

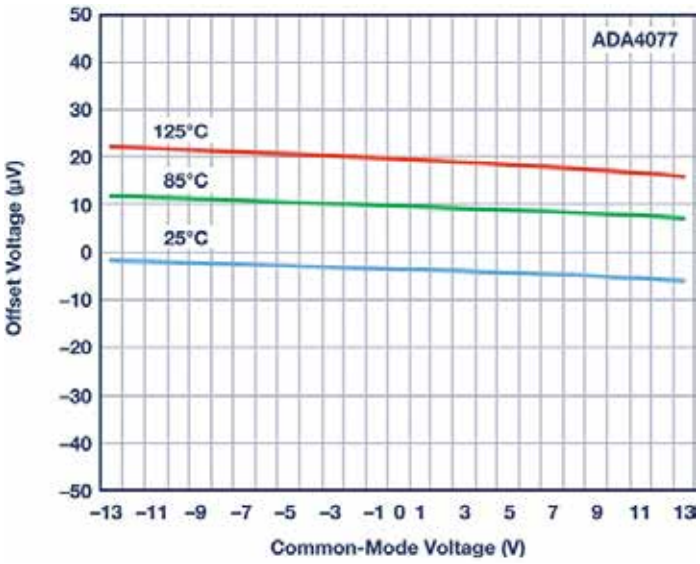

Figure 2:
Input offset voltage vs. input voltage for ADA4077

source (e.g., a sensor) gets powered up before the op amp does, the output of the source can start to output a voltage that will then be applied to the input of the op amp even though the op amp supply pins have no power yet (they are essentially at ground). This will create an over-voltage situation and likely force excessive current through the input of the op amp to ground (the unpowered supply pins).

Clamping: A Classic Over-Voltage Protection Technique

A very popular way to add OVP is shown in Figure 1. When the amplitude of the input signal (VIN) exceeds one of the supply voltages plus the forward voltage of a diode, the diode (DOVPPor DOVPN) will forward bias and send the current to the supply rails rather than into the op amp inputs, where the excess current could damage the op amp. In this application, we are using an ADA4077, an extremely high-precision and low input-offset op amp with a maximum power supply range of 30V (or ±15V). The clamping diodes are 1N5177 Schottky diodes because they have a forward voltage of approximately 0.4V, which is less than the forward voltage of the op amp's input electro-static discharge (ESD) protection diodes; thus the clamping diodes will start conducting current before the ESD diodes do. The over-voltage protection resistor ROVP limits the forward current through the clamping diodes to keep them under their maximum current rating, preventing them from being damaged by excessive current. The resistor RFB in the feedback loop is there because any input bias current on the non-inverting input can cause an input voltage error across ROVP; adding RFB will null out the error by generating a similar voltage on the inverting input.

The Trade-off of a Diode Clamping Circuit: Reduced Precision

Although the classic circuit in Figure 1does protect the op amp inputs, it contributes a significant amount of error to the signal path. High-precision amps generally have low input offset voltages (VOS) in the microvolts range. For example, the maximum VOS for an ADA4077 is 35µV over the full operating temperature range of -40°C to 125°C. Adding the external diodes and an overvoltage resistor contributes an input offset error that can be many times greater than the low offset inherent to the op amp.

Reverse-biased diodes exhibit a reverse leakage current which flows from the cathode through the anode to the supply. When the input signal voltage (VIN) is between the supply rails, the diodes DOVPNand DOVPN have a reverse voltage on them. With VIN at ground (the middle of the input voltage range), the reverse current though DOVPN is approximately equal to the reverse leakage current through DOVPP. However, when VCM moves above or below ground, a larger reverse current flows through one diode than the other. For example, when VCM is at the top of the op

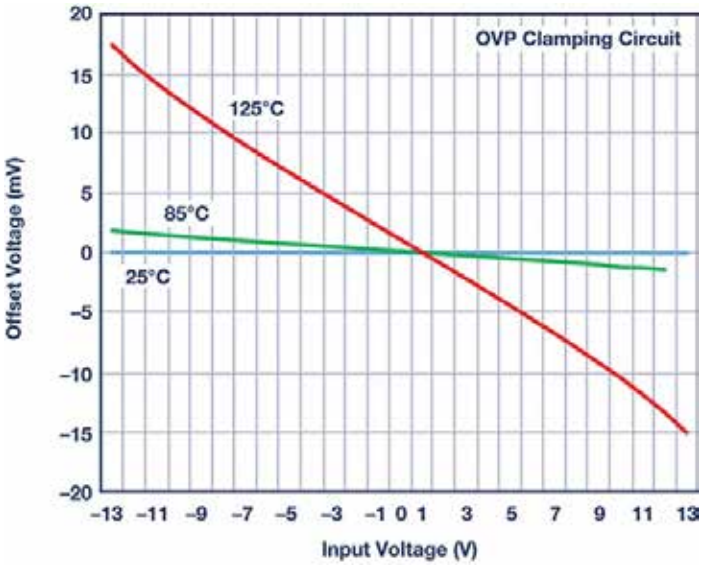

Figure 3:
Input offset voltage vs. input voltage for OVP clamping circuit added to ADA4077

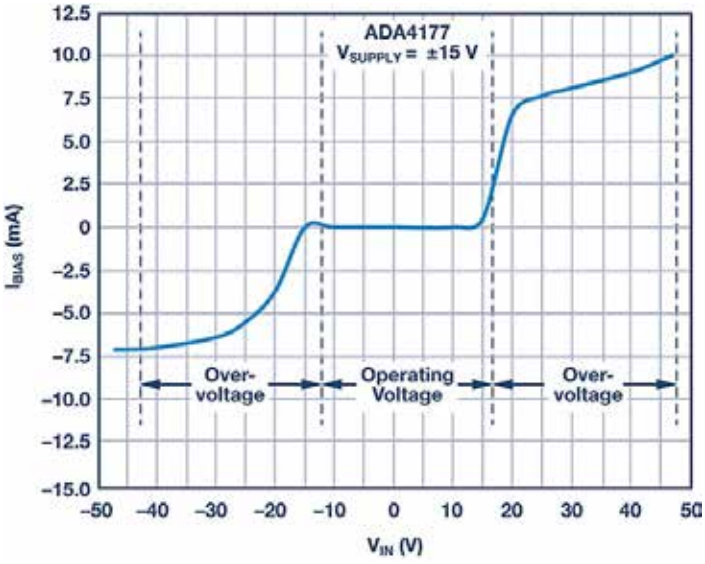

Figure 4:
ADA4177 Input bias current is restricted as over-voltage increases

amp's input voltage range (which is 2V from the positive supply or +13V in this circuit), diode DOVPN will have a reverse voltage of 28V across it. According to the 1N5177 diode datasheet, this can cause a reverse leakage current of close to 100 nA. As reverse-leakage current flows from the input signal (VIN) through ROVP, it will create a voltage drop across ROVP which looks to the signal path exactly like an increased input offset voltage.

Of additional concern is that diode reverse leakage current increases exponentially with an increase in temperature — causing an increase in the offset-voltage penalty of the clamping OVP circuit. As a baseline of comparison for op amp precision with no external over-voltage circuitry, Figure 2 shows the measured offset voltage of the ADA4077 over an input voltage range from -13V to +13V. The measurements were performed at three temperatures: 25°C, 85°C, and 125°C. Note that at 25°C, the VOS of the ADA4077 used in this test reached only 6 microvolts; even at 125°C, the VOS is only approximately 20µV.

When we add the external clamping OVP circuit to the same ADA4007 device and apply the input at VIN, we see the results shown in Figure 3. At room temperature, the VOS jumps to 30 microvolts - five times the signal path error of the ADA4077 alone. At 125°C, VOS goes to over 15 millivolts - an increase 750 times the 20 µV of the ADA4077! The precision is gone.

The 5kΩ resistor does a great job protecting the clamping diodes (and therefore the op amp) during an over-voltage condition, but it adds quite a bit of offset error - reducing precision - during normal operation when the diodes are leaking current across it (not to mention loss of precision from the Johnson noise of the resistor). What we would like is a "dynamic" input resistance that has low resistance during operation within the specified input voltage range, but high resistance during over-voltage conditions.

An Integrated Solution Provides the Answer

The ADA4177 is a high-precision, low-offset op amp which includes integrated over-voltage protection. The integrated ESD diodes act as overvoltage clamps to protect the part. Depletion-mode FETs are in series at each input before the ESD diodes. They provide the dynamic resistance which increases when the input voltage (VCM) exceeds the supply voltages. As input voltage increases, the drain-to-source resistance (RDSON) of an internal FET increases, thus restricting the current flow exponentially with the increased voltage (Figure 4). Because the ADA4177 uses depletion mode FETs on the inputs and not a series protection resistor, the op amp doesn't suffer the offset-voltage penalty across the resistor that the clamping OVP circuit does.

The ADA4177 can withstand voltages on its inputs up to 32 Volts beyond the supply voltage. It limits overvoltage current to a typical 10-12 mA, protecting the op amp without the use of any external components. As shown in Figure 5, even at 125°C, this tested unit is showing an offset voltage of only 40 microvolts. That's

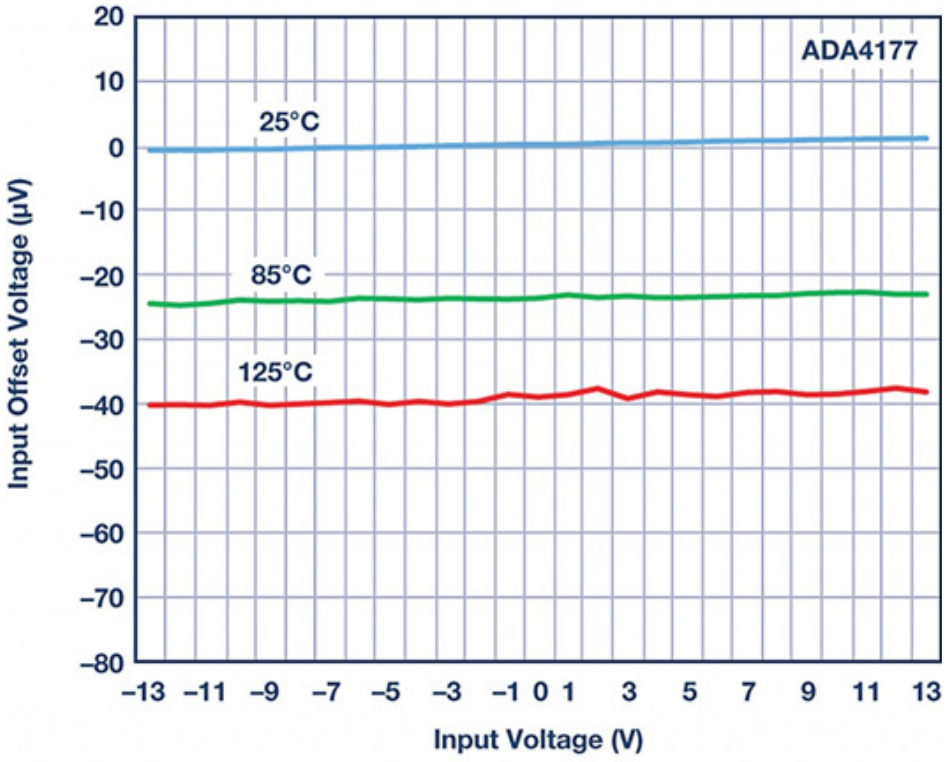

Figure 5:
Input offset voltage vs. input voltage for ADA4177 with its integrated OVP

less than 3% of the error that the clamping circuit showed at that temperature! Precision is maintained.

What This Means to System Performance

When analyzing the effect of varying input voltage on the precision of the signal path, a system designer will consider the amplifier's common mode rejection ratio (CMRR). This is a measure of how much of the common-mode input voltage is rejected from showing up on the output (or how little gets through). Since op amps are often configured to provide gain between the input and the output, we normalize the CMRR specification by referring to change in the input offset voltage (the change in output divided by the amplifier closed-loop gain). The common mode rejection ratio is a positive value expressed in dB and is calculated by the following formula:

$$CMRR = 20 \log (\Delta VCM / \Delta VOS)$$

From this ratio, we see it is clearly desirable to keep the VOS as small as possible. The ADA4177 is specified to have a guaranteed minimum CMRR limit of 125 dB over full operating temperature. Using the test results from the units measured in this experiment, we can calculate and compare the CMRR of the clamping circuit and the ADA4177. Table 1 shows the extreme loss of precision when using the classic clamping diode circuit and the excellent CMRR of the ADA4177 with its integrated FET over-voltage protection.

Over-voltage protction method	25°C	85°C	125°C
ADA4177	143 dB	145 dB	142 dB
ADA4077 + Clamping OVP	113 dB	78 dB	58 dB

Table 1: CMRR Comparison of ADA4177 to Discrete OVP with Clamping Diodes

For more information on designing high-precision amplifier circuits with over-voltage protection, see:

Robust Amplifiers Provide Integrated Overvoltage Protection by Eric Modica and Michael Arkin, Analog Dialogue Volume 46, February 2012:http://www.analog.com/library/analogDialogue/archives/46-02/ovp.html

How ARM Servers Can Take Over the World

› Paul McLellan, Cadence

One of the big themes of the Linley Data Center Conference last week was the possibility that ARM could finally start to get traction in the data center. In the opening keynote, Linley Analysts Jag Bolaria and Bob Wheeler said that microservices and hypercovergence are creating opportunities for ARM but that they would be less than 5% of the market this year. Actually, considering that they are at pretty much zero today, that would be something that looks like the beginning of success.

In fact, with perfect timing, just before the conference opened, Google and Qualcomm announced that they would be working together. Or at least there were off-the-record reports that they would. Since Google installs over 300,000 CPUs per year, even a small percentage being ARM would start to be a large number. Other providers, in particular Amazon, install CPUs at a even higher rate.

The keynote on the second day was by Jon Masters of Red Hat, where he is the chief ARM architect. His talk was titled, How ARM Servers Can Take Over the World. He subtitled it, "or how an industry is coming together to do something disruptive." Red Hat have been involved with ARM servers since the beginning, including co-intitiating many standardization activities associated with ARMv8. He gave a brief history of their involvement:

- 2011: Red Hat ARM team formed, industry standardization effort begins, secret RED Hat ARM v8 OS bootstrap begins, ARMv8 architecture announced, Red Hat on stage with AppliedMicro (showing X-Gene)
- 2012: Many design collaborations initiated, Linaro Enterprise Group (LEG) started, OpenJDK initial release. Showed the bicycle powered ARM server to show potential of low-energy compute.
- 2013: ARMv8 hardware arrives at Red Hat, world's first public demonstration, Broadcom announces Vulcan ARMv8 server processor.
- 2014: ARM server base system architecture (SBSA), ARM server base boot requirements (SBBR), Red Hat on stage with Cavium (ThunderX), Red Hat demonstrates rack-level provisioning and launches ARM early access program
- 2015: Ceph Cluster (AppliedMicro X-Gene, AMD Seattle, Cavium ThunderX and others), Red Hat Enterprise Linux Sever 7.1 and 7.2 development previews, Qualcomm announces 24-core prototype server SoC

What is driving potential growth of ARM servers? Jon pointed out four trends:

I don't think I need to tell any reader here about SoC integration.

Changing workloads refers to the fact that traditional, often proprietary, workloads are being replaced with open-source software that doesn't have the same porting challenges.

Jon Masters, the chief ARM architect

In fact, a lot of software runs at even higher levels. For example, all big data runs on top of the JVM (Java Virtual Machine), meaning that it is insulated from the underlying architecture. There are already two good JVM implementations on ARM (OpenJDK and Oracle).

Migration to the cloud, with the hundreds of thousands of servers typically involved, means that it starts to be economical to invest in customized designs. In fact, Intel does this themselves already, with semi-custom Xeon designs that public clouds such as Amazon run today. Jon reckons that 20% better price/performance is enough to justify the move, although in the panel session later in the day people thought 2X was more compelling.

The fastest growth market for data center solutions is the Chinese domestic market. Just like in the US where we have Amazon, Microsoft, Google, Facebook and more, they have Baidu (search), Alibaba (shopping) and Tencent (social media). But demand exists for locally developed technologies (and government pressure may change to mandate). Since ARM is an IP company, it is easier to build a local-content ARM server than a local-content x86 server. Jon said that there are many serious proof-of-concept projects in flight with lots of rumors around the big public clouds (such as the Google/Qualcomm one). Server silicon is now available from AppliedMicro, Broadcom, Cavium, Qualcomm, HiSilicon and AMD. A large number of operating systems, not just Red Hat, are available. Hypervisors such as Xen are available. JVMs are available, as I mentioned above. Various higher levels of the stack, such as openstack, are available.

ARM servers require standards to take off. They need to "just work" the way that Intel-based servers do today, out of the box. Unbox, plug into rack, provision via the network. In short, give the users a phenomenally "boring" experience.

To wrap up Jon talked about what not to do, and then what you should do:

- Don't ship some hack with your custom hacked-up distribution and kernel of the day
- Don't ship special "OS" that has no upgrade path
- Do ship a standards-compliant platform upon which the user can install the OS of their choice
- Do have a great plan for deploying firmware updates, documentation, overall user experience
- In short, standards, standards, standards

Jon pointed out one great example of what you should do: the Qualcomm Software Development Platform. The engineering is phenomenal and Red Hat (and presumably Jon himself) have found them a pleasure to work with. The trick is to make using an ARMv8 server as boring and uneventful as using an Intel-based server, and ensure that whatever software you need "just runs."

We can only wait and see now.

Back to basics - Reliability considerations in power supplies

› By CUI Inc

Introduction

The importance of reliability can be best demonstrated using an anecdote I was told by a friend back in 2008; when working for a major IC firm from San Francisco, he had received a shipment of new and somewhat problematic desktop PCs.

Within months these PCs had started to crash, with the IT department being rolled in to fix the assumed operating system gremlins and / or viruses that were affecting these new computers – to no effect. After much investigation, and with many a stripped down PC, it was eventually revealed that the problem was caused by substandard bulk capacitors in the ac-dc power supply. These had deteriorated in use, and were causing the supply rails to be out of regulation, producing the random crashes.

The episode highlights that, while power supplies may not have the glamour, nor get the attention that processors and displays receive, they are just as vital to system operation. Here we look at reliability in power supplies, how it's measured and how it can be improved.

Predicting the power supply's expected life

First, a few definitions:

Reliability, R(t): The probability that a power supply will still be operational after a given time

Failure rate, λ: The proportion of units that fail in a given time, note, there is a high failure rate in the burn-in and wear-out phases of the cycle – see figure 1

MTTF, 1/λ: The mean time to failure.

MTBF (mean time between failures) is also commonly used in place of MTTF and is useful for equipment that will be repaired and then returned to service. MTTF is technically more correct mathematically, but the two terms are (except for a few situations) equivalent and MTBF is the more commonly used in the power industry.

A supply's reliability is a function of multiple factors: a solid, conservative design with adequate margins, quality components with suitable ratings, thermal considerations with necessary derating, and a consistent manufacturing process.

To calculate reliability - the probability of a component not failing after a given time - the following formula is used:

$$R_{(t)} = e^{-\lambda_A t}$$

For example, the probability that a component with an intrinsic failure rate of 10-6 failures per hour wouldn't fail after 100,000 hours is 90.5%, after 500,000 this decreases to 60.6%, and after 1 million hours of use this decreases to 36.7%.

Going through the mathematics can reveal interesting realities. First, the failures for a constant failure rate are

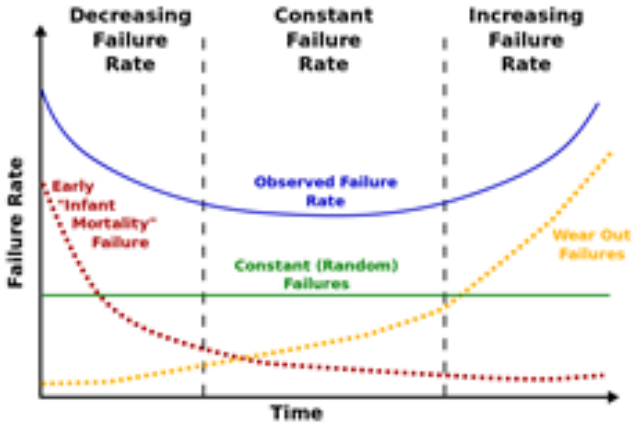

Figure 1: The bathtub curve, failure rate plotted against time with the three life-cycle phases: infant mortality, useful life and wear-out.

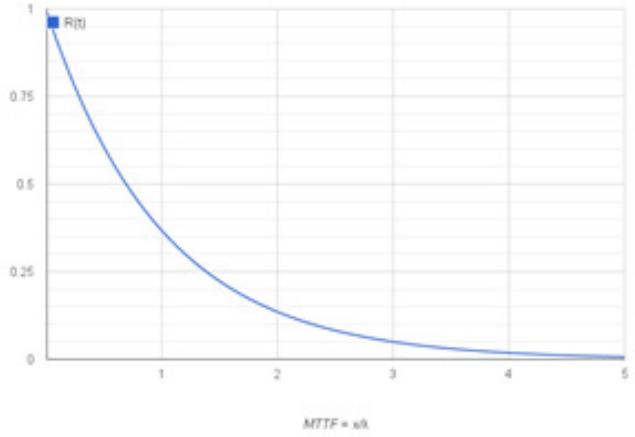

Figure 2: Curve showing the probability that a component is still operational over time.

characterized by an exponential factor, so only 37% of the units in a large group will last as long as the MTBF number; second, for a single supply, the probability that it will last as long as its MTBF rating is only 37%; and third, there is a 37% confidence level likelihood that it will last as long as its MTBF rating. Additionally, half the components in a group will have failed after just 0.69 of the MTBF.

It should also be noted that this formula and curve can be adapted to calculate the reliability of a system:

$$R_{(t)} = e^{-\lambda_A t}$$

Where λA is the sum total of all components failure rates (λA = λ1n1 + λ 2n2 + … + λini)

Calculating the failure rate

Three methods can be used to calculate failure rates, prediction (during design), assessment (during manufacturing) and observation (during service life).

Prediction uses a standard database of component failure rates and expected life, typically MIL-HDBK-217 for military and commercial applications or Telcordia for telecom applications.

The MIL approach requires use of many parameters for the different components and includes voltage and power stresses, while Telcordia requires fewer component parameters and can also take into account lab-test results, burn-in data, and field-test data. Finally, the MIL approach yields MTBF data, while Telcordia produces FIT numbers, (failures per billion hours).

Using these databases and techniques means several, often incorrect, assumptions need to be made, such as the assumption that the design is perfect, the stresses are all known, everything is operated within its ratings, any single failure will cause complete failure, and the database is current and valid.

But, it is the least time consuming method and by applying it consistently across different designs, it can indicate the relative reliability of topologies and design approaches, rather than absolute reliability.

Conversely, assessment is the most accurate way of predicting failure rate, but requires greater time and resources. This method subjects a suitable number of final units to an accelerated life test at elevated temperature, with carefully controlled and increased stress factors.

One method, the HALT (highly accelerated life test) approach, tests a number of prototype units under as many conditions as possible, with cycling of temperature, input voltage, output load, and other impacting factors. HALT testing seeks to fatigue a component, PCB, subassembly, or finished product through either intense stressing for fewer cycles, or low level stressing for more cycles.

A second method, HASS (highly accelerated stress screen) testing is an accelerated reliability screening technique used to reveal latent flaws not detected by environmental stress screening, burn-in, or other test methods. HASS testing uses stresses beyond initial specifications, but still within the capability of the design as determined by HALT.

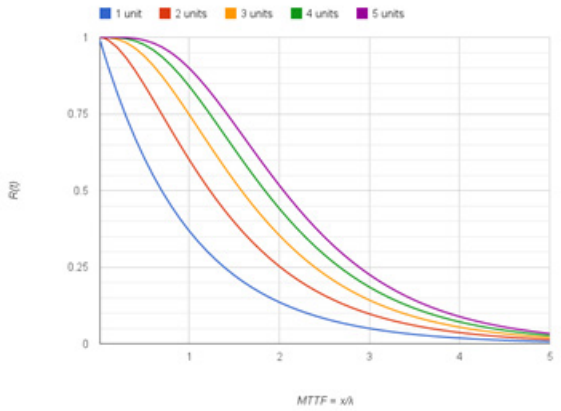

Figure 3: The effect of redundancy on the MTTF.

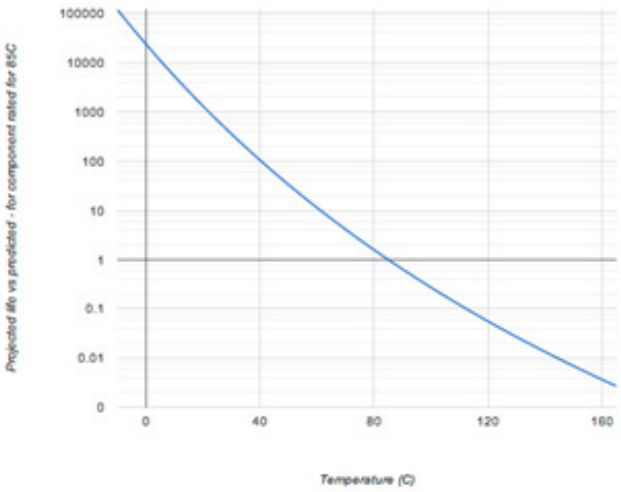

Fig 4: Effect of temperature on a component's projected life. Plot is based on a component rated for 85oC and an activation energy (Ea) of 1.0

The stresses in HASS are more rigorous than those delivered by traditional approaches, so HASS testing substantially accelerates early discovery of manufacturing-process issues. Reliability engineers can then correct the variations that would otherwise lead to field failures and greatly reduce shipment of marginal product.

Observation in the field is also possible, but this is more difficult as it is impossible to control all of the conditions a supply has been subjected to and therefore more difficult to undertake reliable causation analysis.

Stresses that affect power supply reliability

Power supply life is affected by three kinds of stress: thermal, mechanical, and electrical. A quality design anticipates each of these and takes necessary steps to minimize both their occurrence and their impact.

Thermal stress takes two forms: static and dynamic. Static thermal stress, where supplies are operated at elevated temperatures, degrades components and their basic materials. Bulk capacitors may begin to dry out, or their seals may be stressed, and even resistor coatings may begin to deteriorate and break down. Interconnection and mating areas can expand and mismatch.

Dynamic stress is associated with the heating and cooling cycles and the resulting expansion / contraction, which leads to micro-cracks.

Mechanical stress severity depends on how and where the supply will be installed and used. This stress can cause both intermittent and hard failures, as cracks develop and circuit connections start to open and, in some cases, reconnect.

Electrical stress is any voltage, current, etc. that is applied to a device. Over-stress occurs when a component is operated beyond its rated value, either through poor selection or one-time events. For example, a capacitor may be rated to 100 VDC, but sees a 150 VDC spike in operation.

Improving power supply reliability through design

Obviously, the paper design and topology should be robust and cautious. This should take into account the effects of load and line transients, as well as noise. The designer should also carefully determine the required minimum/maximum values of component parameters to ensure reliable operation (a "typical" value is nearly meaningless), as well as those for critical second- and third-tier parameters; including less-publicized factors in the magnetic components, such as temperature coefficient of some values.

We've discussed the need to manage operational temperatures and a thermal analysis of the design and its physical implementation is therefore critical.

SPICE (simulation program with integrated circuit emphasis) or similar modeling of the design is essential, using realistic, not simplified, models of the components and PC boards and tracks, to verify both static and dynamic performance. And, the choice of components must be done with conservative bias, with extra margin in both initial and long-term values for many of their specification values. Furthermore, the layout must accommodate the fact that most

supplies are dealing with significant current flows, on the order of 10, 20 or more amps.

After design, the next critical step is selection of specific components. As it's nearly impossible to distinguish a poorly made or counterfeit unit, vendor credibility is key. Furthermore, components must be compatible with the manufacturing process; with mounting tabs, sufficiently large connection points and heavy wire leads, or screw terminals where appropriate.

And, on the subject of design for manufacturability, even the basic soldering process used in supply construction is an area for consideration. While the common reflow-soldering temperature profiles are well established, the regulatory mandate for lead-free (Pb-free) components and solder also means that a different reflow soldering profile is needed and all components used must also be qualified to perform to specification after this higher reflow temperature and soak time.

Improving power supply reliability through over specification

In addition to a cautious electrical design, the power supply vendor can do many things to increase overall reliability.

Using components that are inherently more reliable - by their physics, their design, their materials, or their manufacturing and test process – can significantly reduce the overall risk but does add to the overall cost. In power supplies the most common failure point is the capacitor, and, therefore, using longer-life capacitors will have the greatest effect.

A second way is to introduce redundancy. As we can see in figure 3, the probabilities of more than one unit failing are quite low. For example, if the reliability of any single unit is 0.99, then the probability of both units failing is 0.9999 in an N=1 design.

As we have already stated, just 37% of supplies will be operational after the MTTF. However, by adding just one additional supply, 60% of systems will have at least one operating supply after the same time period has elapsed.

Taking this to extreme, we can calculate that if we incorporate five power supplies into the design, more than 50% of systems will be still have a functioning supply after twice the MTTF has elapsed.

The N+1 method brings higher up-front cost, but does allow for a hot-swap capability to replace the failed supply.

Additionaly, using components at levels well below their rated specifications is a relatively simple method of enhancing reliability.

If we look at temperature, a component rated for reliable operation at 85°C will have a significantly improved lifespan if used at 55°C - typically, a component's life doubles for every 10°C decrease in temperature.

Minimizing temperature rise and temperature cycles is the most direct way to increase reliability, and this temperature-versus-life relationship is based on an adaptation of the Arrhenius equation:

$$A_R = e^{((Ea/k).(1/T_1-1/T_2))}$$

Ea = activation energy for the processes that lead to failure – typically 0.8eV to 1.0eV

k = Boltzman's constant 8.617×10^{-5} ev k^{-1}

T is temperature (°K), typically at ambient room temperature (298.15°K, 25°C)

But, because it is dependent on how the customer mounts the supply, its enclosure, additional components in the enclosure, its ambient conditions, the use or non-use of active cooling such as fans, and other factors, this will often be beyond the OEM's direct control.

Next on the list is burn-in testing. If we look back to figure 1, failure is significantly more likely during the early stages of a components life than it is during its useful life. Burn-in testing weeds out units that would have failed early in the field and therefore would have brought down the overall reliability rating.

Summary

Reliable supply design is not a guessing game. A reliable supply requires suitable design and analysis, components, manufacture process, test, and installation.

No single step will ensure a reliable supply, although there are many ways to decrease the supply's reliability.

When a vendor analyzes the supply's expected reliability, it is important to be consistent in databases, models, environmental conditions, and manufacturing in order to yield meaningful results, which can be compared across different power supplies and implementations.

At CUI we follow best practices to ensure our power supplies are among the industry's most reliable. For further information on our power supplies and how they can be used to increase your system's reliability visit www.cui.com.

A new kind of challenge

Mark Adams, AMP

Here Mark Adams of The AMP Group explains why power is presenting a new design challenge for the industry, and how it's being addressed.

The word 'digital' has been adopted by many sectors outside of electronics to represent a new era in efficiency, quality or simply just ability. In truth, as those inside the electronics industry will already appreciate, digital is all about intelligent control, and subsequently it works symbiotically with the analogue world. The term 'digital control' is equally rife within the industry because it truly does represent a new era in efficiency, particularly in reference to power supplies.

Continued and prolonged semiconductor breakthroughs - known as Moore's Law - has resulted in incrementally greater integration, leading to higher power demands at the board level, where power density continues to rise. The driver behind this increasing power density is predominantly the demand for functionality, which inevitably requires more power-hungry processors within a given form factor; nowhere is this more apparent than in the communications sector, fuelled by the trend for ubiquitous connectivity. The demand for on-demand video services, the Internet of Things and our online lives in general means network traffic is rising at an incredible rate; according to the recent Ericsson Mobility Report, annual IP traffic will reach 7.7 zettabytes by 2017 - an increase of 1 zettabyte year-on-year since 2012.

The power demands for this level of processing is already seeing individual processors requiring well above 100A at voltages as low as 0.6. Managing that demand will require power supplies that not only operate efficiently under steady-state conditions, but are able to react to large and frequent fluctuations; it demands intelligent digital control. For developers, this represents a significant challenge, one that is increasingly being met through the use of proven solutions in the form of modularised power since the time and resources needed to design such complex discrete solutions are no longer an option for OEMs.

However, while the challenge of meeting power demands can and has been moved to the module provider, their challenge is also increasing. With such high currents and tolerances to deliver, there is no room for compromise, which is forcing module providers to accelerate the development of intelligent digital control for power supply modules. This is the new challenge that the power industry now faces, and while digital control may not lead to smaller power supplies, it will provide greater stability and flexibility, allowing it to successfully address more complex power applications.

And although applications require leading edge performance from the power module, OEMs are still demanding a multi-source solution to minimize supply chain risk. The digital layer that allows power modules to address challenging applications also adds a new layer of complexity to the module. Through unprecedented collaboration, three of the industry's leading power supply companies have formed the Architects of Modern Power Group (www.ampgroup.com) and are working together to deliver the most technically advanced end-to-end distributed power solutions to deliver true plug-and-play multi-sourcing. This long-term strategic alliance will enable the power design community to benefit from world-leading technology innovation and unrivalled supply chain security.

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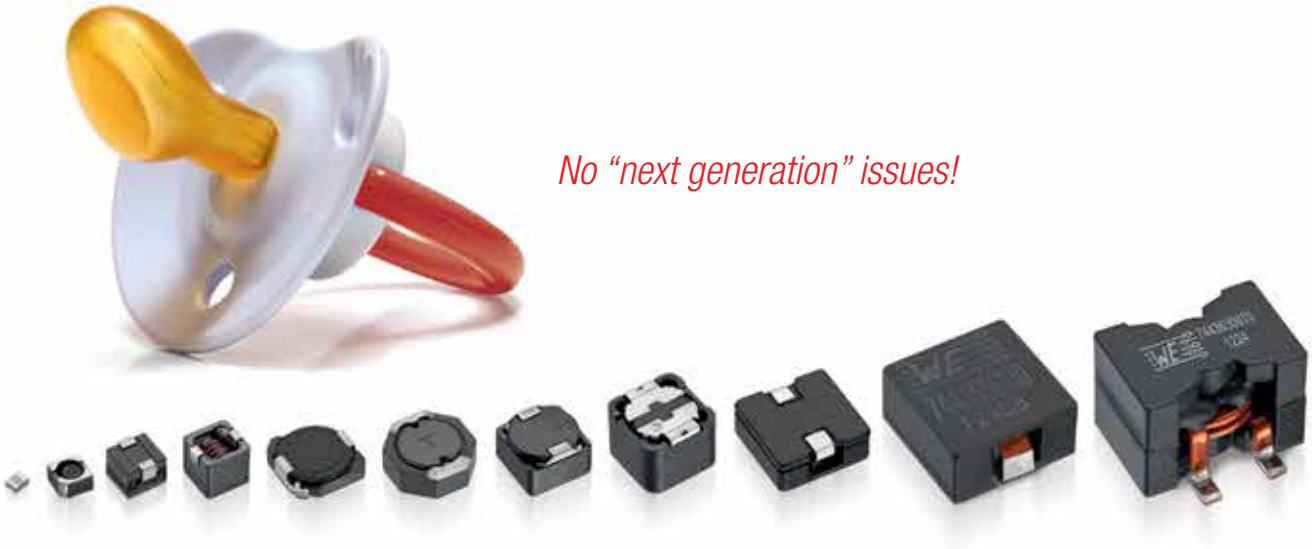

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How Network-Function Virtualization Enables New Customer-Premise Services

› Haim Cohen NXP Semiconductors

This paper describes how network-function virtualization (NFV) and software-defined networking (SDN) will help network operators profit from greater flexibility and the faster rollout of new revenue-generating services. Important building blocks in this transformation are embedded processors optimized for networking and communications. NXP's QorIQ processors are well positioned to meet the requirements of virtualized network services. The Linley Group prepared this paper, which NXP sponsored, but the opinions and analysis are those of the author.

Squeezed by rapidly growing data traffic and customer demand for new services, network operators need to upgrade their network architecture and change their business model to become more efficient, nimble, and profitable. Consequently, everyone is talking about network-function virtualization (NFV) and software-defined networking (SDN) as the most promising solutions. Although the buzz revolves mostly around data centers and cloud servers, NFV and SDN will also change network-edge devices and even customer premise equipment. Small-business and enterprise branch-office routers are prime candidates for these changes, but home gateways will soon evolve, too. NFV and SDN are really end-to-end solutions that can make every network component more efficient, flexible, and cost effective.

In addition to helping operators manage escalating costs, SDN and NFV can generate new revenue by rapidly adding new services. One example is virtual customer-premise equipment that can offer new features such as antivirus security, a firewall, a virtual private network (VPN), and unified communications for voice and data. Typically these services are distributed on both the local and the remote equipment. To quickly add new services or to reconfigure existing ones, operators need a flexible cloud.

Migrating Away From Fixed-Function Hardware

SDN makes the network more flexible by replacing dedicated fixed-function hardware with programmable hardware and open software. NFV scales performance by implementing the networking functions in general-purpose virtual machines. Racks of multipurpose systems can perform the same functions as the expensive function-specific equipment that proliferates in today's central offices and Internet points of presence.

Network operators want the freedom to easily port the virtual network functions (VNFs) among platforms from different vendors.

Variable workloads are more easily balanced on multipurpose hardware that can adapt to rapidly changing conditions; adding capacity is easier and less expensive when the hardware is standardized and programmable; single points of failure vanish when tasks can quickly migrate to other hosts; software upgrades can quickly offer new services; and equipment maintenance is easier, thus improving reliability and security.

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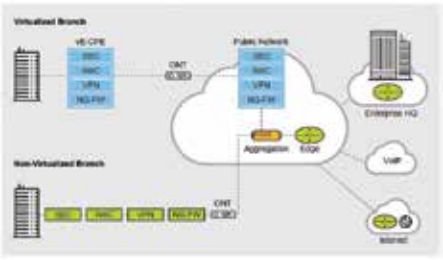


Figure 1. Software-defined networking (SDN) and network-function virtualization (NFV) extend to the premises. Functions implemented in separate systems in a classical nonvirtualized branch can be implemented in virtual enterprise customer-premise equipment, hosted either at the branch or at an aggregation site in the public network.

combine acceleration hardware with general-purpose processors to run the control-plane and high-level data-plane tasks. As Figure 2 shows, new industry standards such as OpenFlow (OF), Open Data Plane (ODP), and Open Platform for NFV (OPNFV) enable developers to write software that's more flexible and more portable to multipurpose "white box" hardware. Looking beyond data centers, central offices, and the cloud, this evolution must be an end-to-end transformation. It must include not only the network core, but also its edges,
its access points, and even the customer premise equipment (CPE). Although virtualized functions such as vRouters in the network are vital links in the chain, virtual CPE (vCPE) completes the link and allows network operators to offer new services.
The vCPE is still a box located on the customer's premises, but the VNFs it supports can run either locally and remotely. Network operators can use them to deliver new services such as those described above. The VNFs may not be co-located but the services are often chained together within the network and the vCPE for a cohesive user experience.
Whether the operator implements these services locally or remotely is transparent to the end users.

Standards Create a Multivendor Environment

Most routers already separate the control plane and data plane. SDN and NFV don't alter those basic functions but do change their implementations. SDN enables a reconfigurable data path that software can modify on the fly in response to changing conditions. NFV enables a customizable network, so operators can add new services more quickly than legacy equipment would allow. Software interfaces created by the industry's new open standards (such as the aforementioned OF, ODP, and OPNFV) help to enable this flexibility by inserting abstraction layers between the application software and the underlying hardware. Programmers can write portable high-level code to application programming interfaces (APIs) without worrying about the underlying hardware-thus enabling software portability across platforms. These standards enable network operators to choose equipment from different OEMs.

Solution: Optimized Embedded Processors

SDN and NFV can be implemented on embedded processors that are optimized for communications, virtualization, programmability, and security. These optimized solutions embed hardware accelerators that are more power efficient for specialized tasks than general-purpose processors. Additionally, they integrate networking and storage interfaces that enable smaller system designs and high density.
NXP's QorIQ processors represent the ideal marriage of processing power and hardware engines for SDN and NFV applications. Depending on the particular chip, these processors may include NXP's Security Engine (SEC), which handles all the popular cryptography algorithms and protocols; the Data Compression Engine (DCE), which accelerates popular compression and decompression algorithms; the Pattern-Matching Engine (PME), which can perform regular-expression (reg-ex) operations for deep packet inspection (DPI); and the Data Path Acceleration Architecture (DPAA), which accelerates many low-level packet-processing functions. Where present, all this optimized hardware works together to accelerate the data plane. Furthermore, it is user programmable and supports standard APIs such as ODP for easy application portability.
QorIQ processors also support virtualization in hardware, and they are fully programmable. NXP offers some off-the-shelf software under its VortiQa brand, such as the Open Network Switch Software and the Open Network Director Software. Both are commercial-grade products for switches, routers, and gateways in enterprises, data centers, and customer premises. Both of these VortiQa products also comply with the Open Networking Foundation's OpenFlow 1.3 protocol. Third-party software suppliers offer additional ready-made solutions, and developers can fine-tune their own networking software. This programmability includes the hardware accelerators as well as the general-purpose CPU cores.
In addition, some newer QorIQ processors have a significantly enhanced version of DPAA. This second-generation DPAA2 is available in the QorIQ LS2085A and LS1088A,
a pair of ARM-based eight-core processors. It is also being designed into NXP's future ARM chips.
Figure 3 shows how a QorIQ LS1043A processor can enable vCPE in a router using industry standards such as OpenFlow and Open Data Plane. This 64-bit processor has four ARM Cortex-A53 cores, providing ample general-purpose processing muscle for this application. For packet acceleration, it has DPAA and a SEC engine. Network interfaces include a 10 Gigabit Ethernet (10GbE) port and five Gigabit Ethernet (GbE) ports. For additional I/O, it has three PCI Express (PCIe) controllers and a SATA

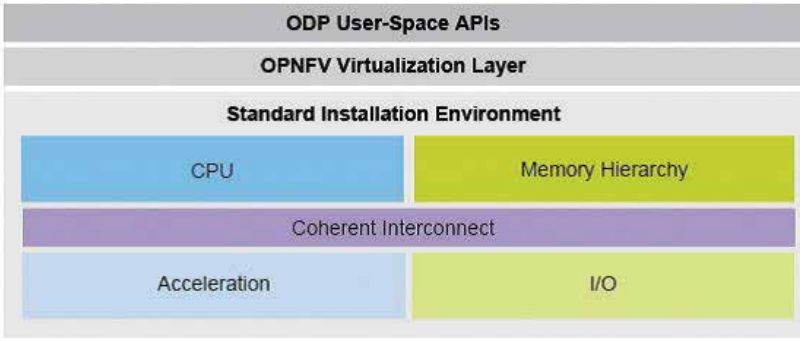


Figure 2. Standard software enables interoperability and portability across multiple vendors. NXP is a co-founder or contributor to several of these industry standards.

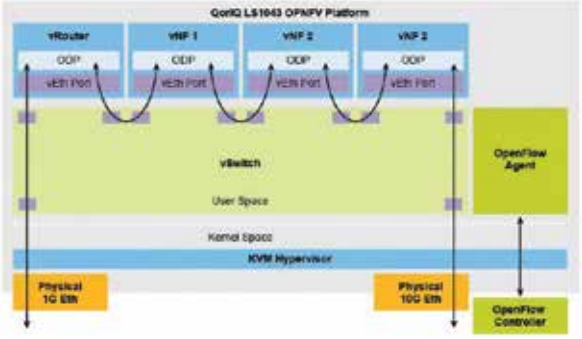


Figure 3. The basic building block of this virtual customer-premise equipment is a QorIQLS1043A quad-core ARM processor with packet acceleration, a cryptography engine, hardware support for virtualization, and fast I/O and network interfaces

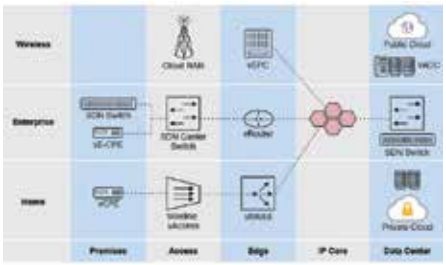


Figure 4. SDN and NFV are overhauling the whole network architecture, not just the hardware in data centers and central offices.

III controller. A 32-bit DRAM controller supports low-power DDR3L or higher-performance DDR4 external memory.

Using this building block and industry-standard open APIs, designers can implement a vCPE router. It runs a hypervisor in the kernel space and a virtual multiport Ethernet switch in the user space. VNFs running on the Open Data Plane layer can share the physical Ethernet ports through their virtual Ethernet (vEth) ports. This design implements multiport switching in hardware-accelerated Open vSwitch software instead of using a dedicated hardware switch that's either on or off the chip. The virtual switch is fast enough for this vCPE application and is more flexible than a dedicated Ethernet switch because it's programmable. Also, by eliminating a hardware switch, this router is a lower-power and lower-cost solution.

What's more, this basic design is highly scalable, because NXP offers larger (and smaller) QorIQ processors that have similar features. For example, a higher-end design could replace the quad-core LS1043A with the LS1088A, which has eight Cortex-A53 cores, second-generation DPAA2 acceleration, two 10GbE ports, eight GbE ports, and a 64-bit DRAM interface. This processor delivers twice the CPU performance and four times the packet throughput of the LS1043A for about twice the power consumption (10W typical). Thus an OEM could offer a broad product line that scales from home gateways to small-business access points to enterprise branch-office routers-all running essentially the same portable software. And ODP helps developers port VMs and VNFs from different vendors, thereby avoiding vendor lock-in.

Figure 4 shows how SDN and NFV enable virtualization throughout the whole network.

Almost any network function can be virtualized; the main limitation is performance and power. If the network functions were implemented using general-purpose embedded processors, throughput would indeed suffer-so badly, in some cases, that virtualization would be impractical. Also, power consumption would be higher.

Performing low-level tasks in hardware is generally more power efficient than doingeverything in software. By offloading those tasks from the CPUs to the accelerationengines, SDN and NFV can compete with special-purpose networking hardware.

Because multipurpose hardware is programmable using industry-standard softwaredevelopment tools and open APIs, operators can more easily customize their software, deliver new services, and thoroughly test their code on VMs under real-world conditions before deployment.

Designing for Tomorrow

The simple fact is that networks must become more configurable and scalable to keep pace with the rapid growth of network traffic and the pressure on operator revenues.

They must embrace open standards to ease software development and achieve compatibility on hardware from multiple vendors. They must enable the rapid rollout of new services to stay competitive and generate new revenue streams. And they must become more secure to be reliable platforms for e-commerce and business communications.

How Project Tango Will Change the Way You Use Your Phone

Vice President and General Manager, Tablets, Lenovo

We're getting excited. Project Tango is getting ready for its close-up, and we're working closely with Google to create the first consumer mobile device enabled with Project Tango. This summer, you'll see us announce a new Project Tango-enabled smartphone that gives users a magic lens to experience the world in a new way.

But first, you have to know What is Project Tango? And what can it truly do for you?

At its essence, Project Tango gives your mobile device the ability to navigate the physical world, similarly to how we do as humans. We see three important usage scenarios for Project Tango: location and navigation, gaming, and utility. Today, we're going to show youtwo new apps that put location and navigation abilities in action. With mobile technology taking a focus this week at Mobile World Congress in Barcelona, we've teamed up with Google to show the magic a Project Tango-enable phone can bring to your everyday life by two apps made by GuidiGO and Glympse.

A New, Interactive Way to Go and Glympse into History

Whether you're discovering Barcelona's jewels for the first time or just reveling in the city's magic, GuidiGO's Project Tango app brings its stories to life in a totally new, immersive way – on your mobile device. To see the power of this app in action, let's go to the Museu Nacional d'Art de Catalunya in Barcelona. It uses Project Tango's augmented reality features to create your own personal tour guide – even showing you hidden details invisible to the naked eye. Simply hold up your phone, choose a work of art, and follow the directions superimposed on the floor, as if a real person were guiding you up to it. Once you are at the painting, hold up your phone and see virtual annotations on the painting that unlock new information about the painting.

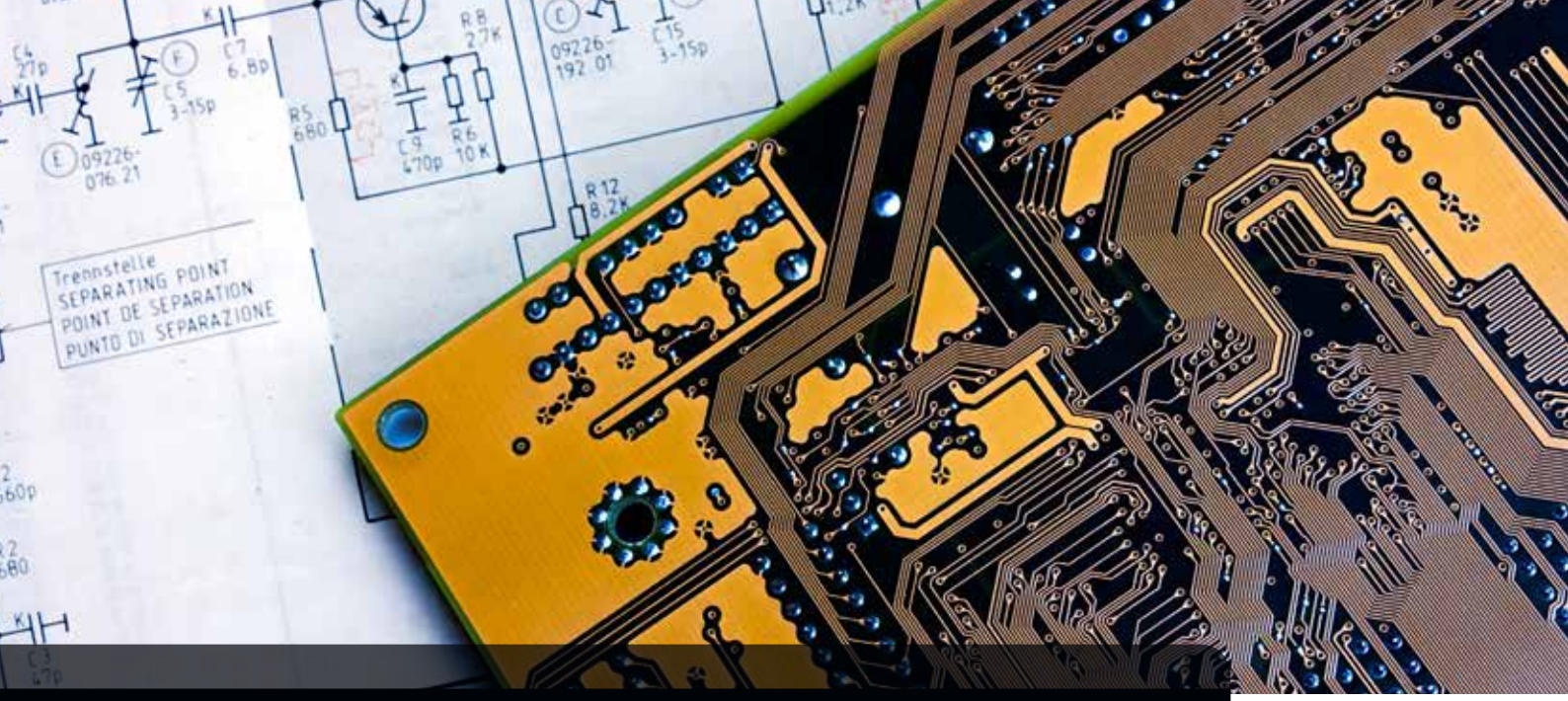
Now Glympse, the leader in real-time location sharing technology, makes it even easier to share your location with the people you care about. Using Project Tango's AR technology, Glympse is enhancing its indoor capabilities. Users who share their location with each other can now see through walls, floors and

other obstructions to find each other in places like a museum. Simply hold up your Project Tango phone, and you'll see who's sharing their location with you — a quick and easy way to answer the question, "Where are you?"

Here's a step-by-step on how it works:

Picture yourself in a room of an art museum. You're holding a smartphone loaded with the GuidiGO app – the app displays a map of the interior of the art museum with the specific paintings listed out. You're interested in one of the paintings on the map, so you click on that painting to get more information and directions to it. You're presented with the camera view of the room through your phone's screen – except it's actually a window into an augmented world with blue directional dots overlaid on the ground having formed the path leading to the painting you just picked. Once you arrive, GuidiGO marker pops up on your screen letting you know you made it, and you're presented with video content and virtual annotations about the piece.

In the coming months, we'll bring you stories of partners working with us to make this future a reality and show you the potential of some our gaming and utility apps and features. We're now working with thousands of third party developers to build killer apps for each of its three pillars and to populate and enrich the Project Tango app ecosystem.



3D Printing PCBS

› by Simon Fried, Nano-Dimensions

For anyone familiar with 3D printing and printed circuit boards (PCBs) it's difficult to imagine a future where PCBs are not 3D printed. 3D printing promises to make PCB manufacturing faster, easier and more innovative. It is only recently however that Printed Electronics and 3D printing technology has started to catch up with imagination.

First a brief introduction to the world of 3D printing, or as it's more properly known 'additive manufacturing'. Nowadays it comprises a range of different competing processes that use heat, lasers, inkjet deposition or other techniques to add different materials, layer by layer, to build new or to add to existing objects. Each process has advantages and disadvantages in terms of precision, materials, end-product durability and flexibility in terms of the objects and shapes that can be supported. As a rule there is a correlation between price, resolution and range of supported materials.

Developing Materials for Electronics

To 3D print PCBs the systems have to be able to print conductive traces, which is the domain of Printed Electronics. This is an advanced technological area which involves the development of conductive materials suited to a range of different substrates. Basic connections can be embedded in objects by 3D extrusion printers using conductive filaments. These contain conductive polymers, carbon nano-tubes or other conductive materials. However, the end result, using current technologies, is a low resolution, point-to-point conductive trace that struggles to cope with the electrical requirements of professional circuits.

For higher resolution and acceptable conductivity, more advanced printing solutions are required. The nano-ink industry is currently providing formulations to meet this challenge in the form of various silver nanoparticle inks. These inks are suspensions of nanometer sized silver particles that, after printing, need to be cured either chemically, by light or by heat. Once cured, the particles coalesce to form a conductive solid silver trace. The technology is now developed enough that silver nanoparticles are emerging as a mature technological solution to printing electronics. That is not to say that all silver nanoparticle inks are the same, nano-ink development itself is a very advanced field. Silver may be an expensive metal to use but given that traces are so fine not much is needed. The performance justifies the cost.

Copper ink would be clearly preferable from a cost perspective but copper ink is not currently a mature enough technology. Copper is much harder to print with as oxidation issues mean that the ink isn't as easy to make or use and the end results are not robust. Carbon nano-tubes and other exotic

materials may well offer alternatives in the future also.

3D Printing Professional Multi-Layer PCBs

On one hand PCBs are multilayered which implies they are well suited to additive manufacturing. On the other hand the multiple materials, conductivity requirements and exacting precision present serious technological challenges.

To rise to the challenge of making proper multilayer PCBs the conductive traces clearly have to be printed in such a way that they are precise enough, conductive enough and robust enough to do the job reliably. Inkjet deposition is likely to be the first true

3D printing process to provide this technology for professional multilayered PCBs.

Having solved the printing of advanced inks to give precise conductive traces the next step in order to 3D print a PCB is to print the substrate. For traditional rigid boards the substrate ink material needs to be inkjet printable, e an excellent insulator and offer rigidity that is comparable to standard FR4. Flexible boards are another field and require a different combination of substrate and conductive ink formulations. Each substrate requires its own ink specifications to ensure adhesion, precision and compatibility with the relevant ink curing stage.

If nano-materials can be engineered to meet the requirements of a PCB the next challenge is how to manage the printer. The software has to be able to process Gerber files which are intended for a 2D manufacturing environment. This would allow the 3D printer to print the substrate to the required thickness, to leave and fill holes where vias are required and so on.

The only company currently dedicated to 3D printing professional multilayer rigid PCBs is Nano Dimension. The company, which is listed on the Nasdaq and Tel Aviv stock exchange (NNDM), is developing a 3D inkjet printer that will offer in-house rapid-prototyping of professional multilayer PCBs to be printed in-house. To this end the company has formulated and makes its own nano-inks. To make a multi-layer PCB Nano Dimension's printer will print a proprietary silver nano-particle ink for the conductive trace and another proprietary nano particle dielectric ink for the insulating layer. The company promises a trace width of 3-4 Mil.

It is early days for the 3D electronics revolution but it's clearly coming. If all of these elements; 3D printer, inks and software come together then there is no reason that PCBs shouldn't be 3D printed. 3D printing can lead to dramatically faster in-house development, protect IP in development, reduce waste and even inject more design innovation and creativity with PCBs that can not be produced in any other way.

For prototypes and very small-batches, 3D printing may be just around the corner. First printers will deliver in-house prototyping solutions that change the way products are developed however, as is the case in other industries it is unlikely that 3D printers will replace efficient mass-production processes anytime soon. Whether 3D printing completely replaces traditional manufacturing processes remains to be seen. There are those that dream of a 3D printer that can print multi-material objects with completely embedded HD circuits and no traditional PCB at all

AMP up Your Next SoC Project

Harness real-time performance and the rich features of Linux

› Scott McNutt, Senior Software Engineer

Embedded systems usually fall into one of two categories: those that require hard real-time performance and those that don't. In the past, we had to pick our poison-the performance of our "go to" real-time operating system or the rich feature set of our favorite Linux distribution-and then struggle with its shortcomings.

Today, embedded developers no longer need to choose between the two. Asymmetric multiprocessing (AMP) offers the best of both worlds. Several modern system-on-chip (SoC) product offerings integrate multiple CPUs, a broad variety of standard I/O peripherals and programmable logic. The Xilinx® Zynq-7000® All Programmable SoC family, for example, includes a dual-core ARM® Cortex™-A9, standard peripherals (such as Gigabit Ethernet MACs, USB, DMA, SD/MMC, SPI and CAN) and a large programmable logic array.

We can use these SoC products as the basis of a Linux/RTOS AMP system that provides considerable flexibility. In many ways, the typical AMP configuration is similar to a PCI-based system, with the Linux domain functioning as the host, the RTOS domain functioning as an adapter, and one or more shared memory regions used for communication between the two domains.

Unlike PCI, however, an AMP configuration can more conveniently-and dynamically-assign resources (both the standard peripherals and custom logic) to one domain or the other. In addition, a Linux/RTOS AMP system can dynamically reconfigure programmable logic based on runtime requirements, such as the presence or absence of various external devices.

This level of flexibility is often coupled with concerns about complexity and the degree of difficulty involved in bringing up an AMP system. Rest assured that the Linux development community has introduced many features into the kernel that greatly simplify AMP configuration and use.

LINUX MULTIPROCESSING IN A NUTSHELL

With respect to multiprocessing, the Linux kernel comes in two flavors: the uniprocessor (UP) kernel and the symmetric multiprocessor (SMP) kernel. The UP kernel can only run on a single core, regardless of the number of available cores. AMP systems can incorporate two or more instances of the uniprocessor kernel.

The SMP kernel, however, can run on one core or simultaneously on multiple cores (Figure 1). An optional kernel command line parameter controls the number of cores used by the SMP kernel following system initialization. Once the kernel is running, various command line utilities control the number of cores assigned to the

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	ZHL-5W-422+	500-4200	25	3	5	1670
	ZHL-5W-2G+	800-2000	45	5	5	995
	ZHL-10W-2G+	800-2000	43	10	12	1295
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•	ZHL-20W-13SW+	20-1000	50	13	20	1445
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•	ZHL-100W-52+	50-500	50	63	79	1995
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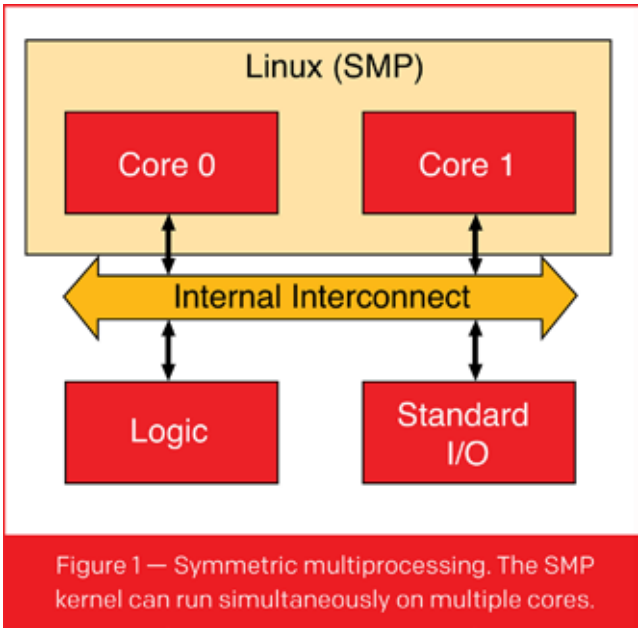


Figure 1 — Symmetric multiprocessing. The SMP kernel can run simultaneously on multiple cores.

Figure 1. Symmetric multiprocessing. The SMP kernel can run simultaneously on multiple cores.

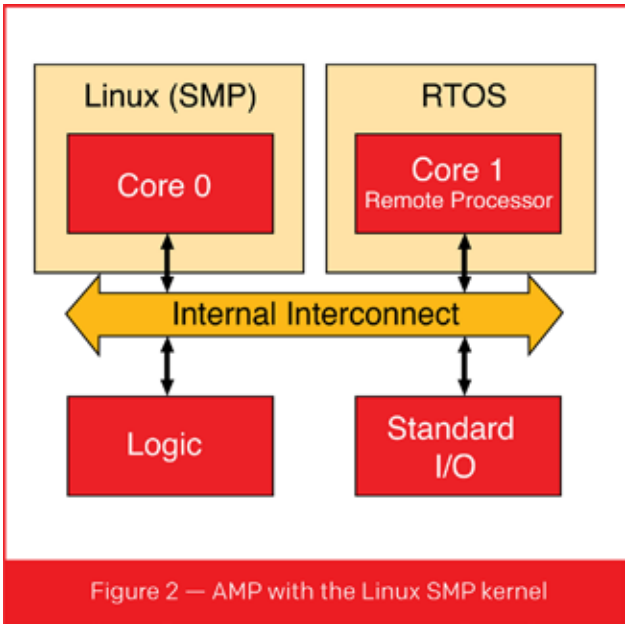


Figure 2 — AMP with the Linux SMP kernel

Figure 2. AMP with the Linux SMP kernel

kernel. The ability to dynamically control the number of cores used by the kernel is a primary reason AMP developers prefer the SMP kernel over the UP kernel.

The Remote Processor Framework

The Remote Processor (remoteproc) Framework is the Linux component that is responsible for starting and stopping individual cores (remote processors), as well as for loading a core's software in an AMP system. For example, we can dynamically reconfigure the SMP system shown in Figure 1 into the AMP system shown in Figure 2, and then back again to SMP, using the capabilities of remoteproc.

We can fully control reconfiguration via a user-space application or system initialization script. This allows user applications to stop, reload and run a variety of RTOS applications based on the dynamic needs of the system.

The core's software (in our example, the RTOS and user application) is loaded from a standard Executable and Linkable Format (ELF) file that contains a special section known as the resource table. The resource table is analogous to the PCI configuration space in that it describes the resources that the RTOS requires. Among those resources is the memory needed for the RTOS code and data.

Trace buffers

Trace buffers are regions of memory that automatically appear as files in a Linux file system. As their name suggests, trace buffers provide basic tracing capabilities to the remote processor. A remote processor writes trace, debug and status messages to the buffers, where the messages are available for inspection via the Linux command line or by custom applications.

One or more trace buffers may be requested via entries in the resource table. Although they typically contain plain text, trace buffers may also contain binary data such as application state information or alarm indications.

Virtual I/O devices

The resource table also supports the definition virtual input/output devices (VDEVs), which are basically pairs of shared memory queues that support message transfer between the Linux kernel and the remote processor. The VDEV definition includes fields that negotiate the size of the queues as well as the interrupts used to signal between the processors.

The Linux kernel handles initialization of the virtual I/O queues. The software running on a remote processor need only include a VDEV description in its resource table and then use the queues once it begins execution; the kernel handles the rest.

Remote Processor Messaging Framework

The Remote Processor Messaging (rpmsg) Framework is a messaging "bus" based on the Linux kernel's virtual I/O system. The messaging bus is similar to a local area subnetwork in which individual processors can create addressable endpoints and exchange messages, all via shared memory.

The kernel's rpmsg framework acts as a switch, routing messages to the appropriate endpoint based on the destination address contained in the message. Because the message header includes a source address, ad hoc connections can be established

between various processors.

Naming service

Processors can dynamically announce a particular service by sending a message to the rpmsg framework's naming service. By itself, the naming service feature is only marginally useful. The rpmsg framework, however, allows service names to be bound to device drivers to support the automatic loading and initialization of specific drivers. For example, if a remote processor announces the service dlinx-h323-v1.0, the kernel can search for, load and initialize the driver bound to that name. This greatly simplifies driver management in systems where services are dynamically installed on remote processors.

Managing interrupts

Interrupt management can be a little tricky, especially when starting and stopping cores. Ultimately, the system needs to redirect specific interrupts dynamically to the remote processor domain when the remote processor is started, then reclaim those interrupts when the remote processor is stopped. In addition, the system must protect the interrupts from inadvertent allocation by potentially misconfigured drivers. In short, interrupts must be managed systemwide.

For the Linux SMP kernel, this is a routine matter—and a further reason that the SMP kernel is preferred in AMP configurations. The remote processor framework conveniently manages interrupts with only minimal support from the device driver.

Device drivers

Device driver development is always a concern because it requires a skill set that may not be readily available. Fortunately, the Linux kernel's remoteproc and rpmsg frameworks do most of the heavy lifting; drivers need only implement a handful of standard driver routines. A fully functional driver may only require a few hundred lines of code. The kernel source tree includes sample drivers that embedded developers can adapt to their requirements.

Generic open-source device drivers are also available from vendors. DesignLinx Hardware Solutions provides generic rpmsg drivers for both Linux and FreeRTOS. Since the generic driver makes no assumptions about the format of the messages that are exchanged, embedded developers can use it for a variety of AMP applications without any modifications.

MOVING INSIDE THE PINS

The kernel's multiprocessing support is not limited to homogeneous multiprocessing systems (systems using only the same kind of processor). All of the features described above can also be used in heterogeneous systems (systems with different kinds of processors). These multiprocessing features are especially useful when migrating existing designs "inside the pins."

Modern SoC products let designers conveniently move various hardware designs from a printed-circuit board to a system-on-chip (Figure 3). What was once implemented as a collection of discrete processors and components on a PCB can be implemented entirely inside the pins of an SoC.

For example, we can implement the original PCB hardware architecture of Figure 3 with a Xilinx Zynq-7000 family SoC using one of the ARM processors as the control CPU and soft processors (such as Xilinx MicroBlaze™ processors) in the programmable logic to replace the discrete microprocessors. We can use the remaining ARM processor to run the Linux SMP kernel (Figure 4).

The addition of Linux to the original design provides all of the standard multiprocessing features described above for both the ARM cores and the soft core processors (such as start, stop, reload, trace buffers and remote messaging). But it also brings the broad Linux feature set, which supports a variety of network interfaces (Ethernet, Wi-Fi, Bluetooth), networking services (Web servers, FTP, SSH, SNMP), file systems (DOS, NFS, cramfs, flash memory) and other interfaces (PCIe, SPI, USB, MMC, video), to name just a few. These features offer a convenient pathway to new capabilities without significantly altering tried-and-true architectures.

THE CORES KEEP COMING

The past several years have seen an increase in multicore SoC offerings that target the embedded market and are well suited for AMP configurations. The Xilinx UltraScale+™ MPSoC architecture, for example, includes a 64-bit quad-core ARM Cortex-A53, a 32-bit dual-core ARM Cortex-R5, a graphics processing unit (GPU) and a host of other peripherals—and, of course, a healthy helping of programmable logic. This is fertile ground for designers who understand how to harness the performance of real-time operating systems coupled with the rich feature set of the Linux kernel.

For more information on designing a Linux/RTOS AMP system, contact DesignLinx Hardware Solutions. A premier member of the Xilinx Alliance Program, DesignLinx specializes in FPGA design and support, including systems design, schematic capture and electronic packaging/mechanical engineering design, and signal integrity.

DJI Introduces Next-Generation Matrice 600 Aerial Platform

DJI introduced the Matrice 600, its next-generation aerial platform, marking a new era for professional aerial photography, filmmaking and industrial applications.

The M600 integrates DJI's brand-new A3 flight controller onboard and features advanced Lightbridge 2 video-transmission technology that offers high frame rates and HD live-streaming capability at distances up to five kilometers.

The M600 is a six-rotor system with a maximum payload of 6.0 kilograms, making it ideal for the full range of DJI's Zenmuse gimbals, including the Z15 series and the Zenmuse X series cameras, which are unmatched in providing stabilized aerial imagery. The M600's carrying weight also allows it to fly the Ronin MX, DJI's newest handheld and aerial three-axis gimbal. The M600's propulsion system is dustproof to simplify maintenance and increase durability. It has actively cooled motors for more-reliable flight, and its landing gear is retractable for full 360-degree, unobstructed imaging.

The M600 is powered by six DJI Intelligent Batteries. The customized battery-management system and power distribution board allow all six batteries to be turned on and off with the push of one button and keep the system aloft, should a single battery fail. The M600 will fly up to 36 minutes with a Zenmuse X5 camera attached and up to 16 minutes with a larger camera, such as a RED EPIC. Flight time will vary for different cameras, gimbals and a number of other conditions.

Integrated A3 Flight Controller

Setting the M600 apart is its integrated A3 flight controller. It uses sine-wave-driven, intelligent electronic speed controllers to ensure the M600 performs accurately, safely and efficiently. Meanwhile, self-adaptive flight systems adjust parameters automatically, based on different payloads.

It's upgradable to the A3 PRO system, which features advanced diagnostic algorithms that compare sensor data from three Global Navigation Satellite System (GNSS) units and three inertial measurement units.

The A3's GNSS system can also be optionally upgraded to DJI Real-Time Kinematic technology, offering centimeter-accurate positioning to allow for complex maneuvers in an industrial setting and so that cinematic shots can be precisely replicated. The RTK technology can also withstand magnetic interference.

The M600 supports the DJI GO app, which includes a live video feed, battery and redundancy status, transmission strength and other data to keep the user informed of flight status at all times. The app also provides access to aperture, shutter speed, photo and video capture on any Zenmuse X-series camera, plus remote focus on the Zenmuse X5 and X5R cameras.

The M600 is a top-quality development platform,

compatible with the DJI Onboard Software Development Kit and Mobile SDK to work with different industrial applications. It has dual parallel CAN and API ports for connecting DJI devices, including the Guidance sensor system, RTK GPS units or third-party components.

The M600's retail price, including the integrated A3 flight controller with Lightbridge 2 and a full set of batteries, is $4,599.

Works Seamlessly with Ronin-MX

When paired with the new DJI Ronin-MX, the M600 offers best-in-class three-axis aerial video stabilization. The latest in the Ronin line is also the most-versatile, working both on the ground and in the air with minimal setup.

The Ronin-MX works perfectly with the M600, as a fully integrated system that includes the A3 flight controller, Lightbridge 2 transmission system and gimbal in the air. It's the first universal aerial gimbal DJI has made that communicates with the onboard DJI flight controller.

It's fully compatible with a rich selection of DJI accessories for long-distance focus and aperture control and features remote start/stop controls and video transmission. The Ronin-MX is built for convenient, handheld use, but it also has multiple operation modes, including underslung, upright and briefcase. Apart from the M600, it's also compatible with video cranes.

The Ronin-MX has a built-in, independent IMU module, a Bluetooth module and a 2.4GHz receiver. It operates through the DJI GO app and has settings for SmoothTrack and gimbal-tuning for various cameras, including some of the RED series, DSLRs and other professional camera. It also operates in multiple modes, including aerial and car mount.

Mounted on the M600, the Ronin-MX's CANBUS port allows all flight controller data to pass through to the Ronin-MX, meaning the gimbal is positionally aware and able to keep the horizon level. The Ronin-MX can pan 360 degrees, tilt +45 to -135 degrees and has redundant slip rings, offering enhanced reliability for operators. With an optional accessory, the Ronin-MX can transmit video real-time from a mounted camera, making full use of the M600's Lightbridge 2 capabilities. It will also be compatible with the DJI Focus, through a wireless adapter mounted to the Focus remote.

The Ronin-MX is powered by a 4S Ronin-M battery. Third-party cameras mounted on the Ronin MX can be powered by an optional onboard DJI battery.

The Ronin MX is compatible with a wide range of cameras from Arri, Black Magic, Canon, Panasonic, RED, Sony and Nikon. Its maximum load weight is around 4.5 kilograms.

The Ronin MX retails for $1,599. Bundled with the M600 and integrated A3 flight controller and Lightbridge 2, it will sell for $5,999.

http://www.dji.com/newsroom/news/dji-introduces-next-generation-matrice-600-aerial-platform

1.5A Synchronous Step-Down DC/DC Converter Delivers 93% Efficiency at 2MHz & Operates from 3.0V to 42V Inputs

Linear Technology Corporation announces the LT8608, a 1.5A, 42V input synchronous step-down switching regulator. A unique synchronous rectification topology delivers 93% efficiency while switching at 2MHz enabling designers to avoid critical noise-sensitive frequency bands, such as AM radio, while using a very compact solution footprint. Burst Mode® operation keeps quiescent current under 2.5µA in no-load standby conditions making it ideal for always-on systems. Its 3.0V to 42V input voltage range makes it ideal for automotive applications which must regulate through cold-crank and stop-start scenarios with minimum input voltages as low as 3.0V and load dump transients in excess of 40V. Its internal 2A switches can deliver up to 1.5A of continuous output current. The LT8608 maintains a minimum dropout voltage of only 200mV (@500mA) under all conditions, enabling it to excel in scenarios such as automotive cold-crank. Spread spectrum frequency modulation and special design techniques offer low EMI operation to minimize noise concerns in automotive and industrial environments. Furthermore, a fast minimum on-time of only 45ns enables 2MHz constant frequency switching from a 16V input to a 1.5V output. The LT8608's 10-lead thermally enhanced MSOP package and high switching frequency keeps external inductors and capacitors small, providing a compact, thermally efficient footprint.

The LT8608 utilizes internal top and bottom high efficiency power switches with the necessary boost diode, oscillator, control and logic circuitry integrated into a single die. Low ripple Burst Mode operation maintains high efficiency at low output currents while keeping output ripple below 10mVP-P. Unique design techniques and a new high speed process enable high efficiency over a wide input voltage range, and the LT8608's current mode topology enables fast transient response and excellent loop stability. Other features include internal compensation, a power good flag, output soft-start/tracking and thermal protection.

The LT8608EMSE is packaged in thermally enhanced MSOP-10 package. An industrial temperature version, the LT8608IMSE is tested and guaranteed to operate from a -40°C to 125°C operating junction temperature. Pricing starts at $2.25 each in 1,000-piece quantities and both versions are available from stock. For more information, visit www.linear.com/product/LT8608.

Epson Begins Shipping Samples of Low-Power, 16-bit Microcontrollers with High-Performance LCD Drivers

High-capacity, high-resolution models ideal for feature-rich watches –

Seiko Epson Corporation (TSE: 6724, "Epson") has developed and recently begun shipping samples of three new models in the company's S1C17W series of low-power 16-bit microcontrollers with on-chip Flash memory. The new models are the S1C17W34, S1C17W35, and S1C17W36. Epson plans to produce 200,000 units per month of each model when volume production beings in October 2016.

Epson's original 16-bit microcontrollers with built-in Flash memory have proved to be a popular choice for embedding in mobile devices owing to their exceptionally low power consumption. The S1C17W series, which entered volume production in 2013, has been especially popular for use in digital watches because of low power consumption and liquid crystal driving capability.

Digital watches have been gaining an increasing number of features and functions in recent years. In addition to sensors for tracking activity and measuring things such as temperature, and altitude, many timepieces have also added GPS, Bluetooth® and other wireless features, so the amount of data processed by the microcontroller has steadily grown. The need for more on-chip microcontroller memory has increased commensurately. Also, since more watches now need to display more information, their LCD screens tend to be larger and have higher definition. These screens require high-resolution liquid crystal drivers.

The S1C17W36 meets these needs with 384 Kbytes of on-chip Flash memory, the most in the series, and an integrated liquid crystal driver

that drives up to 2,084 dots. The low voltage and low current operation of the microcontrollers makes them ideally suited to customers who develop watches that are not designed to be recharged by users. Since the integrated liquid crystal drivers are capable of driving LCDs with resolutions as high as 2,048 dots, displays can render crisp characters, graphs, and other graphics. The microcontroller has a built-in real-time clock that is capable of instantly calling up and displaying the time in cities in three different time zones. This feature has the benefit of lightening the load on the CPU and reducing program size. In addition to shipping in a 176-pin plastic package (QFP21-176), the microcontrollers will also be available as bare die to help users reduce the board area within their finished products.

The new microcontrollers provide customers with Flash memory size options. In addition to the S1C17W36, which has 384 Kbytes of memory, customers can choose the S1C17W34, which as 128 Kbytes of memory, or the S1C17W35, which has 256 Kbytes, depending on size requirements of control programs. In addition, the three new models are drop-in compatible and can be swapped for one another without any special settings. This interchangeability gives customers the flexibility to upgrade to a microcontroller with more Flash memory when, for example, the customer wants to add additional control programs.

The Bluetooth word mark and logo are registered trademarks of the Bluetooth SIG, Inc.

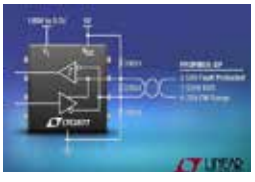
Seiko Epson Corporation has licensed the use of these trademarks.

Robust ±60V RS485 Transceivers Fortify PROFIBUS-DP Networks

Linear Technology Corporation introduces the LTC2876 and LTC2877, exceptionally rugged, high voltage tolerant RS485 transceivers targeted for PROFIBUS-DP (decentralized periphery) master and slave devices. As with any fieldbus, PROFIBUS-DP systems are prone to installation cross-wiring faults, ground voltage faults, or surge, which can cause catastrophic overvoltage conditions that exceed the absolute maximum ratings of typical transceivers. Whether transmitting, receiving, in standby or powered off, the LTC2876 and LTC2877 tolerate ±60V on their bus pins, eliminating common damage due to transmission line faults.

The LTC2876 and LTC2877 provide multiple levels of protection that make them suitable for a variety of PROFIBUS-DP applications, including discrete manufacturing and process automation. An extended ±25V input common-mode range and full failsafe operation improve data communications reliability in electrically noisy environments and in the presence of ground loop voltages, which would otherwise cause data errors and possible device damage. Their incredibly high ESD protection guarantees the LTC2876 and LTC2877 can withstand ±52kV HBM on the transceiver pins without latchup or damage; all other pins are protected to ±15kV HBM. Fully symmetric receiver thresholds ensure the devices maintain good duty cycle symmetry at low signal levels and boost receiver noise immunity, while supporting full failsafe operation. Both devices are tested with PROFIBUS IEC 61158-2 and TIA/EIA-485-A (RS485) loads to ensure compatability with both standards.

The LTC2876 and LTC2877 are offered in commercial, industrial and automotive versions, supporting operating temperature ranges of 0°C to 70°C, -40°C to 85°C, and -40°C to 125°C, respectively. The LTC2876 is available in an RoHS compliant 8-pin 3mm x 3mm DFN or MSOP package, while the LTC2877 includes a logic supply and is available in an RoHS compliant 10-pin 3mm x 3mm DFN or MSOP package. Pricing starts at $2.48 each in 1,000 piece quantities. Please visit www.linear.com/product/LTC2876 for more product selection and information.



New Vishay Intertechnology Thick Film, Multi-Resistance-Value Chip Resistor Arrays Supplement Thin Film Arrays

Providing an alternative to thin film arrays in applications requiring lower performance, Vishay Intertechnology, Inc. (NYSE: VSH) today introduced the industry's first thick film chip resistor arrays to offer multiple resistance values in one device. Allowing

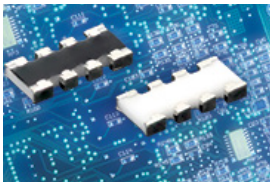
designers to lower pick-and-place costs and save board space in automotive and industrial applications, the AEC-Q200-qualified devices are available with two resistors of different values in the 0606 case size (CRAS0606), or two pairs of resistors with different values in the 0612 case size (CRAS0612 and CRAE0612).

With resistance from 10 Ω to 1 MΩ, resistance tolerance of ± 1 % and ± 5 %, and TCR of ± 100 ppm/K and ± 200 ppm/K, the Vishay Draloric resistor arrays released today are to be used as voltage dividers, operational amplifier feedback circuits, and DC/DC converter output voltage sensing.

The convex terminal arrays are available with square corners (version S) or scalloped corners (version E). RoHS-compliant and halogen-free, theCRAS0606, CRAS0612, and CRAE0612 feature a 50 V operating voltage, power dissipation of 0.063 W per element at +70 °C, and operate over a temperature range of -55 °C to +155 °C.

Samples and production quantities of the thick film, multi-resistance-value resistor arrays are available now, with lead times of 10 weeks.

Vishay Intertechnology, Inc., a Fortune 1000 Company listed on the NYSE (VSH), is one of the world's largest manufacturers of discrete semiconductors (diodes, MOSFETs, and infrared optoelectronics) and passive electronic components (resistors, inductors, and capacitors). These components are used in virtually all types of electronic devices and equipment, in the industrial, computing, automotive, consumer, telecommunications, military, aerospace, power supplies, and medical markets. Vishay's product innovations, successful acquisition strategy, and "one-stop shop" service have made it a global industry leader. Vishay can be found on the Internet at www.vishay.com.



Vishay Intertechnology Releases AEC-Q101-Qualified Tall Dome Transmissive Optical Sensors for Automotive and Industrial Applications

Vishay Intertechnology, Inc. (NYSE: VSH) today introduced two new AEC-Q101-qualified surface-mount transmissive optical sensors for automotive and industrial applications. Offered in a compact 5.5 mm by 4 mm by 5.7 mm package, the Vishay Semiconductors single-channel TCPT1600X01 and dual-channel TCUT1600X01 feature an increased dome height compared with previous-generation devices.

Thanks to their tall dome design, the devices released today offer more vertical headroom for the code wheel in turn-and-push applications. They can be used as position sensors for encoders in high-temperature environments close to motors, in addition to turn knobs, ignition locks, and adaptive headlights. Both sensors can detect motion and speed. With dual channels, the TCUT1600X01 can also be used to detect direction in applications such as electronic power steering (ESP) systems.

The single-channel TCPT1600X01 includes an infrared emitter and phototransistor detector located face-to-face in a surface-mount package, while the dual-channel TCUT1600X01 includes an infrared emitter and two phototransistor detectors. Both sensors deliver a typical output current of 1.6 mA and operate at a wavelength of 950 nm. The devices feature a 3 mm gap width and apertures of 0.3 mm, and they operate over a wide temperature range of -40 °C to +105 °C.

With a Moisture Sensitivity Level rating of 1 (MSL1), the TCPT1600X01 and TCUT1600X01 have an unlimited floor life. Compatible with reflow solder processes according to JEDEC-STD-020D, the devices are halogen-free, RoHS-compliant, and Vishay Green.

Samples and production quantities of the optical sensors are available now, with lead times of eight to 10 weeks for larger orders.

Resources:

Transmissive optical sensors from Vishay

Check TCPT1600X01 distributor stock on the Vishay website.

Check TCUT1600X01 distributor stock on the Vishay website.

Weekly updates: Sign up for Vishay Newsfeed.

Renesas Electronics Delivers RH850/E1M-S2 32-Bit MCUs for Improved Automobile Fuel Efficiency in Vehicle Powertrain Control Applications

Enables Enhanced Fuel Efficiency

to Meet Strict Environmental Regulations

Renesas Electronics Corporation (TSE: 6723), a premier supplier of advanced semiconductor solutions, today announced the 32-bit RH850/E1M-S2 microcontrollers (MCUs) for automotive powertrain control applications, such as engine or transmission control, that provide high performance and advanced functionality to enable improved fuel efficiency. The RH850/E1M-S2 MCUs include four product versions, including the most high-end R7F701216EABA (BGA304, 320MHz).

In recent years, regulations covering automobile fuel efficiency and CO2 emissions have become increasingly strict. Some current regulations(Note 1) stipulate that CO2 emissions must be reduced by 10 percent from their current level by 2018. To meet these targets, engine control systems must optimize the ignition and fuel injection timing to match a variety of conditions, such as current combustion and driving status. Transmission control systems, for their part, must instantly select the optimal gear ratio to match the driving conditions, which change moment by moment, in order to minimize power loss in the transmission.

The new RH850/E1M-S2 MCUs bring more precise control to powertrain control systems by boosting processing performance to accommodate the increasing number of calculations required. At the same time, the RH850/E1M-S2 MCUs boost network performance to match the larger volume of control data resulting from the use of more sensors and provides stronger security functionality to prevent unauthorized access to control systems.

Key features of the new RH850/E1M-S2:

(1) Newly developed high-performance G3MH CPU core to help boost fuel efficiency

The RH850/E1M-S2 MCUs are built around Renesas' new and improved G3MH CPU core. The G3MH core has improved access latency towards memory and peripheral functions while retaining an industry-leading operating frequency of 320 MHz at Tj (Note 2) = 150°C. This results in an improved engine control system responsiveness of approximately 30 percent (Note 3) compared with earlier Renesas products.

(2) High-speed network functionality to accommodate the use of more sensors and communication with other vehicle control units

The RH850/E1M-S2 MCUs support the Single Edge Nibble Transmission (SENT, Note 4) digital communication standard for sensors and CAN FD (Note 5), which accommodates the increase in the volume of data from the increasing number of sensors and the need for high-speed data transfer to other vehicle control units respectively.

a) Support for SENT communication standard for sensor data

The number of sensors used in automobiles to provide information on the vehicle or environment status is growing rapidly, and these sensors are becoming more sophisticated. The new RH850/E1M-S2 MCUs are equipped with six Renesas SENT (RSENT) channels compliant with the SENT communication standard for sensor data. This enables the MCUs to handle communication of digitized data from approximately 50 sensors. Since a single signal line can be used for multiple sensors, it can contribute to overall weight reduction of the wiring harnesses as well.

b) Support for CAN FD high-speed communication

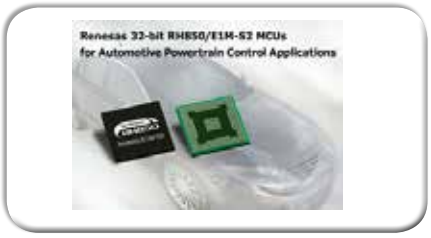
Intended as a next-generation automotive CAN communication standard, the CAN FD accelerates the maximum throughput. It also supports a mode allowing connection to CAN buses using the earlier standard.

(3) Enhanced security functionality

for greater robustness

To protect engine and transmission systems from unauthorized access and ensure safe control, the RH850/E1M-S2 MCUs are equipped with an Intelligent Cryptographic Unit—Slave (ICU-S) hardware security module that complies with the SHE/EVITA-Light (Note 6) standard for automotive security. It provides functions such as data encryption like Cypher Message Authentication (CMAC) and random number generation.

The new RH850/E1M-S2 MCUs are supported with a code generator tool that automatically produces C source code for drivers, based on settings entered via a Graphical User Interface (GUI), making it easier for system manufacturers to develop applications. In addition, model-based design development is supported in collaboration with Renesas partner vendors. This contributes to shorter development cycles, even though the Electronic Control Units (ECUs) used in automobiles become more complex.



Microchip's MOST150 Technology with Proven, Automotive-Ready, In-Car Ethernet

Microchip Technology Inc. (NASDAQ: MCHP), a leading provider of microcontroller, mixed-signal, analog and Flash-IP solutions, today announced that MOST150 technology has been implemented in the new Volvo V90. Volvo Cars has been utilizing Microchip's technology for many years and recently began utilizing MOST150, the latest MOST® technology from Microchip. MOST150 is the first standard to provide a proven, automotive-ready physical layer for Ethernet packet transport inside vehicles in accordance with the IEEE 802.3 Ethernet specifications. This is the third Volvo model where its infotainment system includes MOST150 technology.

"We are very pleased to see that Volvo Cars relies on the MOST150 technology in the new V90, just a couple of months after the release of the new S90 and XC90 with MOST150 technology," said Dan Termer, Microchip's automotive vice president. "Volvo Cars' continuous roll out of the latest MOST150 technology shows that this technology provides a reliable network platform for automotive infotainment systems."

MOST150 technology continues to meet Volvo Cars' high standards. When implemented, the technology reduces vehicle weight and offers high bandwidth communication. In addition, it creates a robust physical layer and proven EMC behavior. This latest version of MOST technology can transport video, audio, packet and control data with zero processor overhead and offers dedicated application-specific hardware interfaces to simplify data communication. In addition, the MOST technology networked infotainment system features ultra-fast system startup behavior to support early audio applications.

The MOST Cooperation standards enable automotive OEMs and their Tier 1 suppliers with a proven and well-supported methodology for defining and implementing high-bandwidth infotainment and Advanced Driver Assistance (ADAS) systems, including a standard physical layer and a robust method for system management and control with superior reliability and Quality of Service (QoS). Using MOST technology also reduces weight for easier compliance with environmental regulations.

For more information about MOST150 technology, visit http://www.microchip.com/VolvoV90_MOST1504934

TI introduces chokeless high-speed CAN transceiver families with industry-leading EMC performance

New industrial and automotive interface devices provide leading combination of protection and compliance

Texas Instruments (TI) (NASDAQ: TXN) today introduced two families of controller area network (CAN) transceivers that meet all industry requirements for electromagnetic compatibility (EMC) from U.S. and European automotive manufacturers. Delivering high bus-fault protection, fast CAN flexible data rate (FD) speeds and the industry's shortest loop delay,

the TCAN1042 and TCAN1051 CAN transceiver families provide the industry's best combination of protection and high performance for a variety of automotive and industrial applications. For more information about these new CAN transceivers, see http://www.ti.com/tcan1042-pr-eu and http://www.ti.com/tcan1051-pr-eu.

Key features and benefits of the new CAN transceiver families:

Compliance with EMC standards from leading international organizations: The 16 Automotive Electronics Council (AEC) Q100-qualified devices meet EMC requirements for automobile manufacturers in the United States (Society of Automotive Engineers [SAE] J2962) and Europe (Ingenieurbüro für Industrielle Elektrotechnik [IBEE]-Zwickau). The eight industrial devices meet the requirements of the Comité International Spécial des Perturbations Radioélectriques (CISPR) 22, International Electrotechnical Commission (IEC) 61000-4-6 up to 10 V, IEC 61000-4-4 Criteria A to ±4 kV, and IEC 61000-4-3 from 80 MHz to 2.7 GHz up to 100 V/meter.

Enables common-mode choke removal: The devices eliminate the need for an external noise-suppressant common-mode choke component, thereby reducing bill-of-materials cost and space in automotive and industrial designs.

High bus-fault and electrostatic discharge (ESD) protection: High bus-fault protection up to 70 V exceeds 12-, 24- and 48-V battery requirements, in addition to protecting against 24-V DC industrial power supplies. This protects CAN bus pins against short-to-DC voltages. ESD protection up to ±15 kV eliminates the need for external transient voltage suppression (TVS) diodes, saving board space and cost.

Increased bandwidth: A fast CAN FD speed of up to 5 Mbps increases the communication speed and data-transfer capability between electronic control units and nodes on the CAN network.

Industry-leading flexibility: The industry's shortest loop delay of 175 ns enables more margin in the system design, longer networks and more nodes on the CAN bus.

Tools and support to speed design

Engineers can quickly and easily evaluate the performance of the TCAN1042 and TCAN1051 families with an evaluation module (EVM). The TCAN1042DEVM is available today for US$49 from the TI store and authorized distributors.

Package, availability and pricing

The TCAN1042 and TCAN1051 families of 24 eight-pin CAN transceivers are available today in 1,000-unit quantities starting at US$0.48. TCAN1042 devices contain a standby mode with a bus wake-up feature and variations for fault protection, bit rate and level-shifting. TCAN1051 devices include a silent mode and variations for fault protection, bit rate and level-shifting.

Learn more about TI's CAN transceiver portfolio:

Check out TI's comprehensive portfolio of CAN transceivers.

Jump-start your design with a TI Designs reference design:

IEC 61000 ESD, EFT and Surge Protected CAN Reference Design.

Read the TI Industrial Strength blog post, "How to protect CAN bus transceivers from ESD and transients."

Download the white paper, "Simplify CAN bus implementations with chokeless transceivers"

Check out these videos about the new TCAN1042 and TCAN1051 CAN transceiver families:

TCAN1042 Emissions Automotive EMC Conformance Testing.

TCAN1042 and TCAN1051 Automotive EMC Conformance Testing Conducted Immunity Performance.

TCAN1042EVM Board Tour.

No more workarounds: The new TO-220 FullPAK Wide Creepage Package

Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) today introduced the TO-220 FullPAK Wide Creepage package. The new package is offered for the 600 V CoolMOS™ CE, targeting a broad range of low power consumer applications. This package features an improved creepage and has been developed to meet the demanding requirements of open frame power supplies where pollution might lead to arcing failures of applications.

The TO-220 FullPAK Wide Creepage replaces frequently used workarounds to increase creepage distance such as silicon potting, the usage of sleeves, pre-bending of leads or others. Offering a better alternative to workarounds, customers profit from reduced system costs when implementing the new package.

Wide spread pins prevent failures

The TO-220 FullPAK Wide

Creepage package targets open frame power supplies such as TV adapters where dust can enter the case through air vents. These dust particles can reduce the effective creepage between pins over time which may lead to high voltage arcing. The new TO-220 FullPAK Wide Creepage package comes with a pin distance of 4.25 mm instead of the prevailing 2.54 mm found in a standard TO-220 FullPAK package.

The other outer dimensions of the new package are almost identical to the TO-220 FullPAK. Additionally, the new Wide Creepage package shows all the well-known benefits of a standard FullPAK, predominantly its excellent isolation behavior as well as the assembly automation ability.

Availability

The TO-220 FullPAK Wide Creepage package is available now. For further information: www.infineon.com/TO220-FP-widecreepage.

Revolutionize high-performance power conversion with TI's 600-V GaN FET power stage

Building on decades of power-management innovation, Texas Instruments (TI) (NASDAQ: TXN) today announced the availability of 600-V gallium nitride (GaN) 70-mΩ field-effect transistor (FET) power-stage engineering samples, making TI the first and only semiconductor manufacturer to publicly offer a high-voltage driver-integrated GaN solution. The new 12-A LMG3410 power stage coupled with TI's analog and digital power-conversion controllers enables designers to create smaller, more efficient and higher-performing designs compared to silicon FET-based solutions. These benefits are especially important in isolated high-voltage industrial, telecom, enterprise computing and renewable energy applications. For more details, see www.ti.com/lmg3410-pr-eu .

"With over 3 million hours of reliability testing, the LMG3410 gives power designers the confidence to realize the potential of GaN and to rethink their power architecture and systems in ways not feasible before," said Steve Lambouses, TI vice president of high-voltage power solutions. "Expanding on TI's reputation for manufacturing capability and extensive system-design expertise, the new power stage is a significant step for the GaN market."

With its integrated driver and features such as zero reverse-recovery current, the LMG3410 provides reliable performance, especially in hard-switching applications where it can dramatically reduce switching losses by as much as 80 percent. Unlike stand-alone GaN FETs, the easy-to-use LMG3410 integrates built-in intelligence for temperature, current and undervoltage lockout (UVLO) fault protection.

Proven manufacturing and packaging expertise

The LMG3410 is the first semiconductor integrated circuit (IC) to include GaN FETs manufactured by TI. Building on years of expertise in manufacturing and process technologies, TI creates its GaN devices in a silicon-compatible factoryand qualifies them with practices that are beyond the typical Joint Electron Device Engineering Council (JEDEC) standards to ensure the reliability and robustness of GaN for demanding use cases. Easy-to-use packaging will help increase the adoption of GaN power designs in applications such as power factor controller (PFC) AC/DC converters, high-voltage DC bus converters and photovoltaic (PV) inverters.

Key features and benefits of the LMG3410

Double the power density. The 600-V power stage delivers 50 percent lower power losses in a totem-pole PFC compared with state-of-the-art silicon-based boost power-factor converters. The reduced bill of materials (BOM) count and higher efficiency enable a reduction in power-supply size of as much as 50 percent.

Reduced packaging parasitic inductance. The new device's 8-mm-by-8-mm quad flat no-lead (QFN) package decreases power loss, component voltage stress and electromagnetic interference (EMI) compared to discrete GaN solutions.

Enables new topologies. GaN's zero reverse-recovery charge benefits new switching topologies, including totem-pole PFC and LLC topologies to increase power density and efficiency.

Expanding the GaN ecosystem

To support designers who are taking advantage of GaN technology in their power designs, TI is also introducing new products to

expand its GaN ecosystem. The LMG5200POLEVM-10, a 48-V to 1-V point-of-load (POL) evaluation module, will include the new TPS53632G GaN FET controller, paired with the 80-V LMG5200 GaN FET power stage. The solution allows for efficiency as high as 92 percent in industrial, telecom and datacom applications.

Availability and pricing

TI will offer a development kit that includes a half-bridge daughtercard and four LMG3410 IC samples. A second kit contains a system-level evaluation motherboard. When used together, these two kits enable immediate bench testing and design. The two development kits are available for purchase now in the TI store and are priced at $299.00 and $199.00, respectively.

Scienlab presents solutions for BMS development based on Linear Technology BMS products

Scienlab will present its engineering services and products for the entire development chain of battery management systems (BMS) at Hannover Messe, Linear Technology Stand H23, Hall 9.

ScienlabIn addition to its energy storage test system for characterization of cells, Scienlab will also present a BMS test environment for BMS development and validation, as well as newly developed Module Monitoring Electronics using Linear Technology's LTC6804 multicell battery monitor.

The LTC6804 is a 3rd generation multicell battery stack monitor that measures up to 12 series-connected battery cells with a total measurement error of less than 1.2 mV. The cell measurement range of 0 V to 5 V makes the LTC6804 suitable for most battery chemistries. With six programmable 3rd order low pass filter settings, the LTC6804 data acquisition rate and noise reduction can be optimized for the application. In the fastest ADC mode, the LTC6804 can measure all 12 cells within 290 µs.

The BMS development at Scienlab is based on the proven V-model, which comprises the phases of design, implementation and testing

BMS design

Alongside its own BMS, Scienlab also offers specific tailor-made solutions for customer applications. For this purpose, the company determines the necessary BMS functions taking into account the individual customer application, compliance with applicable standards and safety requirements. Specifications are then defined for development as well as the software and hardware.

Implementation of BMS software and hardware

Scienlab offers complete model-based software development including code generation in MATLAB/Simulink. This simplifies ideal parameterization of the BMS for the cells used, and thus ensures optimum capacity utilization and maximum durability of the connected cells.

Since the purely statistical values from the battery datasheet are not sufficient for optimum BMS design, cells are characterized with Scienlab's energy storage test system in order to determine the required parameters. Non-linear effects are also included here, such as the interdependencies of temperature, current or state of charge.

For model-based development, Scienlab also has a model-based test environment. In this environment, the BMS software can be tested at very early stages of development with the aid of cell models and simulation of the other BMS peripheral devices (e.g., charger). Scienlab also realizes the corresponding BMS hardware for the specific customer application.

BMS validation with Scienlab test systems

The BMS is validated with the Scienlab BMS test environment. Using various emulators that simulate the cells, current and temperature sensors and insulation resistances, reproducible, safe and reliable BMS tests are carried out without the need for real components such as battery cells.

Interfaces with real-time capability permit fast data transfer (1 kHz) between the test systems and the hardware-in-the-loop system. The voltage measuring accuracy of up to ± 0.2 mV and current measuring accuracy of up to ± 2 µA ensure exact voltage and current adjustment and

therefore optimum emulation of the cell characteristics. Highly dynamic bidirectional voltage sources permit voltage jumps in less than 80 µs.

Hitachi Automotive Systems has developed a high-output 48V lithium-ion battery pack for mild hybrid electric vehicles

Hitachi Automotive Systems, Ltd. today announced that it has developed a high-output 48-volt battery pack to improve the fuel efficiency of mild hybrid electric vehicles ("mild HEVs") that use a battery and motor to provide power assistance when the vehicle is being driven by its internal combustion engine. This summer, Hitachi Automotive Systems will start shipping samples to customer car manufacturers and aims to commence mass-production in fiscal 2018.

A mild HEV is a technology for improving the fuel efficiency of passenger cars by using the power of a battery-driven motor to provide power assistance when the vehicle is being driven by gasoline power. In recent years, mild HEV systems, especially those using 48-volt lithium-ion batteries, have been attracting increasing attention in the vehicle markets of Europe and China. In Japan's domestic car market, the mainstream has been strong HEVs, which use high-voltage batteries of 100 volts or more, with mild HEV systems being limited to light cars that are equipped with low-voltage 12-volt batteries and storage capacitors. In Europe and China, however, mild HEV systems that use 48-volt batteries are rapidly spreading as they are viewed as a relatively low-priced way of achieving improved fuel economy. With the expectation being for rapid future growth, Hitachi estimates that by 2023, HEV unit production will be over 2 million units in Europe and over 4 million units in China.

In view of these trends in the vehicle markets of Europe and China, Hitachi Automotive Systems concentrated on bringing together its accumulated strengths in the technology of manufacturing lithium-ion battery cells for hybrid vehicles and its battery management system (BMS) technology to develop a battery pack, and in this March completed the basic design of a lithium-ion battery pack for 48-volt HEV systems.

The newly developed 48-volt lithium-ion battery pack is a highly integrated package that in addition to the BMS board and battery cells, includes a relay and fuse. With excellent low-temperature characteristics and approximately 1.5 times the output density of Hitachi's previous battery cells, it is a highly reliable battery pack that, with its high-output prismatic lithium-ion cells, when assisting the acceleration of a motor using a 48-volt system, delivers a fully sufficient torque performance for a maximum output of 10 kW or more and maximum input of 13kW or more (for 10 seconds in each case). Moreover, the compact design of the battery pack helps to increase the degree of installation freedom in the passenger compartment.

Hitachi Automotive Systems is in charge of product development and sales, while the manufacturing will be done by Hitachi Vehicle Energy, Ltd., which is a manufacturer of automotive lithium-ion batteries.

The lithium-ion battery pack will be on display at the 14th Beijing International Automobile Exhibition (also referred to as the Beijing Motor Show 2016) from Wednesday April 27 to Wednesday May 4 in Beijing, China, and at the Automotive Engineering Exposition Yokohama 2016 held under the sponsorship of the Society of Automotive Engineers of Japan, Inc. to be held at Pacifico Yokohama from Wednesday, May 25 to Friday May 27.

Hitachi Automotive Systems will continue to contribute to the evolution of electric vehicles by strengthening lithium-ion batteries and electric powertrain components.

Cadence Unveils Next-Generation Virtuoso Platform Featuring Advanced Analog Verification Technologies and 10X Performance Improvements Across Platform

Highlights:

Next-generation Virtuoso ADE enables engineers to explore,

analyze and verify designs against goals to ensure that design intent is maintained throughout the design cycle

Virtuoso Layout Suite offers up to 100X accelerated zoom, pan, drag and draw performance on large layouts

Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced the delivery of the next-generation Virtuoso® platform which offers designers an average of 10X performance and capacity improvement across the platform. The platform includes new technologies within the Cadence® Virtuoso Analog Design Environment (ADE) and enhancements to the Cadence Virtuoso Layout Suite to address requirements for automotive safety, medical device and Internet of Things (IoT) applications.

For more information on the Virtuoso ADE product suite, please visit www.cadence.com/news/virtuosoade, and for more information on the Virtuoso Layout Suite, go to www.cadence.com/news/virtuosols.

Next-Generation Virtuoso ADE Product Suite

The next-generation Cadence Virtuoso ADE product suite addresses the challenges that come with the emergence of new industry standards, advanced-node designs and the requirements for system design, enabling engineers to fully explore, analyze and verify designs to ensure that design intent is maintained throughout the design cycle. Enhanced data handling provides up to 20X improvement in loading waveform databases in excess of 1GB and a 50X improvement in versioning and loading set-up files into the environment. The suite's key technologies include:

Virtuoso ADE Explorer: Enables fast and accurate real-time tuning of design specs, provides pass/fail datasheets and delivers a complete corners and Monte Carlo statistical environment for detecting and fixing variation problems

Virtuoso ADE Assembler: Enables engineers to analyze their designs under various process-voltage-temperature (PVT) combinations; also offers GUI-based verification plans so designers can easily create conditional and dependent simulations

Virtuoso ADE Verifier: Provides a substantial technological advancement in analog verification, offering an integrated dashboard that lets engineers easily verify that all of the blocks are contributing to the overall design specifications

Cadence Virtuoso Analog Design Environment (ADE):

Reimagining analog design with emphasis on usability, performance, and innovation

"The new Virtuoso ADE Verifier technology and the Virtuoso ADE Assembler technology run plan capability make our design teams more productive," said Yanqiu Diao, deputy general manager, Turing Processor business unit at HiSilicon Technologies Co., Ltd. "Through our early use of the new Cadence Virtuoso ADE product suite, we've found that we can improve analog IP verification productivity by approximately 30 percent and reduce verification issues by one-half. Our smartphone and network chip projects should benefit from these latest capabilities."

Virtuoso Layout Suite Enhancements

The enhanced Virtuoso Layout Suite addresses the most complex layout challenges by offering accelerated performance and productivity for custom analog, digital and mixed-signal designs at the device, cell, block and chip levels. The suite's latest updates provide the following enhancements:

Graphics rendering performance: Provides from 10X to 100X accelerated zoom, pan, drag and draw performance on large layouts

Module Generator (ModGen): Interactive pattern manipulation flow that makes real-time customization of ModGens very visual and simple; also now supports synchronous clones, which are layout elements with identical physical properties—like width and length of transistors—that the layout designer can layout once and reuse

New structured device-level routing: Structured device-level routing capabilities can enhance routing productivity by as much as 50 percent

"Customers have continually placed their trust in the Cadence Virtuoso platform for more than 25 years, taping out thousands of designs each year," said Tom Beckley, senior vice president and general manager, Custom IC & PCB Group at Cadence. "The need to do custom design has never been greater, and increasing complexity is driving the need to further simplify the design

process so our customers can meet design schedules. Cadence remains at the forefront of custom design innovation with the delivery of our next-generation Virtuoso platform, which enables fast, accurate custom design."

Build SFP28 Modules for Data Centers and Radio Access with Industry's First Transceiver IC in Mass Production

Keep heat away from lasers using Maxim Integrated's transceiver chip and TO-can optics.

Enables low-cost optics: Reduced module BOM through the use of TO-can based opticsMUNICH, Germany – March 16, 2016 – Manufacturers of SFP28 modules for data center and radio fronthaul applications can now use TO-cans enabled by the industry's first transceiver IC, which is shipping now from Maxim Integrated Products, Inc.(NASDAQ: MXIM).

Maxim's SFP28 transceiver allows module manufacturers to avoid a driver inside the transmit optical subassembly (TOSA). This keeps heat away from the sensitive laser, simplifies production, and improves yield. Maxim's SFP28 transceiver also includes advanced digital eye tuning capabilities that enable use of low-cost TO-can based optics. The SFP28 module can simply be designed in the same way as an SFP+ module using TO optics, one transceiver IC, and one controller IC.

SFP28 optical modules for data centers and radio fronthaul applications need to offer cost competitive performance relative to the incumbent SFP+ module, while still having low power and a wide operating temperature range. Optimized specifically for these requirements, Maxim's 28.1Gbps low-power transceiver IC has a CDR and laser driver in the transmit path, and a high sensitivity limiting amp and CDR in the receive path.

Maxim will demonstrate its industry-leading SFP28 transceiver and other optical ICs at OFC 2016, March 22-24, in Hall A, Booth 1272,http://bit.ly/OFC2016.

Key Advantages

Accelerates time to market: Digital eye tuning at the output reduces design spins

Reduces production costs: Reusing TO-can-based 10Gbps manufacturing flow improves yield

Commentary

"Maxim's SFP28 transceiver builds on our proven 100Gbps technology and gives the industry what it needs to move to higher bandwidth interconnect," said Andrew Sharratt, Director of Business Management at Maxim Integrated. "Shipping now to customers who are already in mass production, Maxim's SFP28 IC enables cost effective upgrades to enterprise, hyperscale data center, and radio access networks."

"Demand for SFP28 modules will experience strong growth over the next five years, as the market moves from 10Gbps per lane to 25Gbps," said Dale Murray, Principal Analyst at LightCounting Market Research. "With its new transceiver IC, Maxim is poised to support this move by simplifying module design and lowering costs."

Amphenol Industrial's UPT Connector Series

Amphenol Industrial Products Group has expanded its PT series of connectors with a quick disconnect circular connector that is ideal for use in the heavy equipment, transportation, diesel engine and electric vehicle markets.

Based on Amphenol's 26482 series I, the UPT features a plastic shell with a metal coupling system and crimp termination. This lightweight connector has a smaller footprint and is easy to install in the field once it has been crimped in the facility. The UPT contact features three retention tines that can easily be inserted and ensure retention force.

Used in buses, diesel engines, Class 8 trucks, trailers, garbage trucks, tractors as well as in construction equipment, industrial pumping and power generation, the UPT offers bayonet coupling for quick mating and reliability.

These RoHS compliant connectors are environmentally sealed and have an operating temperature

range of -40°C to +125°C. They offer jam nut and square flange mounts for 32-way and 48-way contacts.
Amphenol's UPT contacts are available in either gold or tin. Multiple back shell sealing accessories are available upon request.

20V, 20A Monolithic Synchronous Step-Down Regulator with Ultralow DCR Current Sensing for Higher Efficiency

Linear Technology Corporation introduces the LTC7130, a constant frequency peak current mode synchronous step-down DC/DC converter with temperature-compensated ultralow DCR current sensing and clock synchronization. The device's unique architecture eases compensation and offers the ability to directly parallel multiple ICs for higher current capability. It also enhances the signal-to-noise ratio of the current sense signal, enabling the use of a very low DC resistance power inductor to maximize efficiency in high current applications. This feature also reduces the switching jitter commonly found in low DCR applications and improves current limit accuracy. The LTC7130's 4.5V to 20V input range supports a wide variety of applications, including most intermediate bus voltages, and is compatible with many battery types. Integrated N-channel MOSFETs can deliver continuous load currents as high as 20A at output voltages ranging from 0.6V to 5.5V, making it ideal for point-of-load applications such as high current / low voltage DSP / FPGA / ASIC reference designs. Other applications include telecom/datacom systems, distributed power architectures and general high power density systems.
The LTC7130's low 90ns minimum on-time allows for a high step-down ratio power supply at high frequency operation. The operating frequency is selectable from 250kHz to 770kHz and can be synchronized to an external clock. The LTC7130's total differential output voltage accuracy is ±0.5% over the -40°C to 125°C operating junction temperature range. Additional features include a high speed differential remote sense amplifier, programmable output current limit, output short-circuit protection with soft recovery, programmable soft-start/tracking, EXTVCC for reduced power dissipation and a fault indicator for output UV/OV conditions.
The LTC7130 is available in a thermally enhanced 6.25mm x 7.5mm x 2.22mm BGA package, with both RoHS lead-free and leaded SnPb (63/37) finishes. The E-and I-grades are guaranteed from -40°C to 125°C operating junction temperature range. The 1,000-piece price starts at $7.95 each for the E grade. All versions are available from stock. For more information, visit www.linear.com/product/LTC7130.

IDT Expands Power Portfolio with New Dual-Phase High-Performance Digital Power Controller

Supporting Multiple Configurations, the ZSPM1363 PWM Controller Targets High-Power System Rails, Telecommunications, Server, Storage, FPGA and Infrastructure Applications
Integrated Device Technology, Inc.® (IDT®) (NASDAQ: IDTI) today strengthened its offerings of power management products with the introduction of a high-performance dual-phase digital power controller that can help customers optimize, monitor and control high-power supply systems. The second-generation ZSPM1363digital PWM (pulse-width modulation) controller delivers high performance and excellent transient response, making it ideal for addressing the growing demands in the telecommunications, server, storage, FPGA and infrastructure markets.
The chip's extended one-time programmable (OTP) memory provides storage for multiple application configurations. The device's flexibility and ease of reuse help reduce design time, and the highly integrated silicon requires few external components to help lower system cost.
"System designers are increasingly adopting digital technology to

control their high-power supply systems," said Ed Lam, senior director of IDT's Power Business Unit. "The ZSPM1363 is a high-performance digital power controller that delivers design flexibility to reduce development cost and time to market. And because we developed it using automotive design methodology, the chip is rugged and highly reliable, with operating temperatures up to 125°C."

The ZSPM1363 features simple resistor-based compensation adjustment after programming if load condition changes; there's no need to reprogram the chip. And its multi-programmable compensation architecture achieves fast transient response while providing low ripple, steady state performance.

A related paper, titled, "Controller Scalability Methods for Digital Point Of Load Converters," can be downloaded here.

New 36V Op Amps from STMicroelectronics Raise Ruggedness, Stability, and Efficiency in Automotive and Industrial Applications

STMicroelectronics has introduced two 36V op amps that deliver enhanced performance and ruggedness in automotive and industrial applications. The op amps feature a wide supply-voltage range, stability in challenging operating conditions, and tolerance of electrostatic discharge (ESD) up to 4kV (HBM1).

The TSB572 and TSB611 single op amps are the first devices produced using ST's new 40V-ready BiCMOS2 semiconductor process. This technology delivers superior GBW/Icc3 efficiency resulting in about five times lower supply current in relation to performance, compared with standard op amps. In addition, low input-offset voltages with temperature drift below 6µV/°C simplify system design, eliminate any need for trimming or calibration, and ensure consistent performance over the specified temperature range -40°C to 125°C.

The TSB572, with rail-to-rail inputs and output, has 2.5MHz gain-bandwidth (GBW) and 1.5mV maximum input-offset voltage. The op amp is stable with capacitive loads and highly resistant to phase reversal. Its broad supply-voltage range, from 4.0V to 36V, allows reliance on specified parameters with a wide variety of power supplies.

The TSB611 has 560kHz GBW and can operate from a supply voltage as low as 2.7V. It is a unity-gain-stable device, and has extremely low input-offset voltage of 1mV as well as frugal operating current of 125µA (max.) at 36V.

Compact package options make ST's new op amps ideal for use where space is tight, such as in automotive audio systems and Electronic Control Units (ECUs).

The TSB572 is in mass production now in 3mm x 3mm DFN or Mini-SO8, priced from $0.80. The TSB611 in SOT23-5 is also in mass production, priced from $0.55 for orders of 1000 pieces.

1 HBM. Human Body Model: a standardized simulation to test susceptibility to ESD when touched

2 BiCMOS semiconductor technology combines bipolar junction transistor and CMOS transistor in a single integrated circuit

3 GBW/Icc. Gain-bandwidth per input current: industry-recognized figure of merit relating op-amp performance to power consumption.

Tektronix Introduces iPhone App for Source Measure Unit Instruments The Fastest, Easiest Way to Perform Current-Voltage (I-V) Characterization Comes to Apple iPhone and iPad

Tektronix, a leading worldwide provider of measurement solutions, today announced that the Keithley IVy app for working more efficiently and conveniently with 2600B source measure unit (SMU) instruments is available now foriPhone® and iPad® devices from the App Store. An updated version of the app with support for wireless instrument connection has also been released for Android devices onGoogle Play.

The IVy app offers users a fast and easy way to perform current-voltage (I-V) characterization, troubleshoot a device and collaborate with team members. It allows engineers to

visualize, interact with, and share measurement results, helping them to save time and increase productivity.

Taking full advantage of Apple and Android device interfaces, IVy gives simultaneous control over source levels and monitoring of test results. This makes it easy to visually analyze I-V characteristics, DUT stability, response time, or drift in a circuit using normal touch zooming and scrolling. Test data and graphs can be shared with colleagues using typical mobile sharing apps like email, messaging or file sharing services.

The free app is compatible with Keithley Series 2600B SourceMeter® Source Measure Unit (SMU) Instruments running firmware version 3.1.0 or above.

Wondering what else Tektronix is up to? Check out the Tektronix Bandwidth Banter blog and stay up to date on the latest news from Tektronix on Twitter and Facebook.

Tektronix Unlocks End-to-End ABR Monitoring New Adaptive Bit Rate Decryption for Sentry ABR Delivers Real-Time QoS, QoE and PVQ Monitoring for Multiscreen Services

Tektronix, an industry-leading innovator of video quality monitoring solutions, has unlocked end-to-end ABR monitoring with today's unveiling of decryption and decode functionality for the Sentry ABR video quality monitoring platform. The new Sentry ABR capabilities will be demonstrated in Booth #SU5006 at NAB Show, taking placeApril 18-21 in Las Vegas.

Adaptive bitrate streaming (ABR) is the underlying technology used with multiscreen, on-demand streaming services for PCs, laptops, smartphones, tablets and TVs. Also called TV Everywhere or OTT (over the top), multiscreen video services use ABR to break content into small fragments of compressed content for transmission to viewing devices. With the increased amount of content delivered via ABR, service providers need to be able to pinpoint errors in the network quickly to reduce operational expenses related to trouble calls and mean time to detect and repair (MTTD, MTTR) issues.

Tektronix Sentry products are widely deployed and are used to provide vital QoE (Quality of Experience) and PVQ (Perceptual Video Quality) information to network operators concerned about the experience they are providing their customers. With the addition of decryption and decode functionality, Sentry ABR gives service providers the breadth and depth of monitoring they are accustomed to with linear-based services. After transcoding in a typical ABR workflow, a video stream is fragmented into fixed time duration fragments, encrypted and Digital Rights Management (DRM) applied. Sentry ABR is now capable of viewing this encrypted content to evaluate the actual viewing experience, or QoE as well as determining PVQ.

"With the future of video delivery switching from linear to ABR, it is critical that service providers get the same level of monitoring with ABR services as they do with linear to truly understand the customer experience," said Charlie Dunn, general manager, Video Product Line, Tektronix. "Given the complexity of ABR content delivery, there is a lot that can go wrong, and service providers need to know about it before they start getting calls from subscribers. Our solution now offers end-to-end QoE monitoring throughout the ABR workflow so operators can quickly identify, troubleshoot and resolve issues."

An End-to-End Solution from File-Based QC to Delivered ABR Content

As the industry moves more towards ABR for delivery of all services, the amount of video content that must be tested and verified is growing quickly. Testing a high volume of small fragments and files at multiple bit rates is especially challenging. For this requirement, Tektronix offers Aurora, which provides fast and scalable file-based QC and has tests specifically designed to catch the most common causes of ABR streaming problems. When used in conjunction with the frame accurate Hydra Player operators have the ability to visualize their content and any issues detected. Operators can then add review information for those responsible for producing the ABR content.

From there, the Sentry platform is used to detect QoS (Quality of Service) anomalies in the network at the IP and MPEG TS layers as well as in QoE, identifying issues that represent the bulk of trouble calls from subscribers including frozen video, tiling/macroblocking and audio disruptions or audio-level

and loudness issues. Within an ABR network, Sentry ABR is then used to ensure the availability of content and provide comprehensive QoE analysis on each stream at each bitrate in real time.

Availability

Sentry ABR with decryption/decode is available now. For more information please visit: www.tek.com/video-quality-monitors/sentry-abr

Wondering what else Tektronix is up to? Check out the Tektronix Bandwidth Banter blog and stay up to date on the latest news from Tektronix on Twitter and Facebook.

Keysight Technologies Announces E-Band Signal Analysis Reference Solution for Multichannel mmW Test

Lower-Cost Multichannel mmW Test Solution Helps Engineers Develop New Technologies Faster, More Efficiently

Highlights:

1- or 2-channel E-band (60-90 GHz) analysis with M1971E smart mixer(s)

Measurement plane is corrected to the waveguide flange to provide corrected results

Includes an oscilloscope and signal generator for better asset utilization

Keysight Technologies, Inc. (NYSE: KEYS) today announced an E-band Signal Analysis Reference Solution to provide low-cost millimeter wave analysis capability for applications in the 60-90 GHz range. The reference solution is based around the 10-bit ADC Infiniium S-Series oscilloscope to provide 2.5 GHz of high-fidelity, millimeter wave frequency analysis bandwidth.

The E-Band Signal Analysis Reference Solution provides a powerful test platform for analyzing emerging communication standards operating at millimeter wave frequencies. Two-channel capability allows for testing of multichannel devices; different antenna polarizations simultaneously; and channel sounding measurements. The reference solution is made up of a combination of hardware instruments and software. The new N8838A external mixer assistant software enables the S-Series oscilloscope to control the N5183B MXG X-Series microwave signal generator and the M1971E waveguide smart mixer. Also with the 89601B vector signal analysis software, engineers can make insightful measurements for complex signal analysis. This makes it simple to get accurate, calibrated measurements on E-band signals.

"With applications such as 5G, WiGig, automotive radar and millimeter wave backhaul becoming more prevalent, a simple-to-use, low-cost solution that maintains high performance is needed," said Dave Cipriani, vice president and general manager of Keysight's oscilloscope business. "This reference solution enables customers to develop these new technologies faster and more efficiently."

More information about the E-band Signal Analysis Reference Solution is available at www.keysight.com/find/solution-e-bandsignalanalysis. Images are available at www.keysight.com/find/solution-e-bandsignalanalysis_images.

Keysight will show the new E-Band Signal Analysis Reference Solution at the International Microwave Symposium, Booth 1239, Moscone Center, San Francisco, May 22-27.

U.S. Pricing and Availability

The E-band Signal Analysis Reference Solution and the N8838A external mixer assistant will be available on May 4. Contact Keysight at www.keysight.com/find/contactus for pricing and delivery information.

Keysight and Bluetest Announce Integration of the UXM Wireless Test Set in Bluetest's RTS65 Reverberation Test System

Bluetest Flow Measurement Software Now Supports Keysight's Latest Instrumentation, Simplifying Advanced OTA Measurements

Highlights:

Keysight and Bluetest collaborate to provide integrated OTA solutions

E7515A UXM Wireless Test Set provides support for the most advanced wireless devices

Bluetest RTS65 and Flow supports the wireless industry's latest needs within LTE-A

Keysight Technologies, Inc. (NYSE: KEYS) and Bluetest AB today announced that the Keysight UXM Wireless Test Sethas now been integrated into Bluetest's leading reverberation chamber OTA test solutions, enabling mutual

customers to make measurements quickly and with confidence.

"We're delighted to extend our support of Keysight's instruments to the UXM Wireless Test Set, which has proven easy to integrate," said Klas Arvidsson, product manager for Bluetest's OTA solutions. "Together we are able to innovate at the forefront of the market's requirements as LTE-A continues to evolve with more carriers and higher order MIMO."

"Through this excellent collaboration with Bluetest, we are now in a position to fully use the power of the UXM platform," said Satish Dhanasekeran, general manager of Keysight's Wireless Devices and Operators Segment. "Bluetest's RTS solutions are well proven in the marketplace."

Bluetest's Reverberation Test System RTS65 and measurement software Flow makes it quite easy to add additional streams to the test set-up. Bluetest RTS is available with up to eight measurement ports, hence supporting a UXM solution with, for example, four 2×2 MIMO carriers or two 4×4 MIMO carriers without any external combiners or additional equipment.

Recent enhancements to the UXM Wireless Test Set include support for the very latest LTE-A evolutions, such as 1.6Gbps data rates and up to 8×4 downlink MIMO & 5CC. The UXM also supports 2G and 3G technologies, making it an ideal choice for testing the latest wireless UEs from the simplest Internet-Of-Things devices to the most advanced smartphones.

More information about Keysight's UXM wireless test set is available at www.keysight.com/find/UXM. High resolution images are available at www.keysight.com/find/UXM_ images. Videos demonstrating the UXM's versatile capabilities are available on YouTube. Contact Keysight at www.keysight.com/find/contactus for E7515A UXM pricing and delivery information.

Micronas presents sensor solution for multidimensional measurement with integrated decoupling capacitors

Micronas, a TDK group company, expands its Hall-effect sensor portfolio with integrated capacitors with the HAC 37xy sensors for multidimensional magnetic field measurements in automotive and industrial applications. The TO92UF package was especially designed for this new sensor type and integrates both a chip from the HAL 37xy sensor family based on Micronas' 3D HAL® technology for detecting linear movements and angles as well as two capacitors up to 100 nF. The HAC 37xy sensors enable angle measurements of up to 360° or linear measurements of up to 40 mm by use of two-pole bar magnets with a length in the range of 5 mm. At the same time, the sensors achieve an ESD immunity of up to 8 kV and meet all of the stringent EMC requirements, such as the current Bulk Current Injection (BCI), for example. Micronas will present its HAC 37xy sensors from May 10 to 12, 2016, at the Sensor+Test exhibition in Nuremberg at booth 204 in hall 1.

With the HAC 37xy sensors, Micronas offers its customers three different direct-angle sensor variants: The proven HAL 37xy sensor family, a version with redundancy function via two integrated Hall elements (HAR 37xy) and a version with integrated capacitors (HAC 37xy). While the HAL 37xy and HAR 37xy sensors are available in the SOIC8 SMD package, the pins of the TO92UF package can be welded or soldered directly to a lead frame. This eliminates the need for a printed circuit board (PCB), thus reducing the total system size and cost. Furthermore, the overall system long-term reliability is significantly improved.

All members of the HAC 37xy use a so-called pixel cell, which consists of one horizontal (BZ) and two vertical (BX, BY) Hall elements. The pixel cell measures three magnetic field vector components at one point. Magnetic field lines in parallel to the sensor surface are detected by the vertical Hall elements, whereas the component perpendicular to the chip surface is captured by the horizontal Hall element. The ability to evaluate the relative strength out of the horizontal and vertical magnetic field components is the key for excellent angular performance. Thanks to the 3D HAL technology, the HAC 37xy sensors allow temperature-stable position measurements with high accuracy at reduced system cost. The new sensors suit particularly for PCB-free module solutions in automotive applications, such as turbo chargers, EGR and throttle valves. In these applications, the HAC 37xy sensors

not only increase EMC performance, but also the system reliability.

For these applications, the sensors provide a high degree of flexibility by offering various output formats. The HAC 37xy sensors come both with a ratiometric analog output (HAC 372x) as well as with a digital output (HAC 373x). Besides pulse-width modulation (PWM) output, the SENT protocol according to the latest generation of SAEJ2716 is also supported.

Samples will be available from mid-May 2016. Start of production is planned for early 2017.

8µA IQ Surge Stopper Protects Electronic Systems from Overvoltage & Overcurrent Transients

Linear Technology Corporation introduces the LTC4380, an ultralow quiescent current (IQ) surge stopper, providing compact overvoltage and overcurrent protection for always-on 4V to 72V electronics in automotive, industrial and avionic systems. The LTC4380 replaces traditional shunt circuits composed of bulky inductors, capacitors, transient voltage suppressors (TVS), and fuses with a simple IC and series N-channel MOSFET solution, saving board space and enabling continuous operation through transient voltage or current surges. The LTC4380 protects downstream electronics from input overvoltage up to the MOSFET rating, while also protecting the power supply from output overload. Device current consumption is a mere 8µA in normal operation and 6µA in shutdown mode, prolonging battery run and standby time. The low current allows a large filtering resistor to the device supply pin, enabling operation through automotive cold crank and overvoltage transients above 100V.

During an input voltage surge, such as automotive load dump, the LTC4380 drops the excess voltage across the external MOSFET while clamping its gate and therefore the output to a safe voltage. This enables the use of lower voltage rated electronics downstream, saving costs. The clamp voltage is pin-selectable for 12V and 24V systems, or adjustable with an input Zener diode. During an output overload or short-circuit, the LTC4380 regulates the forward path to a current limit set by a sense resistor. For sustained overvoltage or overcurrent conditions, a MOSFET stress-accelerated timeout ensures safe turn-off of the MOSFET. In contrast, traditional protection circuits may blow a fuse or burn out the TVS, requiring repairs.

The LTC4380 withstands a reversed input, such as an incorrectly inserted battery, to -60V. Adjustable input undervoltage lockout threshold blocks start-up for out-of-range voltages, avoiding deeply discharged batteries. The device also controls inrush current during hot plug of a circuit board's power supply.

The LTC4380 is available in four options: the LTC4380-1 and LTC4380-2 have a pin-selectable clamp voltage, whereas the LTC4380-3 and LTC4380-4 clamp voltage is set with an input Zener diode. After a fault, the LTC4380-1 and LTC4380-3 latch the MOSFET off, while the LTC4380-2 and LTC4380-4 automatically turn on with a 0.1% duty cycle. Specified over the 0°C to 70°C commercial, -40°C to 85°C industrial and -40°C to 125°C automotive temperature ranges, the LTC4380 is offered in 10-pin MSOP and 3mm x 3mm DFN packages. 1,000-piece pricing starts at $2.48 each. Device samples and evaluation circuit boards are available online or from your local Linear Technology sales office. For more information, visit www.linear.com/product/LTC4380

Vishay Intertechnology Medium-Power Planar Transformer Provides Higher Efficiency, Space Savings Over Traditional Winding Technology

Vishay Intertechnology, Inc. (NYSE: VSH) today introduced a new planar transformer offering power from 1 kW to 3 kW in a compact 70 mm by 53 mm by 22 mm size. Compared to devices built on traditional winding technology, the Vishay Sfernice PLA51 delivers the same power transfer / conversion while offering higher efficiency and a lower weight and profile.

The device released today is optimized for DC/DC power converters, on-board chargers for electric vehicles, UPS, power control cooling units, and solar inverters.

In these applications, the PLA51's high typical efficiency of > 99 % typical reduces losses, while its low profile of 22 mm saves space in sub-assemblies. In addition, the transformer's reduced weight of 170 g is a key parameter for power supplies in avionics applications.

Providing excellent repeatability, the PLA51 features a frequency range of 50 kHz to 400 kHz and operates over a temperature range from -55 °C to +125 °C with heatsink dissipation. Offered in full-bridge, half-bridge, and forward power supply topologies, the transformer features tapped outputs for fast and easy connection. This RoHS-compliant device is also available in custom designs upon request.

Samples of the PLA51 are available now. Production quantities will be available in Q4 2016 with lead times of 12 weeks for large orders.

Vishay Intertechnology, Inc., a Fortune 1000 Company listed on the NYSE (VSH), is one of the world's largest manufacturers of discrete semiconductors (diodes, MOSFETs, and infrared optoelectronics) and passive electronic components (resistors, inductors, and capacitors). These components are used in virtually all types of electronic devices and equipment, in the industrial, computing, automotive, consumer, telecommunications, military, aerospace, power supplies, and medical markets. Vishay's product innovations, successful acquisition strategy, and "one-stop shop" service have made it a global industry leader. Vishay can be found on the Internet at www.vishay.com.

Lattice Expands Award-Winning MachXO3™ Product Family New Product Offers 35 Percent Increase in LUTs and 15 Percent More I/Os, Continuing to Deliver on the Promise of Lowest Cost Per I/O Device

Addition of largest density member, MachXO3-9400, delivers more I/Os and on-chip memory

New features help reduce BOM cost, provide best value for I/O intensive, and high-resolution video applications

Integrates support for improved security and reliability

Lattice Semiconductor Corporation (NASDAQ: LSCC), the leading provider of customizable smart connectivity solutions, today announced the expansion of its award-winning MachXO3™ family of FPGAs with the addition of the MachXO3L-9400 and MachXO3LF-9400 devices available in multiple packages. Built in response to customer demand, the new devices bring expanded I/O and logic support for control PLD applications, while increased on-chip memory improves picture clarity for low cost video bridging in large monitor applications. The MachXO3 family targets the server, communications, industrial and display markets.

The new enhanced features of the MachXO3 family make it ideally suited for implementing control path functions. Glue-less 1V I/O interface for out-of-band communication with new, leading-edge processors.

Hitless I/O enables in-system hardware upgrade along with a switch over from its old configuration to the newly programmed configuration without interrupting the circuit board operation – a feature that is mandatory in high volume systems.

Password protection feature makes the system more robust against malicious erase commands.

SED/SEC/SEI feature enables recovery from a soft error event in milliseconds.

Addition of analog I/Os is simple and enables integration of all hardware management while reducing overall cost.

Fast 900 Mbps operating speeds supported by MachXO3-9400 FPGA's I/Os ensures that even high-resolution video streams operate smoothly.

"Our award-winning MachXO3 FPGA portfolio is ideally suited for control PLD and bridging, offering the smallest, lowest cost and instant-on programmable platform to enable the integration of critical functions demanded by today's advanced processors and SoCs," said Shyam Chandra, senior product marketing manager at Lattice Semiconductor. "We continue to enhance our MachXO3 family to deliver customizable solutions that meet our customers' next-generation product requirements."

For more information about the MachXO3 product family, please visit the family page: MachXO3.

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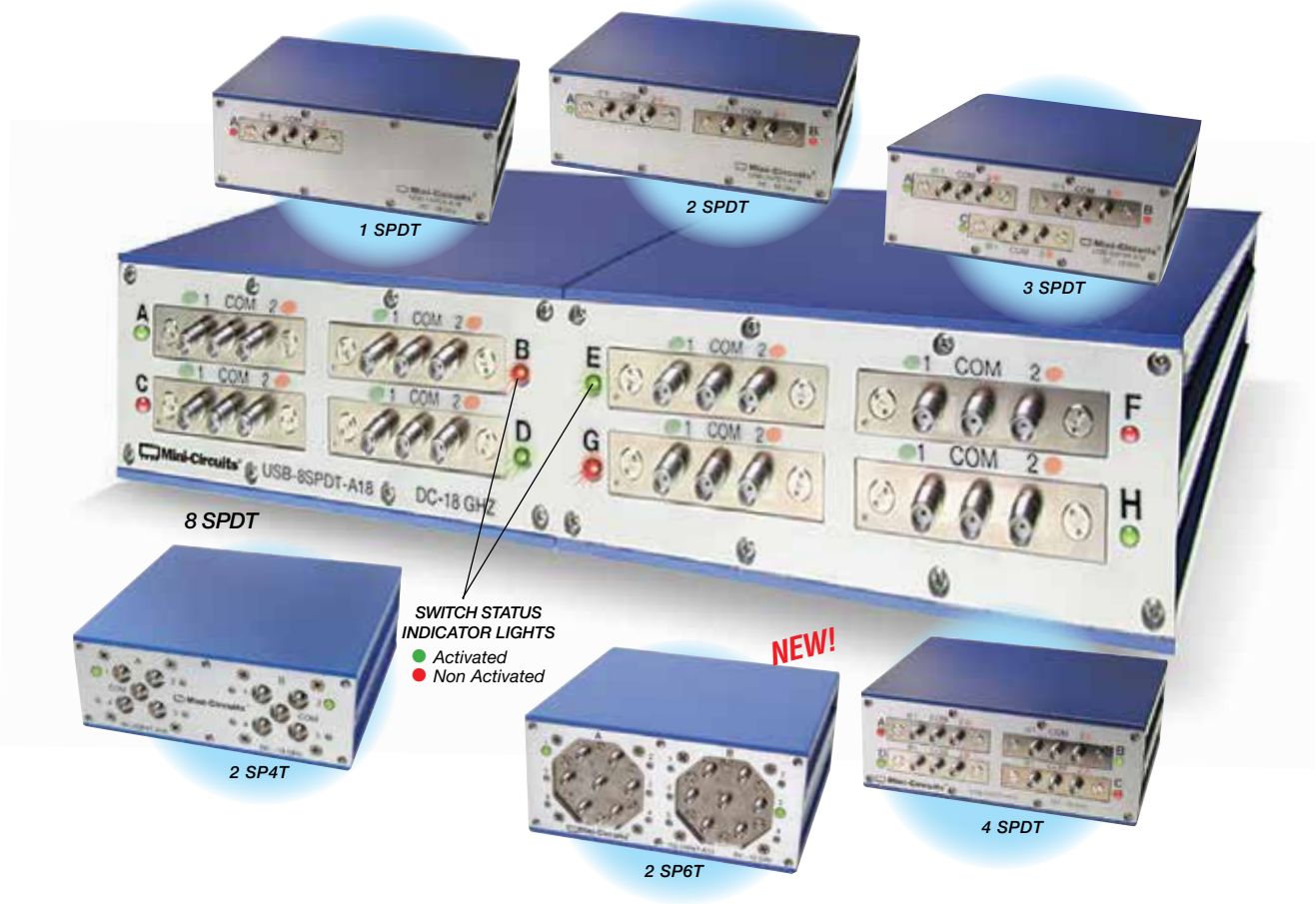

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