

New-Tech

Magazine *Europe*

January
2016

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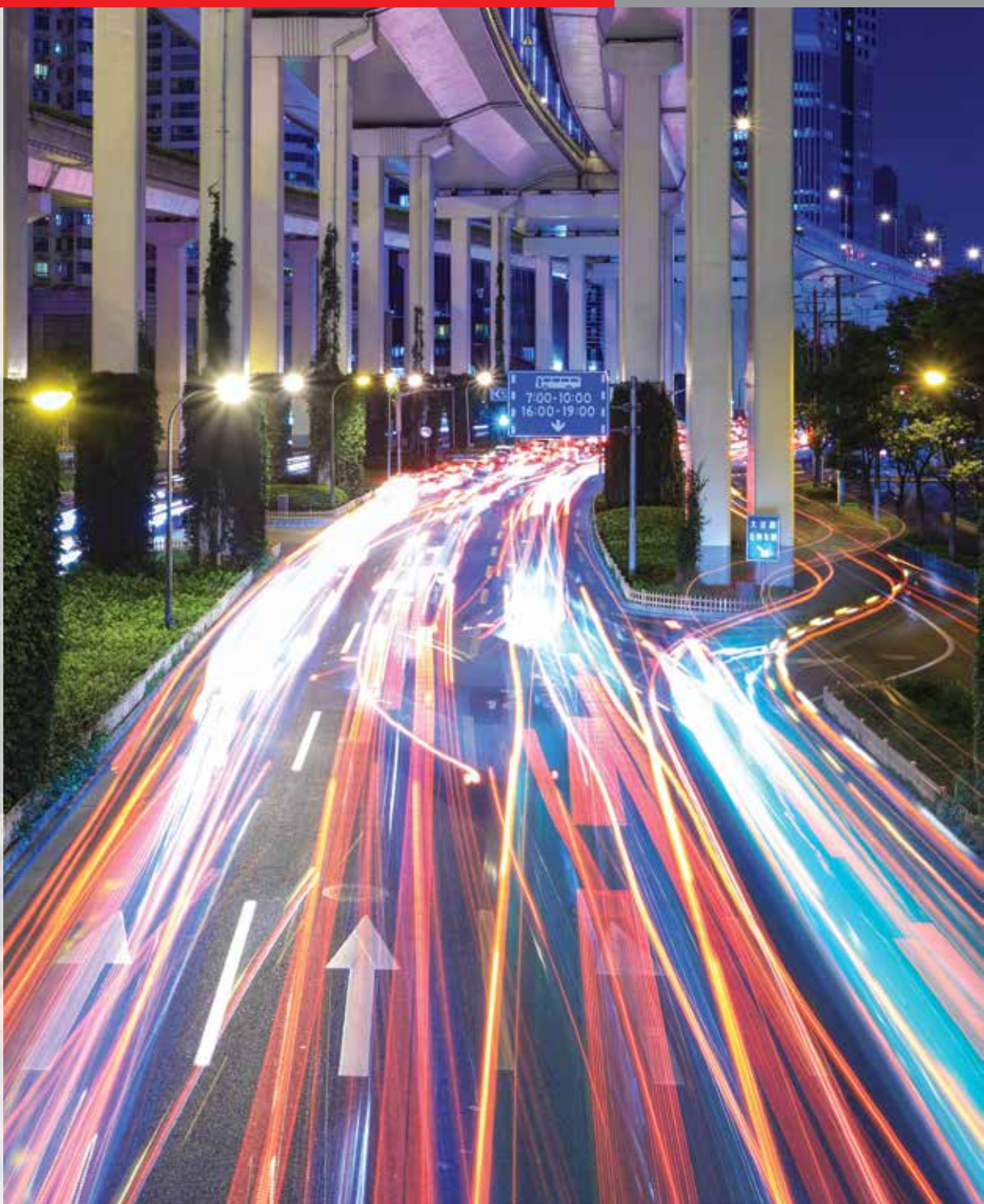
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ZHL-5W-2G+	800-2000	45	5	5	995
ZHL-10W-2G+	800-2000	43	10	12	1295
• ZHL-16W-43+	1800-4000	45	12	16	1595
• ZHL-20W-13+	20-1000	50	13	20	1395
• ZHL-20W-13SW+	20-1000	50	13	20	1445
LZY-22+	0.1-200	43	16	30	1495
ZHL-30W-262+	2300-2550	50	20	32	1995
ZHL-30W-252+	700-2500	50	25	40	2995
LZY-2+	500-1000	47	32	38	2195
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• ZHL-100W-52+	50-500	50	63	79	1995
• ZHL-100W-GAN+	20-500	42	79	100	2395
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January 2016

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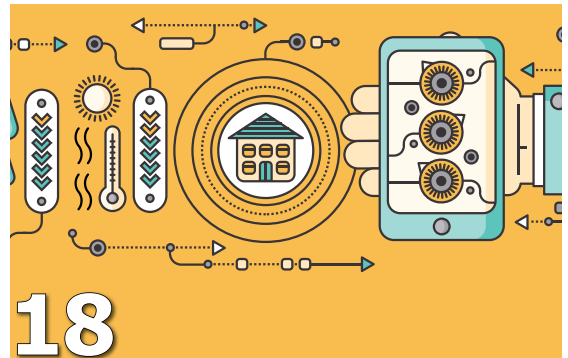
Our specialized target audiences prefer **New-Tech Europe** because they know that our publications are a reliable source of the latest information in their respective fields. Our multidimensional editorials, news items, interviews and feature articles provide them with a full, well-rounded picture of the markets in which they operate - an essential asset for every technological leader striving to stay ahead, make the right decisions, and generate the next global innovation.

Moreover, as an attractive platform for advertisers from around the world, **New-Tech Europe** has become a hub for bustling international commercial activity. Here, through ads and other promotional materials, Israeli readers obtain crucial information about developers and manufacturers worldwide, finding the tools, instruments, systems and components they need to facilitate their innovative endeavors.

Targeting the needs of both the global and european industries and global advertisers, **New-Tech Magazines Group** constantly expands and upgrades its services. Over the years, the company has been able to formulate a remarkably effective, multi-medium mix of offerings, combining magazine publications with useful online activities, newsletters and special events and exhibitions.

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Latest News

Eight projects have been awarded 20 million in funding to develop the next generation of autonomous vehicles

Eight new projects have been awarded £20 million in funding to research and develop enhanced communication between vehicles and roadside infrastructure or urban information systems, including new 'talking car technologies', Business Secretary Sajid Javid will announce on a visit to the autonomous vehicles test bed in Nuneaton.

The projects are the first to be funded from the government's £100 million Intelligent Mobility Fund. They range from developing autonomous shuttles to carry visually-impaired passengers using advanced sensors and control systems, to new simulation trials for autonomous pods to increase uptake and improve real-world trials.

Trials to test driverless cars on the streets are currently being worked on in Bristol, Coventry and Milton Keynes, and Greenwich. Autonomous vehicles are also being used in Heathrow to shuttle passengers, although these are currently on designated tracks.

The UK has a rich fabric of scientists and engineers who have established the UK as pioneers in the research and development of connected and autonomous vehicles. Today's funding will help strengthen the UK as a global centre for the fast-growing intelligent mobility market, estimated to be worth £900 billion per year globally by 2025.

Business Secretary Sajid Javid said:

Our cars of the future will be equipped with the technologies that will make getting from A to B safer, faster, and cleaner. They will alert drivers of accidents ahead and be able to receive information from their surroundings about hazards, increasing the safety of drivers, passengers and pedestrians.

Britain is a world-leader in research and development in such innovative technologies which improve lives and create opportunity for all. That is why this government has protected the £6 billion science budget and is providing up to £20 million for these projects.

Chris Reeves, Commercial Manager, Future Transport Technologies and Intelligent Mobility at HORIBA MIRA, said:

All the projects have received financial backing from industry in addition to government funding, and are backed by leading automotive businesses, engineering firms, IT specialists, universities and local authorities. The UK Connected Intelligent Transport Environment (UKCITE) project, which the Business Secretary will visit today, includes HORIBA MIRA, Jaguar Land Rover, Siemens, and Vodafone Group amongst others. He will also see demonstrations and simulations of the Flourish and Move UK projects.

Future Electronics moves to new regional headquarters premises in Muenchen, Germany



Ole Gerkenmeyer, Future Electronics' Regional Sales Director, Central Europe

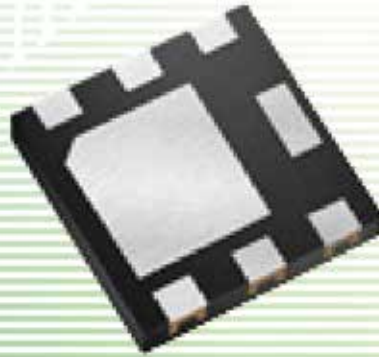
New office provides more floor space and better facilities to support Future Electronics' expansion in the central Europe region

Future Electronics, founded in 1968 by company president Robert Miller and now a world-class leader and innovator in the distribution and marketing of electronics components, today officially opened the new headquarters for its Central Europe region, in Muenchen, Germany.

The move to a new, bigger office complex near the site of the Messe Muenchen exhibition halls provides Future Electronics with space to accommodate its growing workforce. The Central Europe division of Future Electronics, which includes the D/A/CH countries and The Netherlands, is in the middle of an expansion programme as it gears up to support growing numbers of customers and an [▶](#)



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- Low ESD Clamping Voltage
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

The NIS/NIV1161 is designed to protect high speed data lines from ESD as well as short to vehicle battery situations. The ultra-lowcapacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines while the low RDS(on) FET limits distortion on the signal lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB and LVDS protocols

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Latest News

expanded line-up of suppliers.

The increased floor space available in the new office at Aschheim-Dornach will allow Future Electronics to accommodate more specialist engineers dedicated to fast-growing market and technology segments such as connectivity, LED lighting and power electronics. In addition, the modern office complex provides excellent communications facilities and a suitable configuration for the larger customer-service operation that Future Electronics is establishing in Muenchen. This comes in response to rising demand from manufacturers in Germany, Austria, Switzerland and The Netherlands for Future Electronics' advanced logistics and inventory management

programmes, which can provide customers with the assurance of next-day availability of their entire electronics materials requirement.

Ole Gerkenmeyer, Regional Sales Director for Central Europe at Future Electronics

Ole Gerkenmeyer, Future Electronics' Regional Sales Director for Central Europe, said: 'Central Europe is possibly the most competitive region for electronics component distribution in the world. Future Electronics' new, larger regional headquarters is going to help us continue to succeed by keeping our levels of customer service and engineering support ahead of our competitors' while serving a growing customer base.'

Intel and Qualcomm collaborate to build robust 802.11ad ecosystem

802.11ad represents an important step in the evolution of Wi-Fi, enabling new user capabilities such as wire-equivalent docking and high-quality, low-latency video streaming, multimedia kiosks, while bringing a step increase in network capacity, and much more.

We are excited to announce that Qualcomm Atheros and Intel have reached a crucial milestone in making 802.11ad WiGig* a mainstream and widely available technology. Intel and Qualcomm Atheros have successfully demonstrated multi-gigabit interoperability between our companies' respective 802.11ad WiGig solutions. This milestone will help pave the way for industry development of 802.11ad WiGig devices that can communicate and connect seamlessly with each other at amazing speeds of up to 4.6 Gbps [1]. Moreover, this milestone underscores both companies' commitment to the strong evolution of Wi-Fi, both infrastructure and peer-to-peer communications, as well as the critical role 802.11ad WiGig plays in this evolutionary process.

Laptops, tablets, smartphones, access points, storage devices, untethered VR glasses and other 802.11ad WiGig-capable devices offer multi-gigabit speeds, high density, low latency and very high network capacity, as well as empower a new class of applications and services. 802.11ad will transform the experience of Wi-Fi users, be it in their offices, homes or even in public places. Bringing the vast, new spectrum in 60 GHz band to Wi-Fi's fold, 802.11ad will be one of the potent tools to address burgeoning data

demand in homes, enterprises and carrier networks.

Qualcomm Atheros and Intel engineers worked collaboratively for months in each other's labs, running countless tests, culminating in this achievement. These tests spanned across many use cases and scenarios, including peer-to-peer connections between Intel and Qualcomm Atheros 802.11ad WiGig based clients and Qualcomm Atheros 802.11ad WiGig powered access points (wireless routers). Tests examined various cases and conditions—from device discovery and connection to full-blown data uploads and downloads, streaming and more. As part of the testing, we successfully achieved multi-gigabit real data throughput between our devices.

Achieving full interoperability is not easy. This level of collaboration and focused effort is essential in creating new markets and building a robust ecosystem, and in ultimately providing seamless user experience across multi-vendor devices.

While more work lies ahead, our collaboration lays the groundwork for a large ecosystem of interoperable commercial 802.11ad products across networking, mobile and computing segments. We are excited about the new capabilities 802.11ad enables—from 4K display connectivity to tri-band (2.4 GHz, 5 GHz and 60 GHz) Wi-Fi networking and high-speed cellular offload—and we think you should be excited at our progress in bringing these capabilities to your favorite devices.



Latest News

New chip fabrication approach

Depositing different materials within a single chip layer could lead to more efficient computers.

Today, computer chips are built by stacking layers of different materials and etching patterns into them.

But in the latest issue of *Advanced Materials*, MIT researchers and their colleagues report the first chip-fabrication technique that enables significantly different materials to be deposited in the same layer. They also report that, using the technique, they have built chips with working versions of all the circuit components necessary to produce a general-purpose computer.

The layers of material in the researchers' experimental chip are extremely thin - between one and three atoms thick. Consequently, this work could abet efforts to manufacture thin, flexible, transparent computing devices, which could be laminated onto other materials.

The technique also has implications for the development of the ultralow-power, high-speed computing devices known as tunneling transistors and, potentially, for the integration of optical components into computer chips.

Ling and Lin are joined on the paper by Mildred Dresselhaus, an Institute Professor emerita of physics and electrical engineering; Jing Kong, an ITT Career Development Professor of Electrical Engineering; Tomás Palacios, an associate professor of electrical engineering; and by another 10 MIT researchers and two more from Brookhaven National Laboratory and Taiwan's National Tsing-Hua University.

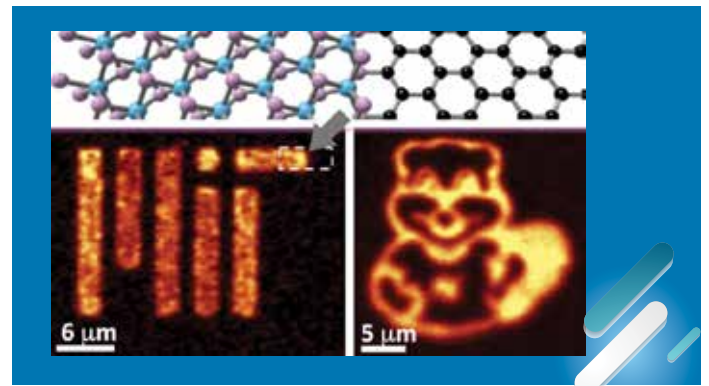
Strange bedfellows

Computer chips are built from crystalline solids, materials whose atoms are arranged in a regular geometrical pattern known as a crystal lattice. Previously, only materials with closely matched lattices have been deposited laterally in the same layer of a chip. The researchers' experimental

chip, however, uses two materials with very different lattice sizes: molybdenum disulfide and graphene, which is a single-atom-thick layer of carbon.

Moreover, the researchers' fabrication technique generalizes to any material that, like molybdenum disulfide, combines elements from group six of the periodic table, such as chromium, molybdenum, and tungsten, and elements from group 16, such as sulfur, selenium, and tellurium. Many of these compounds are semiconductors - the type of material that underlies transistor design - and exhibit useful behavior in extremely thin layers.

Graphene, which the researchers chose as their second material, has many remarkable properties. It's the strongest known material, but it also has the highest known electron mobility, a measure of how rapidly electrons move through it. As such, it's an excellent candidate for use in thin-film electronics or, indeed, in any nanoscale electronic devices. To assemble their laterally integrated circuits, the researchers first deposit a layer of graphene on a silicon substrate. Then they etch it away in the regions where they wish to deposit the molybdenum disulfide. Next, at one end of the substrate, they place a solid bar of a material known



Nokia and Deutsche Telekom show how XG-FAST technology can extend copper network speeds and meet future data demands

Espoo, Finland – Nokia has completed a laboratory trial with Deutsche Telekom that has demonstrated how XG-FAST, a new fixed ultra-broadband access technology, can be used by service providers to meet ever-growing demands for high-quality Internet services delivered over their existing copper networks. The lab trial was conducted end of 2015

by Nokia's subsidiary Alcatel-Lucent.

XG-FAST is a Bell Labs-developed extension of Nokia's commercially available G.fast technology. The trial conducted at Deutsche Telekom's cable laboratory in Darmstadt, Germany, generated data throughput speeds of more than 10 gigabits-per-second (Gbps), [→](#)



Latest News

approximately 200 times faster than speeds in the average residential broadband connection today. In providing fiber-like speeds, the copper-based technology could enable a two-hour HD movie to download in less than 10 seconds, or for 1,000 photos to be uploaded in less than two seconds. Deutsche Telekom's network – which uses VDSL2 Vectoring as well as fiber-to-the-home (FTTH) technology – currently offers customers access speeds of up to 100 megabits-per-second (Mbps). In enabling Deutsche Telekom to make efficient use of its existing copper network infrastructure, the innovative XG-FAST technology could also enable it to deliver further on commitments to Germany's national broadband targets for providing more bandwidth to more people.

Key Facts:

Technologies such as G.fast and XG-FAST use the last section of existing copper networks to deliver fiber-like speeds to homes and offices. XG-FAST is in the early stages of lab testing, but has exceeded expectations in trials with several customers so far.

The XG-FAST trial with Deutsche Telekom demonstrated an aggregated bandwidth exceeding 11Gbps on two bonded pairs of Category 6 cable at 50 meters in length. Similar

tests using standard drop cable illustrated the feasibility of XG-FAST for fiber-to-the-front door applications, achieving aggregate rates that exceed 8Gbps over 50m. All trials were performed using prototype equipment from Bell Labs under laboratory conditions.

XG-FAST is also capable of delivering 1Gbps symmetrical services at distances of 70m enabling operators to deliver fiber-like speeds inside buildings using existing telephone lines, eliminating the need to install new cabling. This allows for faster installation times and less hassle for the end-user.

Nokia's fixed ultra-broadband access portfolio offers service providers a comprehensive mix of fiber and copper access technologies to suit the needs of any deployment.

Bruno Jacobfeuerborn, CTO of Deutsche Telekom, said: "Working on this demonstration we can see the future possibilities of XG-FAST in maximizing existing assets. This will provide another technology option which could enable us to offer high-speed connectivity to our customers quickly and cost-effectively, and at the same time, move our fiber infrastructure closer to our customers."

New toolbox to help boost and secure European electricity networks

EU researchers have created an innovative toolbox in order to ensure the safety and continued security of European electricity networks, and to help facilitate a greater shift towards renewable energy sources

The EU-funded UMBRELLA project has unveiled its key successes and deliverables during a one-day workshop in Brussels on 26 January 2016. This included the creation of a toolbox prototype for Transmission System Operators (TSOs) to guarantee secure grid operation in future electricity networks with a high penetration of intermittent renewable energy sources (RES).

The toolbox enables TSOs to act in a coordinated European target system where regional strategies converge to ensure the best possible use of the European electricity infrastructure.

There is a growing contribution of less predictable and more variable RES, which is taking place alongside the gradual integration of national markets into one common

European electrical energy market. Market mechanisms are increasingly not being able to cover certain aspects of system security, leading to high deviations between scheduled and physical flows in terms of time, direction and volume.

As a consequence, meteorological forecasting errors may lead to unforeseen violations of operating limits and trigger cascading outages in stressed-system situations.

This results in the need for more complex operational planning and transmission operation, taking the network closer to its operational limits.

The UMBRELLA toolbox

The UMBRELLA toolbox includes a deterministic and probabilistic optimisation framework for corrective actions to cope with simulated risks on different timescales and increasing system complexity. The overall aim of this is to reduce the total cost of uncertainty whilst also increasing system security and transmission capacity.



Latest News

Project Skybender: Google's secretive 5G internet drone tests revealed



New Mexico Spaceport Authority, Mark Harris

Trials at New Mexico's Spaceport Authority are using new millimetre wave technology to deliver data from drones - potentially 40 times faster than 4G.

The flight control centre New Mexico Spaceport Center where Google has been testing solar-powered drones. The flight control office at the New Mexico Spaceport Center where Google has been testing solar-powered drones. Google is testing solar-powered drones at Spaceport America in New Mexico to explore ways to deliver high-speed internet from the air, the Guardian has learned.

In a secretive project codenamed SkyBender, the technology giant built several prototype transceivers at the isolated spaceport last summer, and is testing them with multiple drones, according to documents obtained under public records laws. In order to house the drones and support aircraft, Google is temporarily using 15,000 square feet of hangar space in the glamorous Gateway to Space terminal designed by Richard Foster for the much-delayed Virgin Galactic spaceflights.

The tech company has also installed its own dedicated flight control centre in the nearby Spaceflight Operations Center,

separate from the terminal.

Based out of the site near the town called Truth or Consequences, Project SkyBender is using drones to experiment with millimetre-wave radio transmissions, one of the technologies that could underpin next generation 5G wireless internet access. High frequency millimetre waves can theoretically transmit gigabits of data every second, up to 40 times more than today's 4G LTE systems. Google ultimately envisages thousands of high altitude "self-flying aircraft" delivering internet access around the world.

However, millimetre wave transmissions have a much shorter range than mobile phone signals. A broadcast at 28GHz, the frequency Google is testing at Spaceport America, would fade out in around a tenth the distance of a 4G phone signal. To get millimetre wave working from a high-flying drone, Google needs to experiment with focused transmissions from a so-called phased array.

The SkyBender system is being tested with an "optionally piloted" aircraft called Centaur as well as solar-powered drones made by Google Titan, a division formed when Google acquired New Mexico startup Titan Aerospace in 2014. Titan built high-altitude solar-powered drones with wingspans of up to 50 metres.

Emails between Spaceport America and Google project managers reveal that the aircraft have exclusive use of the Spaceport's runway during the tests and will even venture above the neighbouring White Sands Missile Range.

Google spent several months last summer building two communication installations on concrete pads at Spaceport America. Project SkyBender is part of the little-known Google Access team, which also includes Project Loon, a plan to deliver wireless internet using unpowered balloons floating through the stratosphere.

Anderson expects Virgin Galactic to unveil its new SpaceShipTwo at the Spaceport in February, and to begin flights there in 2018. Google declined to comment.

22 Student Teams Will Test Pod Design at SpaceX Hyperloop Test Track

Twenty-two student teams are heading to California this summer to test their design prototype at the world's first Hyperloop Test Track. More than 115 student engineering teams representing 27 U.S. states and 20 countries were at Texas A&M University in College Station, Texas, this weekend participating in SpaceX's Hyperloop Pod Competition Design Weekend.

The teams presented their plans for the overall pod design and were judged on a variety of criteria including

innovation and uniqueness of design; full Hyperloop system applicability and economics; level of design detail; strength of supporting analysis and tests; feasibility for test track competition; and quality of documentation and presentation.

The Top 5 student teams for the design and build category were:

Best Overall Design Award

MIT Hyperloop Team, Massachusetts Institute of 



Latest News

Technology

Pod Innovation Award

Delft Hyperloop, Delft University of Technology (The Netherlands)

Pod Technical Excellence Award

Badgerloop, University of Wisconsin-Madison

Pod Technical Excellence Award

Hyperloop at Virginia Tech, Virginia Tech

Pod Technical Excellence Award

HyperXite, University of California Irvine

"Congratulations to the finalists and all the student teams who competed in the first-ever SpaceX Hyperloop Pod Competition," said John Sharp, chancellor of The Texas A&M University System. "I am especially proud of Aerospace Hyperloop, a finalist representing Texas A&M University and its world-class engineering program in the next round."

"World-changing events such as this do not happen often, so to be able to say one took place at Texas A&M is truly special," said Michael K. Young, president of Texas A&M.

"It is our hope that everyone who participated uses the momentum from this historic meeting of young innovators to go out into the world and continue to create and innovate. This weekend's competition proves the future is in very good hands with such an inspiring and talented group of young people, many of whom are right here at Texas A&M. Congratulations to all the young men and women and their teams headed to California and that certainly includes Texas A&M's Aerospace Hyperloop team."



the nRFready Smart Remote 3

"The future of engineering was on display this weekend in College Station," said M. Katherine Banks, vice chancellor and dean of Texas A&M Engineering. "We challenge our students to step outside their comfort zones and approach engineering problems in novel ways. The young men and women at this competition definitely accomplished that, and presented design and technical concepts that were well beyond anyone's expectations."

Technical awards were also awarded to student teams whose designs displayed outstanding technical merit in subsystem and design.

first SpaceDataHighway Laser Relay in Orbit



EDRS-A liftoff

The European Data Relay System's first laser terminal has reached space aboard its host satellite and is now under way to its final operating position.

EDRS-A was launched on 29 January as part of the Eutelsat-9B telecom satellite at 22:20 GMT atop a Proton rocket from Baikonur, Kazakhstan.

EDRS is ESA's most ambitious telecom programme yet, taking the form of a public-private partnership between ESA and Airbus Defence and Space, with Airbus operating

the service and the DLR German Space Administration funding the development of the laser terminal.

Dubbed the 'SpaceDataHighway', EDRS will revolutionise satcoms as Europe's first optical communication network, capable of relaying user data in near-real time at an unprecedented 1.8 Gbit/s.

Normally, low-orbiting satellites must come within view of a ground station before they can send their information to Earth. EDRS instead collects their information from its higher, geo-stationary position via laser and immediately relays it to the ground, dramatically improving access to time-critical and potentially life-saving data.

ESA, Airbus and DLR will in a few days begin testing EDRS-A's general health and performance, working with the EDRS ground stations in Germany, Belgium and the UK.

Test links to its first customers, the European Commission's Copernicus Sentinel satellites, will then be carried out over several weeks for the service to begin this summer. Data relay for the International Space Station will start in 2018.



Latest News

Ericsson opens 20,000 square meter Global ICT Center in Sweden to drive innovation

Ericsson (NASDAQ: ERIC) has officially inaugurated its Global Information and Communication Technology (ICT) Center in Rosersberg, Sweden. The purpose-built, highly scalable and sustainable facility reflects Ericsson's ongoing commitment to R&D investment both in Sweden and globally. The center also represents an important step in the company's ongoing ICT transformation journey. The Rosersberg site, which covers 20,000 square meters, is the first purpose-built Ericsson Global ICT Center to be inaugurated in Sweden. It follows the opening of the Global ICT Center in Linköping, Sweden in September 2014, which was built adjacent to an existing Ericsson facility. In addition to the two facilities in Sweden, Ericsson will open a Global ICT Center in Montreal, Canada in the second quarter of 2016. The Global ICT Centers allow Ericsson to emulate an operator's mobile network and to test new solutions as if they were running on a live network. In the near future, Ericsson's customers will be able to connect remotely for interoperability testing, trials, early access

and innovation on new offerings from any location. These services will be provided through ten Business-Near Centers, to be announced in 2016, which are connected to the Global ICT Centers.

The Global ICT Centers are set to be powered by Ericsson's cloud solutions and will host a substantial part of the company's product portfolio. As a result of this extensive rationalization and virtualization effort, Ericsson will be able to shorten innovation cycles and increase global collaboration while also reducing R&D costs. Currently, the company's test environments are spread across more than 50 locations worldwide. Ericsson's Global ICT Centers are an important step toward achieving the company's sustainability goals. The cutting-edge design of the centers, combined with modular and scalable construction, secures efficient use of energy and space. Ericsson estimates, when all three Global ICT Centers are in operation, it will result in a 40% reduction in energy usage compared to 2012 test lab energy baseline.

100 operators adopt Ericsson Radio Dot System to improve indoor app coverage

Latest customer marks major milestone for the innovative indoor small cell solution, commercially shipping since the fourth quarter in 2014 - 44 percent in Europe, Middle East & Africa, 39 percent of Radio Dot System operators are in Asia Pacific Region, 17 percent in North and South America 77 percent of Radio Dot Systems have gone live with LTE - almost 10 percent of those support dual-mode LTE and WCDMA on the same Dots.

About 90 percent of our time is spent indoors. However, results from an Ericsson (NASDAQ: ERIC) ConsumerLab survey reveal that only three in 10 smartphone users find indoor voice quality, coverage and reliability to be good. The challenge will be exacerbated by the 11 times growth in smartphone traffic forecast from 2015 to 2021, with around 90 percent of mobile data traffic expected to come from smartphones by the end of 2021.

To improve indoor app coverage for mobile consumer and business customers, leading operators around the world have adopted the Ericsson Radio Dot System, an innovative indoor small cell solution commercially introduced in the last quarter of 2014. Recently, Sichuan Mobile, the largest mobile communications operator in western China, became the 100th mobile operator worldwide to adopt the Ericsson Dot System. The Radio Dot System is designed to enable mobile operators



to deliver consistently high-performance voice and data coverage and capacity in the broadest range of buildings. The system features the iconic Radio Dot, a sleek, ceiling-mounted antenna element that provides high-performance app coverage throughout the building and seamless mobility with the outdoor mobile network. The system is remote software-upgradable, with recent commercial software upgrades, Networks Software 16A, supporting up to 600Mbps peak rates using LTE-Advanced Carrier Aggregation, while reducing power consumption of the already-energy-efficient system. Ericsson Radio Dot System supports the same software as the operator's outdoor macrocell network, ensuring a seamless user experience and faster time to market for new performance and efficiency-enhancing capabilities.



Making Smart Home Sensors Tell Us More

> By European Editors

Contributed By Publitek Marketing Communications

Hollywood action movies like *Ocean's Eleven* and *Mission Impossible* have demonstrated numerous elaborate means of detecting intruders who are up to no good. Ultra-agile black-clad raiders make for great cinema, outsmarting pressure mats, laser fields, thermal cameras and other fiendish devices. In the real world, in countless homes and offices, a passive infrared sensor winking away in the corner of the room is often considered enough to dissuade the opportunistic burglar. The PIR is regarded by homeowners and security companies as being the intruder-detection technology best suited to domestic applications: economical, reliable, adjustable to tune-out false alerts, the PIR is the incumbent presence-detection technology of choice.

The enduring favorite

PIR manufacturers have evolved their sensors to overcome the known

weaknesses of infrared sensing technology. The sensors depend on a temperature differential between the target and background, and also require the target to be moving, in order to detect presence. To minimize these effects, sensors in the Panasonic MP series, such as the AMN11112, integrate four receptors for precision detection of even small movements. The receptors are sensitive to small temperature differences, which ensure accurate detection even in hot climates where ambient temperatures can be close to human body temperature.

Panasonic has also miniaturized its receptors, to ensure high sensitivity and accuracy from small units fitted with small lenses. A high level of integration, with a built-in amplifier, passive components, optical filter and electromagnetic shielding (Figure 1), simplifies design and enhances reliability. Constant evolution has ensured the PIR sensor remains a

favorite of security-system designers.

Smart building demands more

Now that the age of the smart home has dawned, however, people are expecting sensors such as PIRs not only to support intruder detection but also to help automate the control of lighting, heating and other services by monitoring room occupancy. Some of the known characteristics of PIR sensing become weaknesses in this context. Since the sensor relies on detecting changes in the observed thermal scene, the target has to move in order to be detected. This is acceptable in a security system, because an intruder can be assumed to likely move around inside the house having gained access. Homeowners and their guests, on the other hand, may sit still for long periods in a room, for example if talking or watching a film. The system should not incorrectly determine that the



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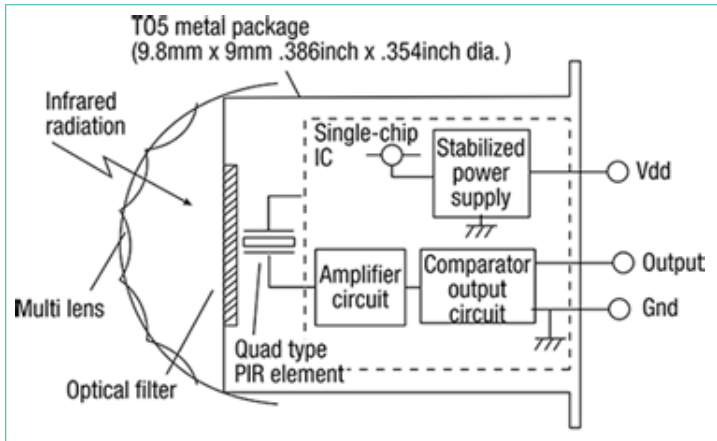


Figure 1: Greater integration and sensitivity have kept PIR sensors at the top of designers' wish lists

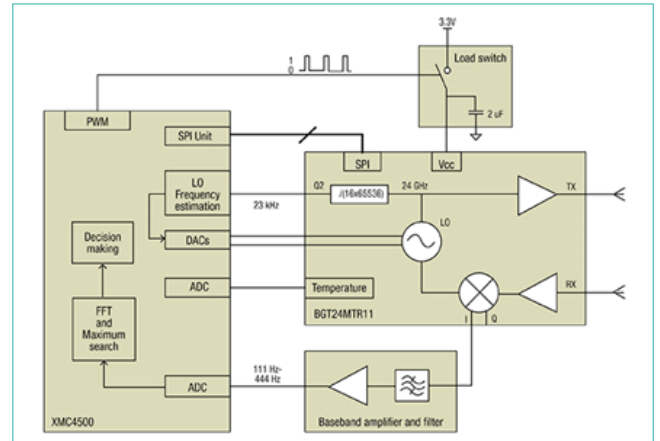


Figure 2: Pulsed-mode Doppler radar for indoor occupancy monitoring applications

room is unoccupied and begin turning off services such as lights or heating. In addition, smart home services of the future may be dependent on gathering more detailed information about the occupant, such as their exact location in the room. This could allow the system to automatically optimize the lighting in a localized area – over a desk or kitchen work surface, for example – while dimming the remainder of the room lighting for optimum energy efficiency.

Smarter occupancy sensing can also help with services such as assisted living, as today's ageing populations seek to live independently and safely in their own homes later into life. Younger relatives are often unable to act as full-time caregivers, and professional care is expensive. Automated supervision can provide a means of detecting whether an elderly homeowner needs assistance, allowing caregivers or emergency services to be alerted quickly.

Today's PIR sensors, as well evolved as they are, are not able to capture the amount of detail needed to drive services such as these. A number

of alternative sensing techniques are available. Video-based sensing, for example, could be used to allow caregivers to check periodically that an elderly person is safe at home, or to determine the exact location of an occupant in a room. Indoor video surveillance is not a desirable solution, however, for reasons of privacy. Partial surveillance may be considered, or video may be discarded after analysis, but still homeowners may feel generally uncomfortable.

Single-chip radar solution

In recent years, radar-based sensing technology has begun to enter consumer-related markets. One example is in automotive driver-assistance systems such as collision avoidance. Low-power radar transmitters working in the unlicensed 24 GHz ISM frequency range are now available at a cost that can be considered acceptable in the smart-home/smart-building market. The principles of detecting presence by monitoring reflected radio waves, and measuring distance by timing the return journey of the transmission,

were first developed around the beginning of the 20th century.

A 24 GHz radar transceiver IC such as the Infineon BGT24MTR11 can be used to build a low-power sensor suitable for indoor occupancy detection. Radar technology enables advanced capabilities such as detecting non-moving occupants, determining the exact location of the occupant, and sensing the direction of any motion. As a further advantage of using radar technology in a domestic setting, the transmitter and sensor do not need an unimpeded line of sight to the target and hence can be positioned in an unobtrusive location. This could be behind lightweight building materials, such as ceiling tiles, hence allowing the sensor to be placed out of sight. The BGT24MTR11 integrates one transmit and one receive channel, as needed for detecting occupancy and the speed and direction of motion, in a single device that requires only a small number of external capacitors to complete a fully operational circuit. This not only saves board space, but also eliminates RF matching challenges. If the system is required

to sense the occupant's location, two receivers are needed. The BGT24MTR12, which integrates two receive channels and one transmitter, is ideal for this purpose.

Design for low power operation

With maximum RF output power of 15 dBm, the BGT24MTR11 is safe to use in the ISM band. The total IC power consumption of 528 mW in continuous mode with maximum transmit power is able to be reduced significantly by applying a duty-cycling scheme that turns off the power supply to the chip in between measurements. Based on the measurement times needed to detect Doppler shift at low target speeds, activating the IC for only 10 ms in every 0.5 seconds allows target speeds of up to about 25 km/h to be

measured with resolution of about ± 1 km/h. This is adequate for typical indoor sensing applications, and reduces power consumption to only 12 mW per cycle.

Figure 2 shows how the radar IC is used in conjunction with the Infineon XMC4500 microcontroller, which programs the BGT24MTR11 registers through the SPI port, monitors the VCO frequency and controls the VCO tuning voltages via its on-chip DACs, and controls a load switch responsible for turning off the power to the BGT24MTR11 in between measurement cycles. As the diagram shows, only a small number of key components are required to complete the design.

Conclusion

As the smart building revolution

gathers pace, new applications and services will require more detailed information describing the activities inside homes and buildings. Enhanced occupancy sensing technologies are needed to capture this information without compromising privacy. Radar-based sensing in the 24 GHz ISM frequency band is safe, discrete, and can now be achieved more easily than ever before by taking advantage of the latest single-chip transceivers that significantly simplify system design. Power-saving techniques have been demonstrated that enable designers to create low-maintenance sensors for indoor use that consume an average power of only 10 mW.



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Why Choose Embedded Multiradio Solutions for M2M and IoT Applications?

› Pelle Svensson, U-blox

During the last few years, integrated circuit vendors have released various multiradio devices that offer two or more wireless technologies in one physical package. This has led to the development of multiradio modules that typically include Classic Bluetooth, Bluetooth low energy and Wi-Fi. Multiradio solutions enable product innovation for the Internet of Things (IoT) in many and varied applications including telematics, usage-based insurance, manufacturing, connected cities, healthcare, asset management, building and home automation, security systems and smart energy. Multiradio devices reduce size, implementation cost and final product cost but, aside from these rather obvious benefits, there are many others. Pre-certified modules will reduce the time and effort involved in securing type approval from the various radio regulatory authorities for

the finished product. The complexities of wireless co-location, where several antennas operate in close proximity within the same small device, are already taken care of too.

Also, multiradio devices permit a single physical implementation for a range of products. They can make use of external technology discovery and proximity detection, perhaps via Bluetooth low energy beacons, and they can be used as cost-effective and compact gateways for the IoT.

Why size matters

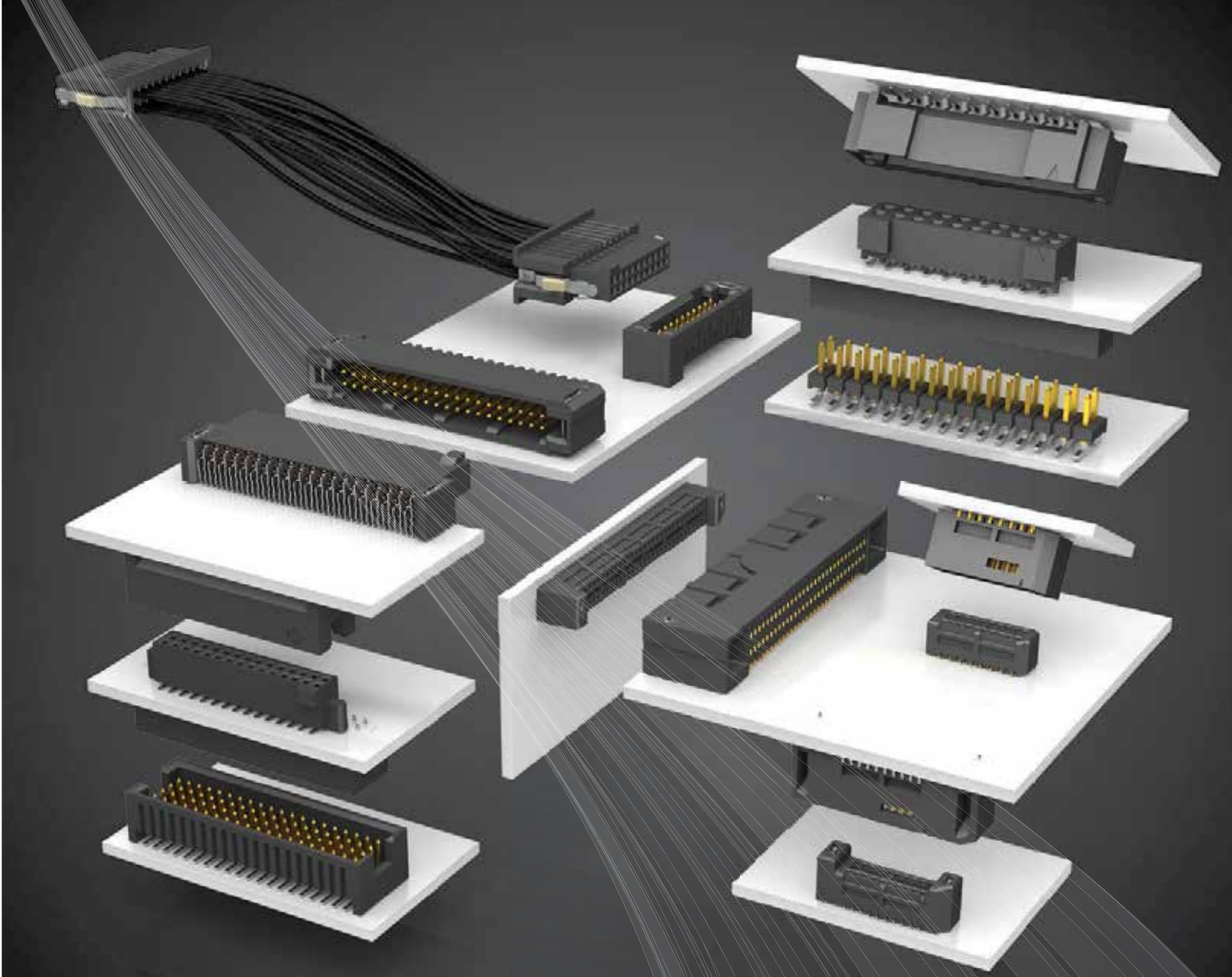
Smartphone manufacturers are particularly focused on reducing the size and cost of their products. Handsets need to integrate several wireless protocols (in addition to the cellular) to fulfill their goals of being multi-tasking units: Classic Bluetooth, Bluetooth low energy, Wi-Fi (2.4 GHz and 5 GHz), FM radio, satellite navigation and, in some recent models,

NFC. Instead of embedding several discrete radios, possibly from different vendors, designers can dramatically reduce the wireless implementation size and cost by adopting a single multiradio solution instead. Printed circuit board size, complexity and cost are all reduced too.

Lowering the cost of both implementation and the final product

Multiple discrete radios mean more components, more circuit board real estate and more testing. There are many fewer external components in a multiradio. Multiradio modules may also include LNAs (low-noise amplifiers), antenna matching components, oscillators, crystals and more components that would otherwise be external to the radio device.

Most multiradio solutions also implement a common antenna



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interface so fewer components are required, for example those for antenna matching. Some even have an integrated antenna, either as primary radiator or as a backup if an external antenna is damaged or becomes disconnected. The more components that a printed circuit board has to carry, the more complex and expensive it becomes. Using a multiradio solution contributes to simplicity and will not only enable smaller boards to be used but may facilitate using boards with fewer layers, which can result in considerable cost savings.

One implementation - several radio options for the user

The overall cost savings from using multiradio solutions make it economical to implement this design strategy across a product range, even when different products will eventually use only one of the available wireless protocols. For example, you may want to offer Bluetooth or Wi-Fi versions of a product, rather than one that's designed for both.

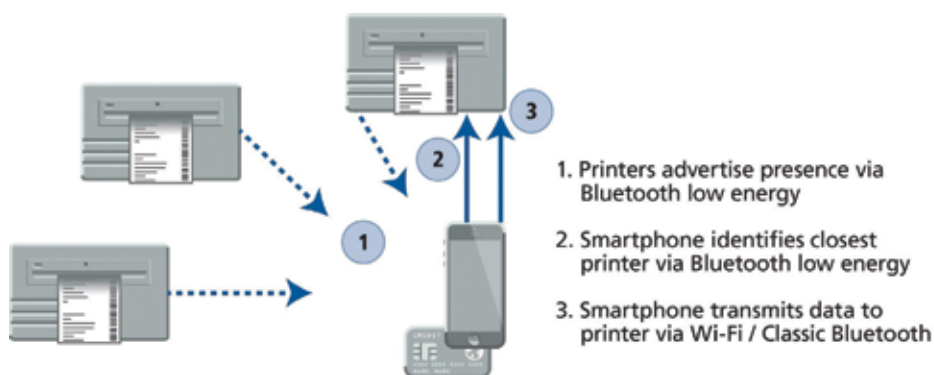
The approach is particularly useful with a range of products that use a common architecture, and perhaps a common main printed circuit board for all the variants. Even if one of the products in the range only uses one of the wireless technologies, the implementation and maintenance is minimized for the entire product range.

External technology discovery and proximity detection

There is often a requirement for two wireless-enabled devices to connect automatically when they come within range of each other. Sometimes one radio technology is used for device service discovery and another for data exchange.

One of the wireless technologies frequently implemented in multiradio solutions is Bluetooth low energy. With its unique radio service discovery, Bluetooth low energy becomes particularly useful in multiradio implementations. The protocol can be used to detect a user or device when the signal close to another device, effectively acting as a proximity beacon. Once detected, a second radio technology can be used for the data exchange if higher bandwidth is required.

For example, in a retail point-of-sale environment, Bluetooth low energy signals may advertise the presence of the nearest receipt printer to a hand-held payment terminal. The connection set up and data transfer could then take place over Classic Bluetooth or Wi-Fi.



In this use case only one of the radio technologies is being used at a time.

Wireless coexistence

Some systems require wireless technologies to be operating concurrently. There is potential signal interference in these circumstances, resulting in higher latency because of the need to use packet traffic arbitration to avoid simultaneous data transmission and reception, or even data loss due from receiver input saturation.

These potential side effects are clearly unacceptable in mission-critical industrial and medical applications so it's important to optimize coexistence of the various wireless technologies to ensure interference-free operation.

Using multiple single-technology radios means that longer development time is needed to deal with with the coexistence issue, adding to cost and extending time-to-market for the end product.

In a stand-alone multiradio device, coexistence is handled within the multiradio chip, eliminating these challenges.

Minimizing type-approval effort

Implementing several single-radio solutions in a product requires extra regulatory testing. Even if a single wireless module has obtained modular regulatory approval, additional testing and reporting will be required when integrating additional radio modules into the device. This once again extends time-to-market, adds development cost, adds test facility cost, and increases technical risks. With a stand-alone multiradio module these problems are avoided.

Multiradio solutions - ideal for gateways

A wireless gateway is a networking device that routes packets from

a wireless device to the network. Gateways can combine the functions of a wireless access point and router, and often provide firewall security too. These converged devices save desk space and simplify wiring - one device replaces two. A gateway can also act as protocol converter for the installed base's devices and transfer the converted data upstream using the new Internet data formats including RESTful, XMPP and MQTT.

Multiradio solutions are particularly suitable when there is a need for different wireless technologies to connect devices in a gateway configuration. One technology is used to communicate downstream to sensors and actuators. A second radio communicates with existing networks upstream.

Consider the example of a medical device such as an infusion pump. Bluetooth low energy may be used with a handheld scanner to ensure that the pump is being connected to the right patient and that the correct medication is being administered. This connection carries very little data but within the same pump a Wi-Fi link may be used to provide a higher bandwidth connection for sending continuous monitoring data over a hospital network.



Using different technologies downstream and upstream is also ideal when a number of battery powered sensors require low power wireless communication

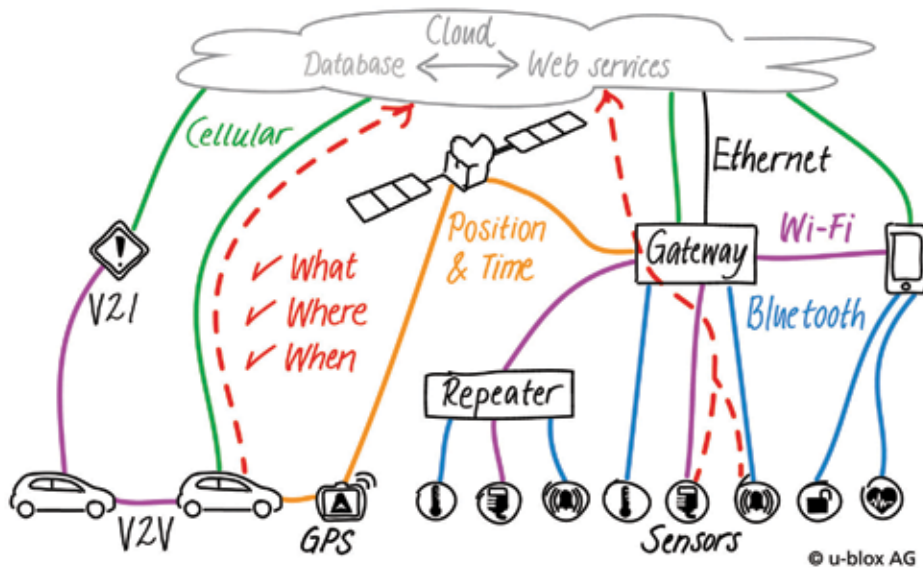
and you then want up-stream connectivity to existing infrastructure, perhaps over Wi-Fi. For instance, you can use Bluetooth low energy to connect to sensors downstream and use Wi-Fi to transfer the sensor data upstream. The same technology can be used to extend geographical coverage using the Wi-Fi upstream link as a repeater. In this case, Wi-Fi is used to connect several Bluetooth low energy gateways in order to achieve greater coverage.

The u-blox ODIN-W262 is an example of a multiradio wireless module designed for the kinds of applications described above. The 14.8x22.3x4.5 mm module supports multiple, concurrent Wi-Fi (2.4 GHz and 5 GHz), Classic Bluetooth and Bluetooth low energy links for product design flexibility and is configured easily for individual applications using AT-commands. Radio type approved in countries throughout the world, it even has a built-in antenna to make adding multi-protocol wireless connectivity to any product as quick and easy as possible.

Enabling the Internet of Things

When the Bluetooth Core Specification added a standard means of creating a dedicated data channel for IPv6 the groundwork was laid for future IP connectivity. With the rapid market adoption of Bluetooth Smart (Bluetooth low energy) and the addition of IP connectivity, everything points to Bluetooth as one of the fundamental wireless links in the Internet of Things. The recent additions to the standard make it possible for Bluetooth Smart sensors to use IPv6, giving developers and OEMs the flexibility they need to ensure connectivity and compatibility.

u-blox = IoT Connectivity





System On Modules and Small Board Computer Make or Buy

› Amir Sherman, Arrow Central Europe GmbH

Definition of challenge - Should we make anymore?

The System on Module, which is sometimes referred to as a Computer on Module (CoM) or SBC (Small Board Computer), is designed to plug into a carrier, or base board, and is generally a small processor module with a CPU and standard I/O capability. The complex effort associated with designing a CPU subsystem is avoided by using SoM functionality and a custom base board.

What's inside the SoM (System On Module)?

- Application Processor from leading semiconductor companies such as Freescale, Texas Instruments, Atmel, Qualcomm, Altera
- Memories, both Flash (NAND/NOR)

and RAM (DDR2/3)

- WiFi/Bluetooth
- Gigabit Phy
- Audio Codec
- PMIC (Power Management IC)
- Touch Controller

And if you think about it, the SoM Block Diagram is very similar to (perhaps 70% the same as) a mobile phone or tablet.

Today this type of question is raised again and again in most of the development companies because the "Need for Speed" and the "Need for IoT" is part of every discussion. Almost every segment wants to add a "mobile phone" to its application and there are few companies in the world that know how to develop a good mobile phone (Apple, Samsung,

LG etc.) so the customers need to understand that they don't need to "Invent the Wheel" again.

A couple of years ago it was very popular to use this solution in low quantity projects - 100pcs to 500pcs per year - but lately, where the prices of processors based on ARM cores have become very cheap (because of the mobile and tablet market that made the core so cost competitive), customers are using the SoMs in 5000 and even 10000pcs per year projects or higher.

In this example, the calculation is for a microprocessor based design with a two Man Year NRE for hardware, software, and production test development, prototypes and debug and software maintenance for another

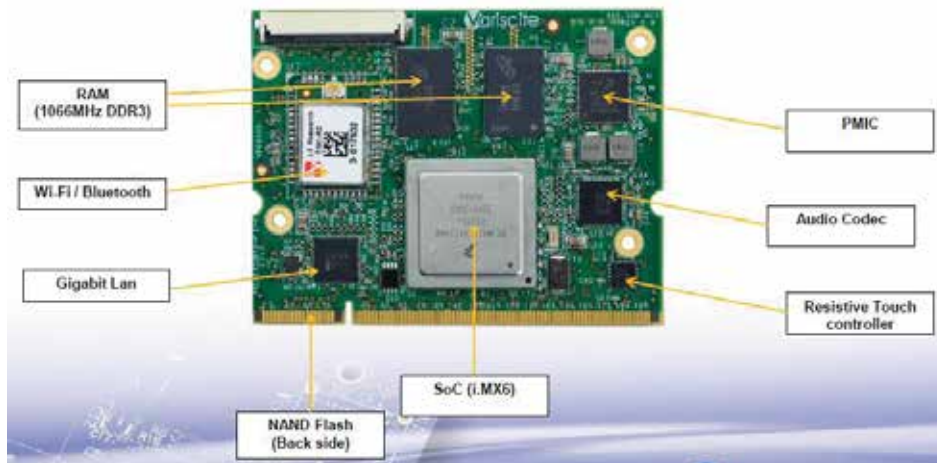
half year.

The cost per unit after this time is around \$40; compare this with using a SoM, where there is no development cost, prototyping and debugging and software maintenance costs nothing and the price for the unit is the same. Any concern that the hardware engineers think that they are not needed is unfounded because their focus should be on the application board, which is their IP (intellectual Property). They don't need to "invent the wheel" again with the processor board when they can get a working platform based on the latest processors in the market from Texas Instruments, Altera, Freescale, Qualcomm and Atmel. All these processors are based on the latest ARM cores from Cortex A5 to Cortex A8 and A9 as well as Cortex A7 and Cortex A57.

Status Quo of technology so far and existing approach

The SoM market can be divided in several ways:

1. Architecture : ARM and x86
2. Form Factor: ARM Based Solution for SMARC , Q7 or Proprietary (Others, like COM Express, are supported by x86 and not ARM based)



Picture Nu1 - Example of System On Module

3. Type of ARM core (Cortex A5, A7, A8, A9) and Example of SoM

4. Operating System Support: Linux, Android , Windows Embedded

1. Architecture: ARM and x86

- ARM - Most popular cores used in 90% of worldwide mobile phones and powerful embedded community
- X86 - Supported mainly by Intel with popular solutions based on Intel Atom and Core ix families

2. Form Factor

- SMARC ('Smart Mobility ARChitecture') is a specification published by the Standardization Group for Embedded Technologies

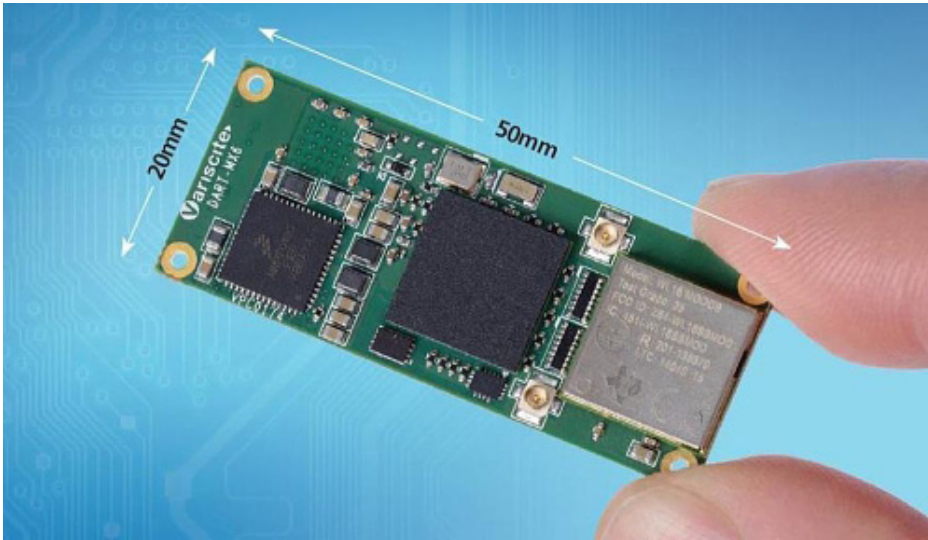
e.V. (SGET) for computer-on-modules (COMs). Generally, SMARC modules are based on ARM processors, they can, however, also be fitted with other low-power SoC architectures, like, for example, those based on x86 SoCs. Typically, SMARC modules' power requirement is in the range of a few watts, which opens up avenues to markets which to date could not be addressed due to processor designs with much higher power consumption. Two module sizes are defined: 82mmx50mm and 82mmx80mm

- Q7 - Qseven is a well-established, legacy-free standard for technology-independent small form factor computer modules, which includes standardized thermal and mechanical interfaces. Qseven was the first standard that supported x86 and ARM technologies in COM-compatible environments. The size is 70mmx70mm and the Qseven standard has been adopted by SGeT.

- Proprietary - The proprietary form factor is the most popular in the SoM market because most customers want a unique platform for their use. It can be very small or in any shape needed to the applicatio.

	Design all in-house	Use a SoM
Development cost (2 man year)	\$240K	
Prototypes and debug	\$30K	
Software maintenance (0.5 man year)	\$60K	
Cost per unit	\$40	\$40 – 60\$

Table 1



Picture Nu2 - Example of Proprietary System On Module based on I.MX6

3 . Which ARM core (Cortex A5, A7, A8, A9, A57) and Example of SoM

Cortex-A5 Processor

The Cortex-A5 is the smallest, lowest cost and lowest power ARMv7 application processor and is supported by a suite of optimized IP targeted at mid-range solutions, bringing the highest efficiency levels and ease of integration.

Popular application processors based on Cortex A5 include the Atmel SAMA5 family as used in the AT-501 System On Module from Shiratech. The AT-501 is an industrial embedded SoM that offers the optimal balance of the most power efficient Cortex-A to date with a high performance CPU running at 536 MHz and a floating point unit. The Memory is 32bit wide @ 166Mhz, 256 MB DDR2, extendable to 512MB. NAND Flash of 256MB extendable up to 1GB, and optional 4GB eMMC.

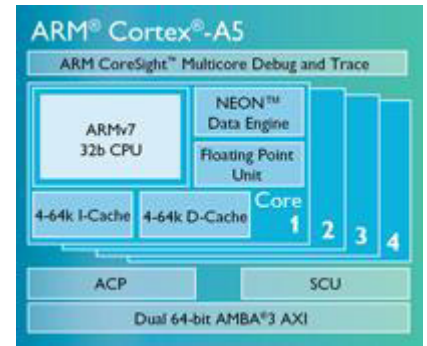
Cortex-A8 Processor

The Cortex-A8 was introduced to the market in 2005 as the first processor supporting the ARMv7-A architecture. The Mali™-400 provides a mid-range graphics processing option for the

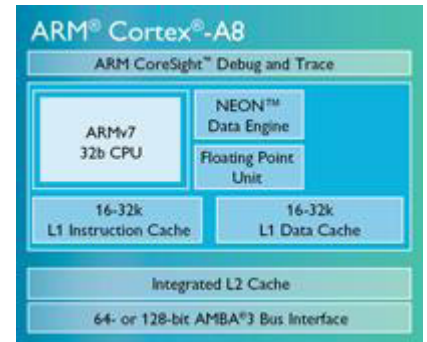
Cortex-A8.

The most popular application processor based on CortexA8 is TI's Sitara family AM33xx and an example of System On Module based on the this solution is the VAR-SOM-AM33 from Variscite. Supporting the 1GHz Sitara™ AM335x ARM Cortex-A8 processor from Texas Instruments (TI) with a rich 2D/3D graphics accelerator, the VAR-SOM-AM33 provides a low-cost, powerful and flexible selection across the full spectrum of applications. Its feature set includes -40 to 85°C temperature range and dual CAN bus, making it ideal for industrial applications such as automotive, control systems, lighting, motor control and agriculture. With dual Ethernet, USB, touch controller, audio and Wi-Fi/BT, the VAR-SOM-AM33 is a highly integrated SoM in a very attractive price range.

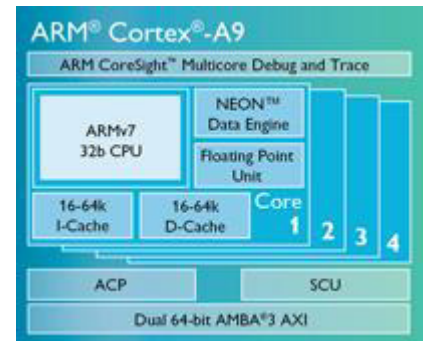
The ARM Cortex-A9 processor is a mature option having been introduced in 2008, and remains a very popular choice to enable the Internet of Things. As a single processor solution, the Cortex-A9 processor offers an overall performance enhancement of well above 50% compared to ARM Cortex-A8 solutions.



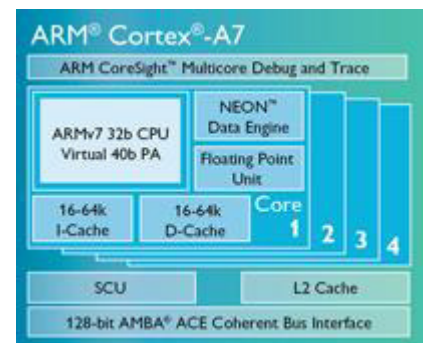
Cortex-A5



Cortex-A8



Cortex-A9 Processor



Cortex-A7 Processor

The most popular families based on Cortex A9 are the Freescale i.MX6 , TI's newest Sitara AM4xxx and the SoCs (System On Chip) from Altera.

SECO have a Q7 module named QuadMo747-X/i.MX6, a scalable, multi-core ARM Cortex™-A9 architecture in Qseven standard modular solution that combines high graphics performance with power-efficient processing capabilities. OpenGL (FULL) and OpenES 2.0 3D graphics and support for up to 3 independent displays (only up to 2 displays with i.MX6DL and i.MX6S) results in a flexible solution that enables multi-display platforms and mobile fanless applications.

The ARM Cortex-A7 processor is the most power-efficient multi-core processor.

The new Cortex-A7 core from ARM , is used in the Freescale Layerscape family LS1. The First SoM in the world based on this solution came from SYSTEC Electronic in Germany, which produces the ECUcore-1021.

The ECUcore-1021 is a compact and cost-effective SOM based on the Freescale QorIQ LS1021A microcontroller. It was especially designed for networked industrial applications. With its high density of available communication interfaces and the two 1GHz ARM Cortex-A7 cores, the module offers outstanding performance at a low power dissipation.

4 . The System On Modules need BSPs (Board Support Packages) to be able to connect between the hardware and the operating system the end customer wants to develop with. The main operating systems are Linux, Android and Windows Embedded.

• Yocto - The Yocto Project is an open source collaboration project that provides templates, tools and methods to help users create custom Linux-based systems for embedded

products regardless of the hardware architecture.

• Ubuntu - A community-developed Linux-based operating system, it is an open source, Debian-based Linux distribution

• Linaro - the not-for-profit engineering organization that consolidates and optimizes open-source software for ARM applications

• Android on an embedded device is a mix of modifications to the Android Open Source Project (AOSP) and the kernel on which it runs, Linux.

• Windows Embedded is a family of operating systems from Microsoft designed for use in embedded systems.

Description of the new solution approach

Arrow Electronics started a project in US in 2013 and activated it in EMEA in 2014 to focus on the System On Module Market to identify best-in-class suppliers with clear differentiation and the ability to support different regions and applications.

The project is supplier focus and market focus driven, as follows:

• Solution based on the top suppliers selected from Texas Instruments, Atmel, Freescale, Altera and Qualcomm

• Market focus on

o Low Cost

□ SoM (System On Modules) from €29 based on Cortex-A5 from Atmel (SAMA5) and \$32 solution with TI AM335x. Also \$40 based on Freescale i.MX6 and TI's Sitara AM49xx Family

o High End

□ SoMs based on Freescale Layerscape LS1 with dual core A7 and Altera SoC Solution with FPGA plus dual core CortexA9

o Community

□ BeagleBoard and BeagleBone

□ HummingBoard

□ UDOO

□ 96Boards

o M2M / IoT

□ Cloud Based SoM Solution from Digi based on Freescale i.MX6

o Standard Form Factors

□ SMARC from Shiratech based on Altera SoC

□ Q7 from SECO based on i.MX6 from Freescale and also from Inforce Computing based on Qualcomm Snapdragon 600

Conclusion

Many embedded development projects today require similar underlying processing and communication functionalities. These capabilities have much in common with those of mobile phones and other high volume devices, which means that the cost of individual components has been reduced and the basic board designs have been completed. By selecting from a variety of existing Systems on Module (SoMs), companies can focus their development efforts and budget on their own IP in the knowledge that they have a tried and tested solution at the heart of their design.



Amir Sherman, Technology Marketing Director Embedded, EMEA, Arrow Central Europe GmbH



This chip can find the needle in a haystack (and examine it)

> Liesbet Lagae, Imec

Just imagine you have to find a tumor cell in a milliliter of blood. One stray cell among many millions of healthy ones; one cell that you have to recognize and isolate so you can further investigate it. Sure, there are tools out there to help you. But now researchers are developing a chip-sized detective that may find the cells you're looking for faster and cheaper than ever before. Moreover, this new diagnosis tool will be much more compact than existing tools, and much easier to use. The secret: a smart combination of silicon technology, lens-free microscopy, and ultras-small steam bubbles.

Scanning everything from tumor cells to stem cells

The evolution in chip technology has given us smartphones that far outcompute the room-sized servers of a few decades ago. In a few

seconds, e.g., anyone anywhere can now take their smartphone, find out who first detected the HIV virus, and download the latest articles on the subject. This thanks to the enormous miniaturization of computer processors, image sensors, memory chips, wireless communication chips and high-resolution screens, all packed into an elegant and compact 'box', also known as your smartphone. What would happen if we could also apply this extreme miniaturization of systems also on tools for medical diagnosis? To make tools that would allow any medical doctor to do complicated tests on the fly, e.g. screening blood cells in a patient's blood sample. Think of a cancer specialist, who would immediately be able to see if a patient has tumor cells roaming in his blood, a potential sign of metastatic cancer. Who would check after a patient's chemotherapy

if the number of tumor cells in the blood has diminished and if the treatment has to be continued or modified. A tool also that would make it possible to see if a patient's blood is contaminated by specific bacteria, allowing to start a targeted treatment immediately.

Such a high-throughput 'cell sorter' chip would not only lead to faster diagnosis. It could also allow a very fast way to isolate tumor cells in order to sequence their DNA and start a treatment based on the characteristics of the specific tumor type. Or used in stem cell therapy, it could be deployed to check if a colony does not contain any bad cells. In the process of culturing cells, something may go wrong, resulting in cells that may be dangerous for patients.

So a compact, fast, and easy-to-use cell sorter chip would open up many possibilities for practitioners in

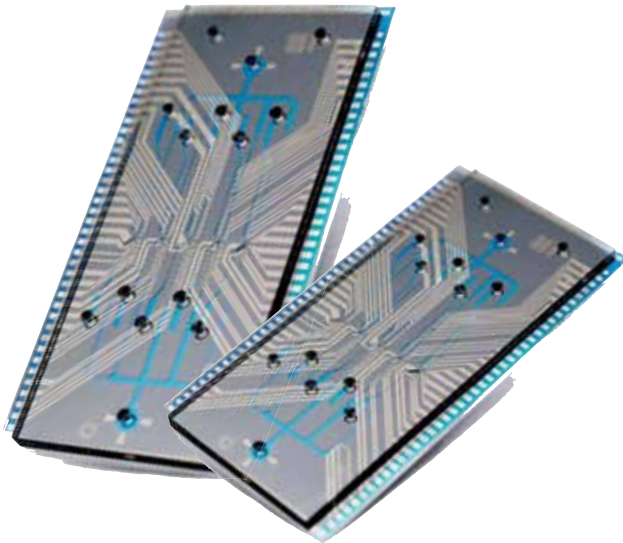


Figure 1: 'Cell sorter' chip that identifies and sorts 3,000 cells per second

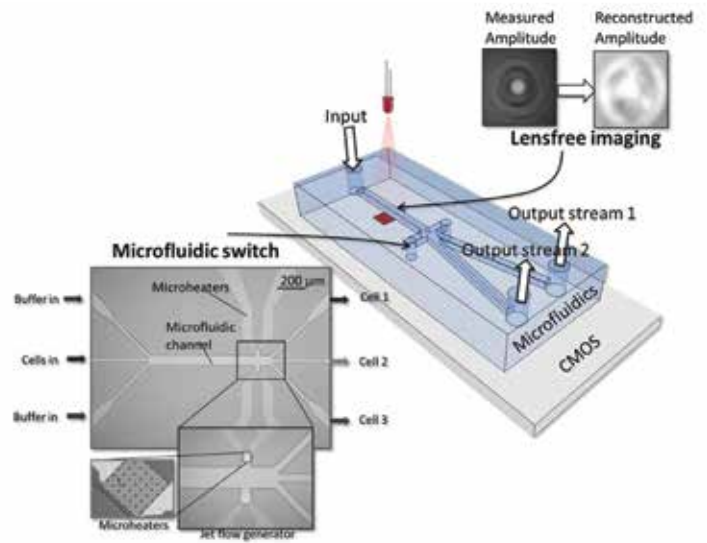


Figure 2: Concept of the high-throughput 'cell sorter' chip

hospitals, remote points of care, or at the doctor's practice.

A concept comes alive

The idea for the high-throughput 'cell sorter' chip was developed two years ago (see <https://vimeo.com/82078661> and figure2). R&D manager Liesbet Lagae was awarded a prestigious ERC-grant to further develop the promising idea. And imec scientists made the first building blocks and integrated them in a chip of 4cm x 2cm (figure3), with the following process for a cell analysis:

- A drop of blood is inserted into the input channel
- The cells move through a microfluidic channel with a high speed of a few meters per second
- One by one, the cells pass over an image sensor while they are illuminated by a laser
- Based on the holographic image on the sensor, a powerful computation chip reconstructs an image of each individual cell
- The cell is identified (a tumor cell, bacteria ...)
- If the cell is of a type that we want

to investigate, it is separated in a distinct microfluidic channel. This is done with the help of steam bubbles generated with heating elements

- In the different output channels, the live cells are collected for further examination

A smart combination of silicon technology, lens free microscopy and ultrasmall steam bubbles

The 'cell sorter' chip is fabricated in silicon technology, the same technology also used to make computer and memory chips. One of the advantages is that all building blocks can be mass-produced extremely compact and be integrated in a cost-efficient way. This cost advantage becomes even greater if more, parallel sorting structures are integrated on the chip.

For visualizing and identifying cells, the cell sorter uses lens-free digital holographic microscopy. A laser on top of the microfluidic channel illuminates the cells as they pass. An image sensor placed under the channel captures the interference pattern of the laser light and the light that has passed through the cells. With this interference pattern, an image of

the cell can be reconstructed. The image quality is comparable to that of phase contrast microscopy. We optimized this technology, improving the resolution considerably by using a light point source (which creates a 'zoom' effect).

Experiments with blood samples have shown that this technique allows to distinguish between three major classes of white blood cells: granulocytes, monocytes, and lymphocytes. These types differ in their size and granularity of the cell contents. In the experiments, we first looked at samples that contain only one type of cell. This allowed to optimize the classification algorithm. Next, we analyzed a full blood sample, with the results shown in figure 5. These results are highly comparable with those obtained with a clinical hematology analyzer (figure 6), which proves the validity of the lens-free microscopy technique.

The microfluidic switch that we use to separate the cells of various types is based on small, starlike heating elements (figure 7). Our prototype contains 288 such elements, situated

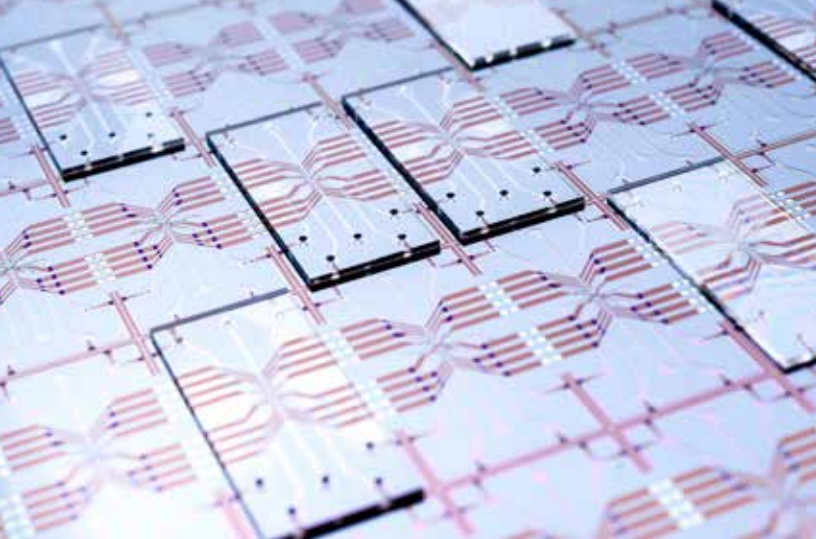


Figure 3: Silicon wafer holding 20 prototypes of the high-throughput 'cell sorter' chip

after the microscope and on both sides of the channel. These heating elements create steam bubbles that push the cells into the right channel. Sorting with these jet flow generators takes about 100 microseconds per cell. This speed is unique, and is also the result of not using any moving elements.

Our scientists have performed an experiment in which the cell sorter had to isolate monocytes from a PMBC-sample (Peripheral Blood Mononuclear Cell) with monocytes and lymphocytes. The sorter, using the jet flow generators, was able to move 88% of the cells to the correct output channel. The purity of the collected monocytes at the chip's exit was 99%. These are exceptional results proving that the cell sorter does

what it has been designed for. One way of further improving the accuracy of the jet flow generators is adding a sensor that communicates the exact position and speed of a passing cell to the jet flow generators.

The power of parallelization

This concept and prototype of a cell sorter becomes extremely powerful if you consider the parallelization that is possible with the silicon technology. The first prototype has one microfluidic channel with a lens-free microscope and with jet flow generators on both sides of the channel – but it is fairly straightforward to extend this design to hundreds of channels that function in parallel and thus can sort hundred

thousands and even millions of cells. That way, it becomes possible to attain an unseen throughput for cell analysis and isolation. In our design, the number of channels we can add is limited by the chip area and related cost (we estimate that a hundred channels will take up a square centimeter of silicon); by the power of the laser of the lensfree microscope; and by the computations needed for the image recognition. Currently, the researchers work to fabricate a 5-channel sorter as a proof-of-concept for the improved throughput and parallel sorting.

About the author

Liesbet Lagae - R&D manager lifescience technologies, imec

Liesbet Lagae is co-founder and currently R&D program manager of the life science technologies activities in imec. In this role, she oversees the emerging R&D of all the life science technologies activities at imec. She holds a PhD degree from the KU Leuven, Belgium for her work on Magnetic Random Access Memories obtained under an IWT grant. As a young group leader, she has initiated the field of molecular and cellular biochips based on magnetic, plasmonic, electrical sensing principles intelligently combined with fluidics to do full diagnostic analysis at IMEC, Belgium. She is also appointed as a professor in nanobiophysics at the KU Leuven. She has

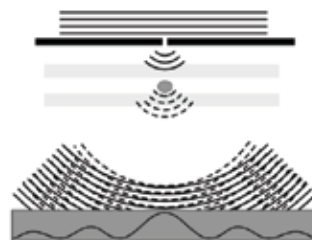


Figure 4A: Lens free digital holographic microscopy captures the interference of direct laser light with light that has passed through the cell

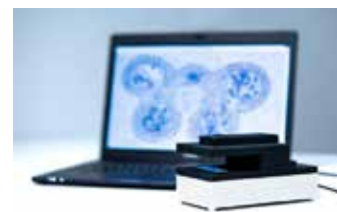


Figure 4B: Demo setup of the lens free microscope

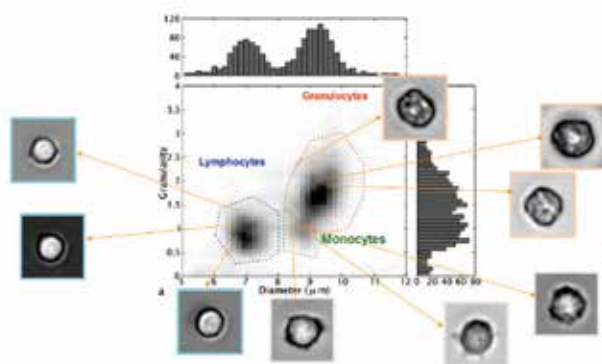


Figure 5: With the help of lens-free microscopy, three types of white blood cells may be recognized in a blood sample

(co-) authored 75 peer-reviewed papers in international journals and holds 15 patents in the field. She is also part-time professor in nanobiotechnology at KU Leuven/Physics department.



Liesbet Lagae, Imec

	Granul.	Lymph.	Mono.
IMEC Cell-Sorter	57.9%	34.5%	7.5%
Hematology analyzer	65.6%	27.6%	6.8%

Figure 6: The measurements of the 'cell sorter' chip and a conventional hematology analyzer show highly comparable results for the percentage of blood cells from the three subtypes in a sample

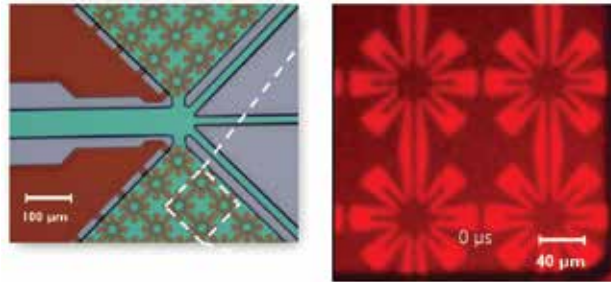


Figure 7: Sorting the cells is done through small, starlike heating elements that cause small steam bubbles. These pressure the cells into the appropriate channel

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Extending the Life of Test Systems that Support Long-term Programs

› Jim Curran, Keysight Technologies, Inc.

At the beginning of every new product program, tremendous amounts of time, attention and money go into defining and integrating the required test system. The system is used to test the new products, ensuring that they function at the required levels and remain highly productive. The system is also expected to last for the life of the program.

Carefully designed test systems help ensure high quality results and maximum throughput. Over time, drifting test results can affect quality, and equipment downtime result in costly delays. In later years, changes in parts availability and vendor support capabilities add to the challenges.

Fortunately, managers can mitigate these risks and keep their programs running by working with an experienced solution partner. As an original equipment manufacturer (OEM), Keysight offers efficient and

effective alternatives that can extend the life of test systems and ensure that the individual instruments are meeting their warranted specifications.

Examples include Keysight's Extended Service Period (ESP) solutions for calibration and repair. These embody the company's commitment to our customers' installed base of older HP, Agilent and Keysight equipment. Through standard and tailored ESP solutions, Keysight helps our customers keep long-term programs running until they're ready to make the transition to new technology.

ESP solutions are part of a bigger initiative called Keysight Instrument Lifecycle Solutions (ILS). Best expressed as a commitment to operational continuity, these solutions address the service requirements that span a customer's product lifecycle (Figure 1). Through these solutions, Keysight helps ensure system longevity, starting

from the initial date of purchase and extending well into the future.

Going around the figure, Warranty Period solutions include our standard three-year warranty as well as the opportunity to ensure that level of coverage for up to 10 years. Standard Service Period (SSP) solutions ensure ongoing performance, post-warranty, by delivering Keysight-quality service-in-calibration and repair - that optimizes the customer's budget and enhances instrument uptime. Extended Service Period solutions cover essential equipment after product manufacturing ends, giving our customers more time to make a seamless transition to new technology.

Understanding the OEM's dilemma

There is an inescapable paradox in the support of aging test equipment. Early in the system lifecycle, OEMs can



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provide strong support; however, new instruments typically require much less support than older equipment. The need for support increases as instruments age, but an OEM's support capabilities typically decline due to discontinuance of manufacturing, reduced parts supply and fading expertise (Figure 1).

The underlying cause is the natural lifecycle of any commercial product: introduction, growth, maturity and decline (Figure 2). Every product progresses at a different rate, driven by outside factors: adoption by customers, competition from other manufacturers, overall economic conditions, and so on. As demand declines, OEMs often introduce new products to replace aging models, and this requires new investments in manufacturing, parts and expertise.

As each product ages, the OEM makes tradeoffs and decisions about the allocation of the scarce resources dedicated to manufacturing and support. Sustaining an older product consumes resources that could be used to develop new products based on newer technologies (Figure 3).

One reason to shift resources is the expectation of higher returns on the money invested in a new product. Astute OEMs do this in a manner that meets the needs of existing customers by providing compatibility modes,



Figure 1. Instrument Lifecycle Solutions address service requirements for the instruments customer's use to support long-term programs

long lead times for notification of discontinuance, and extended service capabilities.

The most challenging scenario is an aerospace/defense (A/D) program, which may be expected to live for 15 to 25 years. In general, the duration of a commercial product's lifecycle is much shorter than that of an A/D program (Figure 4). This creates a timing problem: in many cases, the instruments in a test system have passed their peak demand and are beginning to decline as the A/D program is reaching its peak. As the A/D program crests and then noses

over into a gradual decline, the next generation of OEM products is in the growth phase (refer back to Figure 3). Parts availability is the other major factor. An instrument, such as a microwave signal analyzer, contains thousands of individual parts produced by hundreds of vendors. Each part goes through its own lifecycle, from introduction to discontinuance. External forces such as changes in government regulations (e.g., RoHS compliance) may also affect parts availability. Parts manufacturers, as independent businesses, also go through a natural lifecycle of growth and decline.

Extending the Life of a Test System

All of the preceding provides context - but it is still possible to create an effective strategy that adds years to the usable life of a test system. The best chance to plan and execute this strategy is at the time of the original purchase. If this opportunity has passed, there is still time while the instruments remain in production. Even if the instruments are out of production, there are ways to extend system life.

At the initial purchase (Warranty Period) As noted above, A/D systems may be expected to last 15 years or longer. When defining a test system and evaluating the available instruments,

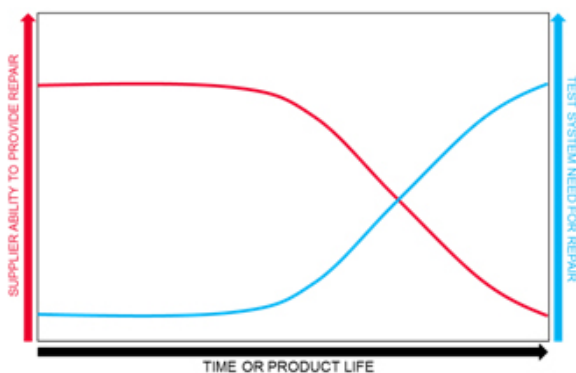


Figure 2. There is often an out-of-phase relationship between an OEM's ability to provide support and a long-term program's need for that support

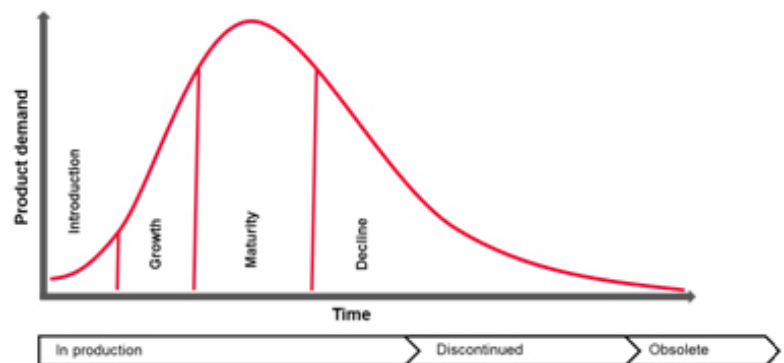


Figure 3. The traditional product-support lifecycle periods (bottom bar) follow the demand lifecycle (red curve)

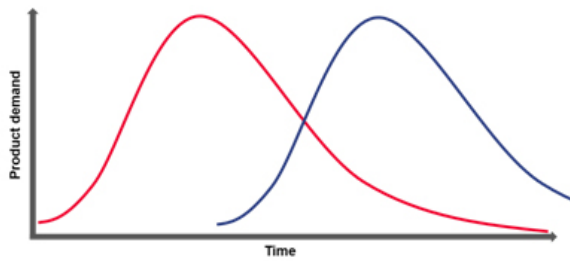


Figure 4. As the older product declines, the newer one grows, requiring new investments in manufacturing lines, parts and warehouse space

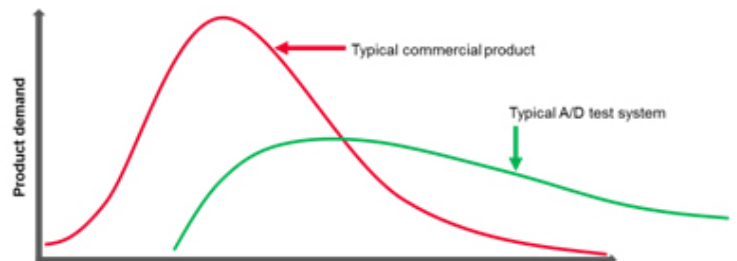


Figure 5. The other timing problem is the offset between the decline of commercial products and the growth and long decline of an aerospace/defense system

several key questions are worth considering:

• **How long has the OEM been in business?**

o What's the likelihood they'll be around 20 years from now?

• **How well do they listen to your needs?**

o Do they respond with suggestions that make sense from a technical perspective?
o Do their suggestions make sense from a business perspective?

• **Can the OEM support your program over the long term by supplying needed system components?**

o Do they offer cost-effective assurance plans and maintenance services?
o Do they have a service infrastructure designed for present and future needs?

• **What is the real cost of doing business with the supplier-now and through the life of the test system?**

o What is the duration of its standard warranty?

The greater the number of favorable answers, the greater the likelihood a vendor will be able to ensure that a system will operate at peak performance well into the future.

During production and while replacements are still available (SSP)

As long as an instrument is in production, the OEM's support capabilities are relatively high. This is a good time to adopt best practices such as utilizing high-quality services and developing contingency plans for the post-

manufacturing phase.

Solid contingency planning starts with a key assumption: OEM support capabilities will diminish with time. It's best to work directly with the OEM to determine long-term plans and needs. For example, it's wise to regularly monitor product lifecycles and assess the value of making lifetime buys of all crucial components. The OEM should be willing to help ensure a sufficient inventory of parts or assemblies to avoid critical failures.

This is also the best time to identify critical instruments and purchase an optimum number of spares based on statistical data such as the mean time between failures. Creating and maintaining intra- and inter-company asset lists may reveal available spares and also prevent unnecessary scrapping of still-needed instruments.

After products are no longer manufactured (ESP)

Eventually, an organization will have to deal with the support and maintenance of instruments that are out of production. At that point, three options are available: OEM services, third-party services and self-maintenance.

While the best choice depends on the business and technical specifics of the situation, the OEM will usually provide higher quality service than a third-party provider or in-house self-maintenance staff. One reason: providing excellent service ensures customer satisfaction and, being pragmatic, helps protect the company's reputation. Also, because

they are aware of need for longer-term support, some OEMs have planned for this on a product-by-product basis. This requires an investment in the necessary infrastructure: staff, equipment, test systems and supply chain of genuine OEM parts.

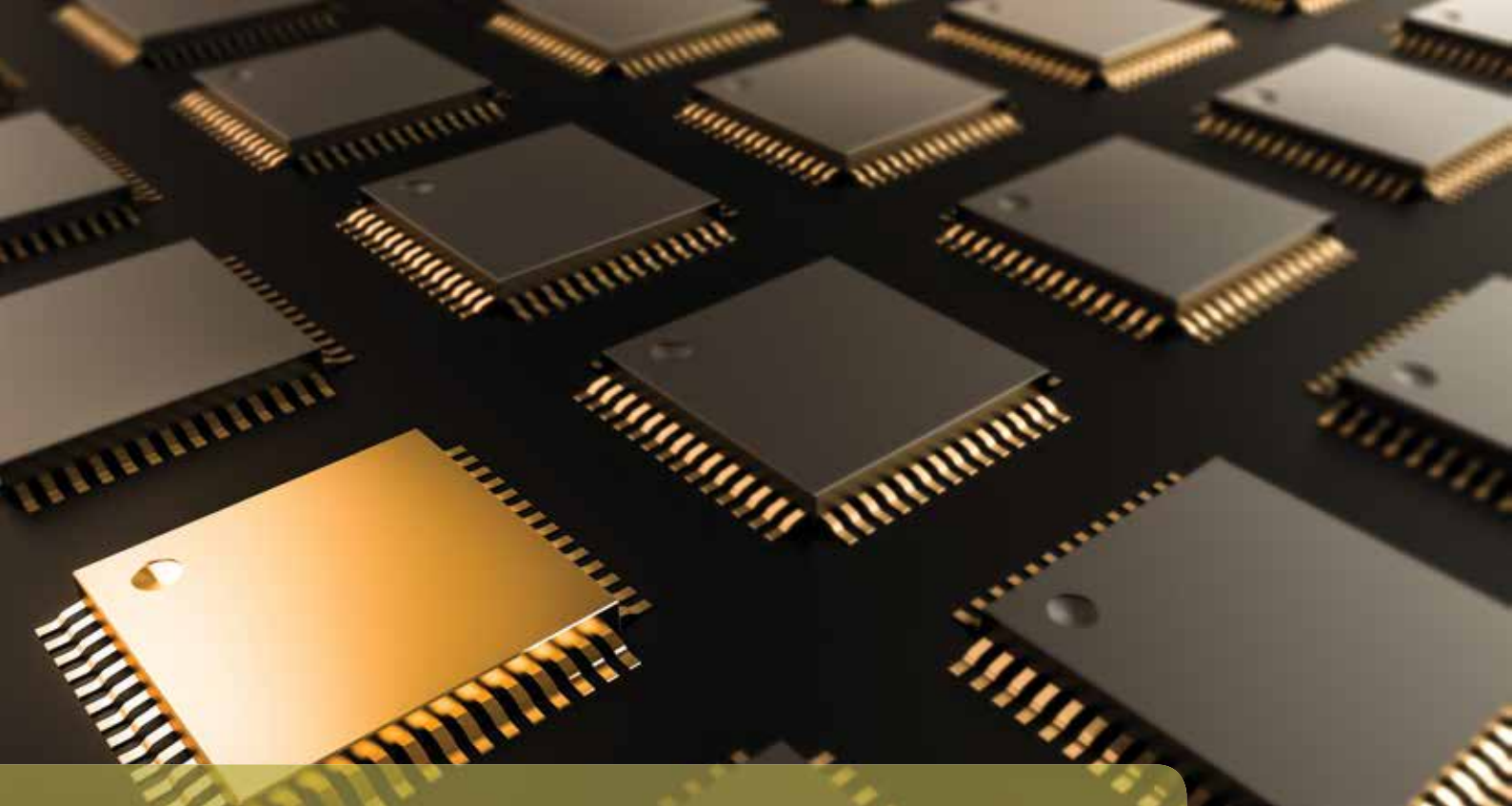
Another option is to purchase second-hand equipment to use as replacements for failed instruments. This can be useful if the following items are true about the used equipment:

- Any necessary repairs have been performed by factory-trained technicians
- When needed, only genuine OEM parts were used
- After any repairs, the instrument received a full calibration and all necessary adjustments

Similar to the suggestions offered earlier, we recommend purchasing used equipment that has been fully refurbished by the OEM.

Conclusion

As our customers assess service alternatives, they can be confident in Keysight's ability to ensure their operational continuity. We know that it takes time to find the right equipment and a trusted solution partner. Once a test system is up and running, the responsible organization needs confidence that it will keep going. That's why we're offering Instrument Lifecycle Solutions, including our Extended Service Period solutions.



CMOS Sensors Boost High-End Medical, Industrial and Consumer Imaging

> Pieter Willems, CMOSIS

Image capture of real-world scenes and blending this with virtual information represented as visual patterns is a vital tool in a growing number of industrial, medical and consumer applications. This new CMOS image sensor is used in a new imaging device for non-invasive cancer assessment. It forms the heart of a custom developed camera, which is used by FFOCT (Full Field Optical Coherence tomography) endoscopes for in-vivo optical probing as well as fast ex-vivo microscopy. The new CSI2100 sensor features an extremely high full-well capacity of 1.6 million electrons in its 1440x1400 pixels and a frame rate up to 700fps. Advanced image-capture applications

are opening up in a broad variety of products and systems. Yet there is no one specific image sensor to serve all those different conditions. Every system is best served with a specific imager optimized and designed to match the prevailing application and user requirements. (Figure 2) This is especially true for industrial and medical vision applications. Thus, such digital camera applications require carefully laid-out image sensors adapted to deliver the best possible results in terms of resolution, noise, speed, spectral sensitivity, robustness, life cycle and price point. A comparison with natural vision capabilities in animals is helpful in this regard: birds of prey, snakes

and cats all depend on very different kinds of visual input in terms of spectral sensitivity, field of view and resolution. As a consequence their "image sensors" have evolved to match the specific circumstances and necessities of their lives.

High Full-Well Capacity

A good example of sensor specialization is the new high-speed CMOS image sensor CSI2100 made by CMOSIS targeting demanding scientific and medical applications. With its global-shutter layout of 1440 x 1440 pixels at a pixel pitch of 12µm, the CSI2100 achieves the extremely high full-well charge of 1.6 Me per pixel – delivering unprecedented

resolution and detail richness in its dedicated field of optical tomography. It enables in-vivo inspection of human tissue down to the cell level as well as fast ex-vivo microscopy. The CSI2100 wafers are fabricated by the wafer foundry Tower Jazz in Migdal Haemek, Israel.

Besides its high full-well capacity the CSI2100 achieves high frame rates up to 700fps by integrating 35 LVDS (Low voltage Differential Signaling) outputs. Dark noise, mainly caused by ADC quantization noise, is held to 945e. Dynamic range is 66dB. The chip, housed in a small μ BGA package with 173 pins, has a power consumption of just 2 watts (Figure 3).

The new sensor was conceived within the EU-funded FFP7-ICT project "CAREIOCA" (Non-Invasive Optical Biopsy for Cancer Assessment Using Ultra-high Resolution Full-Field Optical Coherence Tomography) started in 2013. The program is continuing at a fast pace developing and evaluating high-resolution/high-speed medical imaging devices for performing non-invasive optical biopsy procedures by building volumetric images through a Linnik interferometer analysis of the interference patterns of light reflected by the examined tissue and a reference light source via an oscillating mirror. This way, living cells of 5 μ m in diameter can be captured and examined.

A major scientific goal of the CAREIOCA program is to establish atlases of specific FFOCT histology imagery for clinical use, foremost in the diagnostics and post-surgical evaluation of cancer. This part is carried out by Leiden University, The Netherlands, and Gustave Roussy Institute in Villejuif (Paris). Optical

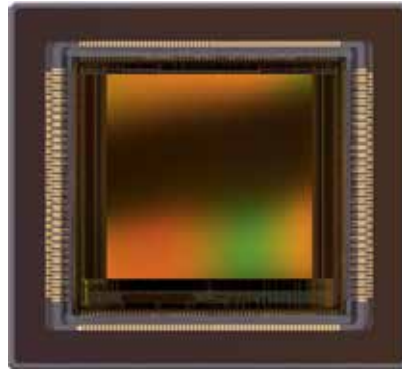


Figure 1: Sensor CSI2100

biopsy is meant to ease the burden on cancer patients by avoiding the destructive removal of tissue probes for traditional biopsy and histological analysis procedures.

By the end of 2014 CAREIOCA had progressed to demonstrating proto-types of a handheld FFOCT endoscope containing the compact 2-MP camera Q-2A750/CXP with CoaXPress interface, integrating the CMOSIS sensor CSI2100. This new diagnostic prototype system shows a 5 times higher processing speed and a 3 times higher sensitivity compared to existing designs.

CMOS Sensor Trends

CMOS sensors and cameras have

developed to a point where they capture near-perfect imagery. Their advantage compared to the older CCD imagers is that they can be narrowly tailored to their specific application fields. In addition, CMOS sensors, by virtue of their operational principle and established manufacturing processes as CMOS semiconductor devices, integrate on the same chip image capture with multiple support functions.

Such support functions include image processing for high dynamic range (HDR), on-chip noise suppression, flexible channel multiplexing, windowing and subsampling, and high-speed LVDS interfacing. All this leads to more compact camera designs, better system interconnect and compatibility, and ease of use.

High data throughput is very much in demand for industrial vision, especially in production and inspection tasks. Users want to get as much data off their imagers as possible, asking for the highest possible frame rate for their specific applications. Throughput rates have increased over the past few years from 30 to 60 to about 120

Figure 2: Image sensors are essential for a broad range of digital systems and products

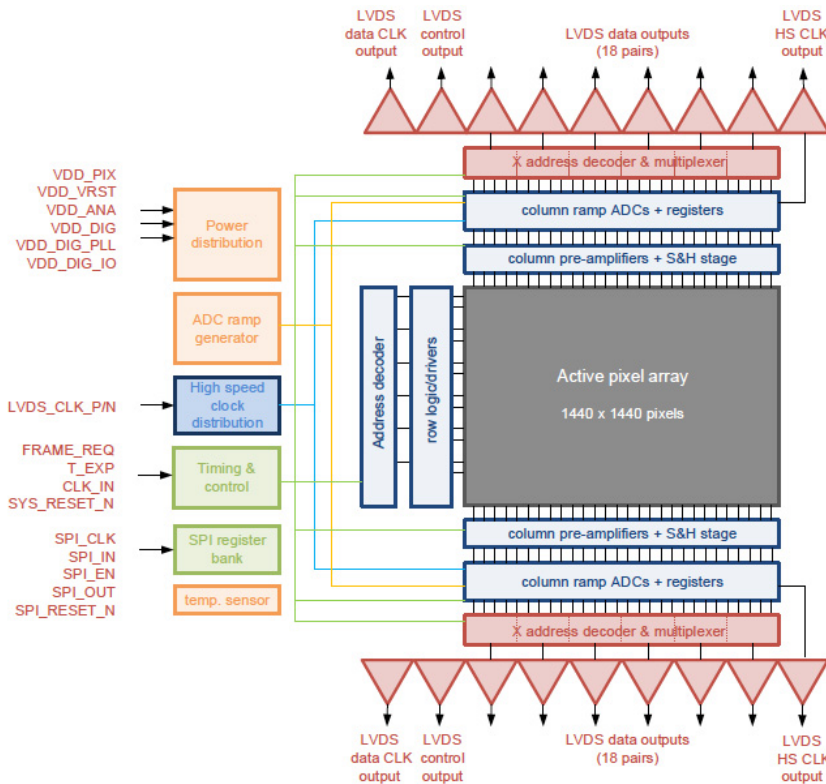


Figure 3: Layout of the CSI2100 high-speed global-shutter

to 240 frames per second.

Thus, sensors and cameras must be able to accommodate higher frame rates. CMOS cameras have improved to a degree where they outperform traditional CCD-based imagers. A new off-the-shelf 12-Megapixel digital image sensor from CMOSIS, the CMV12000 Series, delivers 300 fps at full resolution (10 bits per pixel). Other sensors of the same product family show similar data rates with different resolutions.

Even higher frame rates are feasible in windowing or subsampling modes. The same fast-paced progress of CMOS sensors applies to pixel count, or resolution. It has gone from 1.3 MP (SXGA) up to 2, 4, 8, 12 and 20 Megapixels. Higher resolution enables cameras to capture more details that can be analyzed within one image with a wide field of view (Figure 4). This is advantageous in traffic management applications, where one high-resolution



Figure 4: Capturing a large field of vision with great detail

camera can now track up to four lanes of traffic instead of having to deploy four individual lane cameras.

In the light of this technological progress, a resolution of 3.5 - 4K is standard today in traffic and video recording applications. For high-end industrial inspection, as in flat-panel inspection or aerial mapping, standard resolution is 20 MP. However this is not the end. The general trend points to still higher resolutions for global-shutter cameras. It might take another year to get up to 40 - 50 MP. This is where rolling-shutter sensors are still defending their turf: with pixel counts of up to 70 MP.

Demands on Image Capture Systems

- **High sensitivity:** This should be coupled with low noise levels as the foremost consideration of industrial users. High sensitivity will deliver enough image data at short exposure times. Low noise and high sensitivity also allow operation at a low light intensity by applying the proper gain if needed. High sensitivity across the visible spectrum should be accompanied by increased sensitivity in the near infrared.
- **Low cost:** Minimum system cost is best achieved via image sensor size reduction, optimization and if high-volume production for yield optimization.
- **High frame rate:** This enables several shots of an object in a rapid-fire sequence to track and document its movements. This is supported by the technique of exposing one image while the previously taken image is being read out.
- **High resolution:** This equals a large field of view for delivering high image

detail.

- No image correction: All these demands have to be implemented without impacting the raw image quality so that no extra off-chip correction is needed.

Global Shutter for CMOS Sensors

Combining a much smaller pixel layout with a global shutter is another major progress that imagers from CMOSIS have achieved in the last few years. A global shutter exposes all pixels of a sensor at the same time and over the same duration. It is a more complex concept - and it was initially more costly to implement in CMOS sensors - because it requires some kind of a local storage element (usually a capacitor) inside each pixel, plus some control function to start and stop the exposure. All this enlarges pixel size. A rolling shutter, in a marked difference, will expose an image sequentially, row by row, top to bottom, at different moments in time, much like the mechanical curtain rolling down behind the lens in an old-fashioned analog photo camera. This rolling effect causes time-related artifacts, which can skew the image

of fast-moving objects as the exposure follows or deviates from their horizontal or vertical position at any given moment across the image plane (Figure 5). Another rolling shutter artifact occurs when illuminating the scene with a short-burst flash. The result is that only a few rows or parts of the image are exposed, whereas other areas remain dark.

The rolling shutter concept has been the traditional method also in digital imaging since it is much easier to build a pixel architecture adapted to the row-by-row exposure scheme. Therefore CMOS sensors with four-transistor pixel architecture usually come with a rolling shutter. The lower number of pixel transistors and state-of-the-art layout results in pixels with excellent specs in regard of dynamic range and dark current. CMOSIS has developed high-end sensors for the M camera model of Leica Camera based on these rolling shutter pixels.

Providing a global shutter in a CMOS sensor is more complicated since it involves placing the storage capacity inside each pixel. This takes up space and leads to a larger pixel layout, which is more expensive.

However, global-shutter technology

as offered by CMOSIS has greatly improved. This primarily pertains to the capacitive storage nodes needed inside each pixel to hold the pixel values for reading them out sequentially after the exposure stops. Smaller storage nodes are now feasible with reasonably small pixel sizes and at lower price points. Advanced global-shutter CMOS sensor designs feature pixels down to $5.5 \times 5.5 \mu\text{m}^2$ as available in the CMOSIS CMV product family. The goal is having $3.6\text{-}\mu\text{m}$ pixels with a low noise global shutter in the near future.

Of course, this scaled-down CMOS layout requires fabs or foundries with wafer-processing capabilities that can accommodate these small pixel dimensions. It also needs comprehensive design know-how to create the appropriate pixel architecture and technology.

Eight-transistor Pixel Architecture

Fitting a low-noise global shutter to a CMOS image sensor requires a complex pixel architecture. But a specific new architecture is set to overcome this obstacle. The eight-transistor (8T) global-shutter

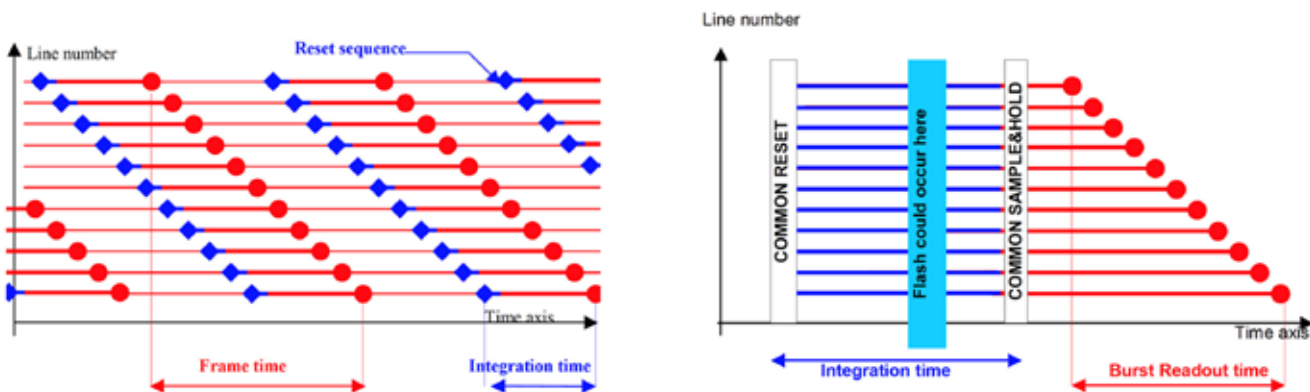


Figure 5: A rolling-shutter design (a) causes moving objects to be depicted with skewed lines, so fast-moving objects to appear skewed. Also, a flashlight exposes only a part of a frame. This is not the case with a global-shutter design (b)

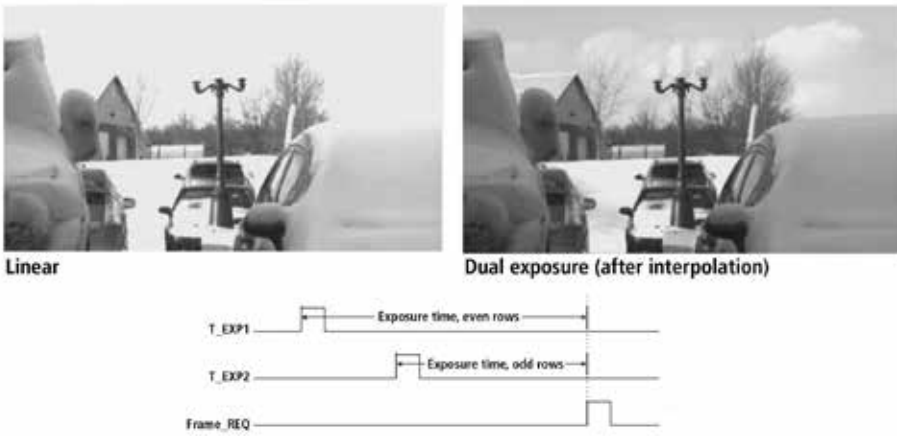


Figure 6: Different exposure times for odd and even lines achieve a higher dynamic range

architecture patented by CMOSIS differentiates it from the traditional 4T rolling shutter or the 5T global shutter concept. This eight-transistor pixel design is now implemented in all global-shutter sensor types of the CMOSIS CMV Series sensor family. The crucial point is that the 8T architecture provides two storage elements inside the pixel, rather than just one (as in the 5T structure). They separately store an image taken at the beginning of the exposure,

and another one at the end of the exposure period. Deploying a clever algorithm, both these images are subtracted during readout to lower the total noise account and increase the shutter efficiency. This way, noise levels below 10 electrons can be reached, and a shutter efficiency of 99.999 percent has been demonstrated. The technique, called correlated double sampling (CDS), enables the lowest fixed-pattern noise and low parasitic-

light sensitivity when compared to 5T layouts or other designs.

Time-Delayed Integration

Time-delayed integration (TDI) imaging is another clever way to better capture moving objects. By synchronizing pixel exposure with the motion of the camera or the object, the effective exposure time can be increased. TDI implementation in CMOS has traditionally been difficult because of the lack of a charge-addition circuit. The application requires the combination of a global shutter and a low-noise readout method. Recently TDI in the digital domain, enabled by high frame rates, has become more and more popular, even though the improvement signal-to noise ratio improvement is lower than for the traditional TDI operation.

High Dynamic Range (HDR)

Another factor in improving global-shutter CMOS sensors is applying a specific method to achieve a high dynamic range (HDR). HDR expands the scale of the captured light and dark areas of an image to depict them in a satisfactory way. This is appropriate when capturing an image before a bright sky background or against very bright light sources, which tends to deliver overexposed images with blurred-out white areas, whereas the darkest shadows appear underexposed and recede into an unstructured black. Thus, the exposure levels for both light and dark areas have to be equalized across the image.

The reason for the unbalanced treatment of light and dark areas is the linear response curve of CMOS image sensors as opposed to the

High Dynamic Range

- **Current CMV solutions:**
 - Dual exposure: odd and even rows different exposure time
 - Piece-wise linear response
- **Other**
 - Logarithmic response
 - Combination of consecutive images with different integration times
 - In the pixel ADC

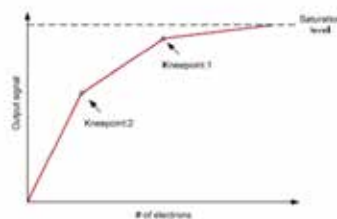


Figure 7: Piece-wise linear forming of the sensor response curve achieves a higher dynamic range

CMV NIR enhanced sensitivity

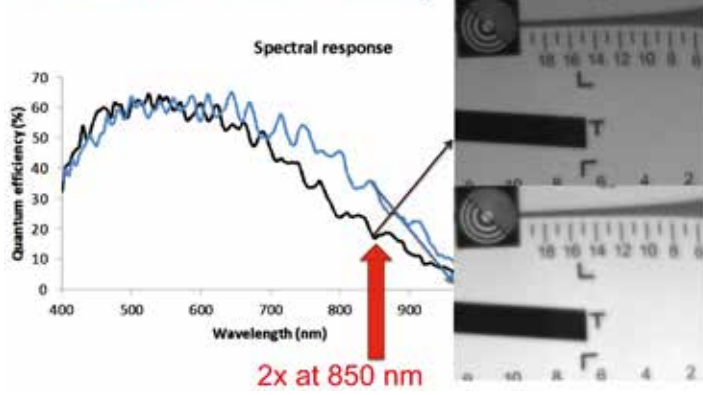


Figure 8: Enhanced sensor sensitivity in the near infrared, as demonstrated in the CMV family of CMOSIS.

CMV image sensors – standard products

- Developed for machine vision applications
- Global shutter, excellent shutter efficiency
- High resolution
- High speed
- Excellent image quality – replacing CCD sockets!!



Figure 9: The CMV Series sensors of CMOSIS were developed for machine-vision applications.

Specification	CMV300	CMV2000, CMV4000, CMV8000, CMV12000	CMV20000
Pixel size	7.4 μm	5.5 μm	6.4 μm
Full Well charge	30,000 e-	13,500 e-	15,000 e-
Sensitivity	6 V/lux.s (550nm)	4.64 V/lux.s (550 nm)	8.29 V/lux.s (550 nm)
Dark noise	20 e-	13 e-	8 e-
Dynamic range	64.1 dB	60 dB	66 dB
SNRmax	45.1 dB	41.3 dB	41.7 dB
Parasitic light sensitivity	1/ 50,000	1/ 50,000	1/ 50,000
Dark current	100 e-/s (@23 degC)	125 e-/s (@23 degC)	125 e-/s (@23 degC)
Fixed pattern noise	<0.1 % of full swing	<0.1 % of full swing	<0.2 % of full swing
Power consumption	<300 mW	600 mW (CMV2000, CMV4000) 900 mW (CMV8000) 3000 mW (CMV12000)	1100 mW

Table 1: Key specifications of the CMV Series.

expo-nential, or logarithmic, behavior of the human eye. HDR is helpful in traffic applications for subduing glaring reflections when reading license plates or countering the over exposure effects of bright headlights. The desired logarithmic response in a CMOS sensor can be achieved on-chip in several different ways:

- by sequential image capture using widely varying exposure times, thereby recording the light and dark areas separately,
- by equipping the sensor's odd and even rows with different sensitivities for light and dark and calculating an appropriate average value for all regions of the image (Figure 6), or
- by using a piece-wise linear response (PLR), which delivers a more logarithmic ramping of the sensor's response curve (Figure 7).

The user can choose the best suited method depending on the application, as they all have their specific benefits and drawbacks.

Enhanced NIR Sensitivity

Extending the spectral range of CMOS sensors to the near-infrared realm is becoming more and more important as a market trend (Figure 8). This especially applies to traffic applications but also to machine vision, because it allows the illumination of the scene to be monitored with flash lights that are invisible to the human eye.

Pieter Willems is Manager Standard Products at CMOSIS in Antwerp, Belgium.



New Adapter Regulations for a More Efficient IoT

> Jeff Schnabel, CUI

Tens of billions of “things” are set to be connected to the Internet over the next few years, but not all will be individual IP-addressable sensors. Many will be gateways that concentrate data received from arrays of devices via links such as Bluetooth® or proprietary low-power radio, or wired point-to-point or fieldbus connections. With these devices included, the Internet of Things (IoT) could be gathering data from more than a trillion sensors to be processed and stored in The Cloud.

Much IoT design analysis is focused on ultra-low-power design, enabling endpoints such as smart sensors to run for long periods powered by a battery or by energy harvested from the ambient environment. Gateway devices require significantly more power than a small battery or energy-harvesting system can provide.

Unlike sensors, which must be placed in specific locations, gateways allow more flexibility to position the device near a convenient source of power such as

an AC wall outlet. If an external power adapter is used to provide the low-voltage DC supply for the gateway, designers can simplify the gateway’s internal circuitry and outsource the responsibility to comply with power safety and efficiency standards to the adapter supplier.

Making Adapters More Efficient

Designers of all sorts of OEM systems have been choosing to power their designs with an external adapter for several decades now. In fact, adapters have been so successful that researchers as long ago as the 1990s foresaw a future powered by billions of the devices. A 1998 study by Alan Meier of Lawrence Berkeley National Laboratory (LBNL) estimated that about 5% of total residential electricity consumption in the US - worth about \$3 billion - was wasted by power supplies while the connected equipment is in standby mode. The percentage was predicted to reach 30% within 20 years if no action was taken.

The first mandatory energy-efficiency specifications for external adapters came into force in California in 2004. Similar standards were adopted worldwide, and became harmonized as the International Energy Efficiency Marking Protocol for External Power Supplies. Evolution of the protocol has imposed increasingly stringent limits on no-load power consumption and minimum average operating efficiency.

In 2014, the US Department of Energy (DoE) announced that all external power supplies (EPS) manufactured after February 10 2016 and marketed in the US must meet the new Level VI efficiency specification. The EU and other authorities, currently operating to Level V specifications, are expected to raise their own requirements to Level VI soon, although none have yet announced official regulations.

The new ruling applies to all external power supplies, whether they are shipped as standalone products or in the box with OEM equipment such as notebook PCs,

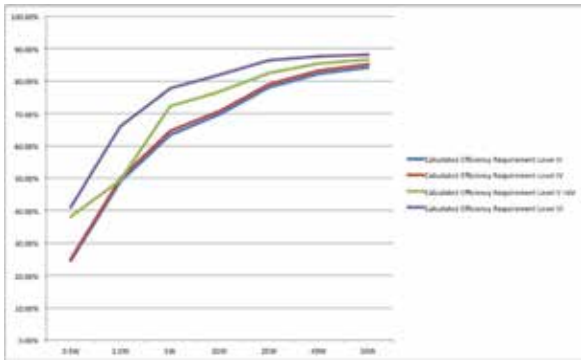


Figure 1. The Level VI minimum average efficiency requirement is significantly higher than in previous specifications

Power supply type		≤ 1W	1W- 49W	49W - 250W	≥ 250W
Single-Voltage AC/DC (output > 6V)	No load max.	0.1W	0.1W	0.21W	0.5W
	Dynamic efficiency (min.)	$0.5 \times P_{out} + 0.16$	$0.071 \times \ln(P_{out}) - 0.0014 \times P_{out} + 0.67$	0.880	0.875
Single-Voltage AC/AC	No load max.	0.21W	0.21W	0.21W	0.5W
	Dynamic efficiency (min.)	$0.5 \times P_{out} + 0.16$	$0.071 \times \ln(P_{out}) - 0.0014 \times P_{out} + 0.67$	0.880	0.875
Low-Voltage AC/DC (output < 6V)	No load max.	0.1W	0.1W	0.21W	0.5W
	Dynamic efficiency (min.)	$0.517 \times P_{out} + 0.087$	$0.0834 \times \ln(P_{out}) - 0.0014 \times P_{out} + 0.609$	0.870	0.875
Low-Voltage AC/AC	No load max.	0.21W	0.21W	0.21W	0.5W
	Dynamic efficiency (min.)	$0.517 \times P_{out} + 0.087$	$0.0834 \times \ln(P_{out}) - 0.0014 \times P_{out} + 0.609$	0.870	0.875
Multiple-Voltage	No load max.	0.3W	0.3W	0.3W	-
	Dynamic efficiency (min.)	$0.497 \times P_{out} + 0.067$	$0.075 \times \ln(P_{out}) + 0.561$	0.860	-

Table 1. Summary of no-load and dynamic efficiency targets for Level VI marking protocol

smartphones, tablets, printers, Internet hubs, routers, and IoT gateways. Given the expectation for explosive growth in IoT applications, the Level VI specification for external power supplies could be seen as providing valuable protection for the environment against the effects of the large numbers of IoT gateways soon to be connected to the power grid.

CUI began introducing Level VI products to its EPS range in late 2014, to address the new regulation. EPS manufacturers typically adjust their product portfolios to meet the highest mandatory standard, which enables OEM customers to maximize operational efficiency and eliminate supply-chain errors by shipping a common power supply type with products destined for multiple export markets.

The Level VI protocol is significantly more complex than its predecessors, and defines five categories of adapters including, for the first time, units rated over 250 W. Table 1 lists the specified no-load power and average efficiency for all categories covered.

Typical IoT gateways are unlikely to require a 250 W or multi-output adapter, but could be designed for use with a single-voltage AC/DC supply of above 6V or a sub-6V low-voltage supply in the under-1W or 1W-49W category. Figure 1 compares the minimum average efficiency specifications for Level VI single-voltage (output > 6V) power adapters against the Level III, Level IV and Level V specifications. The limit is significantly higher for units in the 0.5W-5W range that will likely power a large proportion of

IoT gateway devices. Depending on the application the gateway may be designed to make use of sleep modes, taking advantage of the lower no-load power consumption of the Level VI specification. Other applications may require the gateway to be active more or less continuously.

Meeting Level VI by Design

The new Level VI specifications present tough challenges to power supply designers. Compared with CUI's Level V power supplies, the Level VI units incorporate changes to almost every aspect of the primary and secondary-side circuitry. These have included designing-in the latest control ICs that support enhanced light-load operating modes: in normal operation the new controllers operate at the same 65 kHz switching frequency used in the Level V products, but change to 22 kHz at light-load and no-load to reduce power loss and improve efficiency. The capacitor and resistor values in the secondary feedback circuit have also been re-optimized to mitigate the effects of increased ripple and noise at lower switching frequencies. The control IC also takes advantage of new technologies to reduce quiescent power, which contributes further towards meeting the tougher maximum limits on no-load power consumption.

Changes in the secondary-side circuitry of low-voltage/high-current Level VI power supplies include adopting synchronous rectification using MOSFETs and a dedicated control IC, in place of simple

diode rectification. Other component changes include re-optimized resistance values, and the use of increased wire gauges to reduce internal power dissipation. Moreover, newer MOSFETs with lower on-state resistance help to raise efficiency at heavier loads.

On the other hand, the main power circuitry is arranged in much the same way as the previous Level V units. Units rated below 120 W use CUI's established flyback design, while adapters over 120 W use LLC resonant topology. It is worth noting that the increased average efficiency of the Level VI power supplies also helps to reduce the typical working temperature thereby boosting reliability. This can be a particularly important advantage in IoT applications, where equipment often is required to operate for long periods in the field with little or no maintenance.

Improvements for IoT and Environment

The US Environmental Protection Agency (EPA) has said the regulations imposed on external power supplies over the last decade have already cut CO2 emissions by more than 24 million tons per year and saved households \$2.5 billion annually. The US Department of Energy now believes enforcing Level VI will save around 47 million tons of CO2. Manufacturers of equipment such as IoT gateways need to keep abreast of the latest standards applicable to power supplies and energy.



LTE Global Overview and LTE for M2M Status

› Carlos Dyk, Quectel Wireless Solutions

LTE Global Deployment Status

The massive deployment of LTE by network operators worldwide has started. By the end of 2015, more than 440 operators had commercially launched LTE coverage in more than 150 countries. Around 90 percent of operators have deployed FDD mode, with 60 operators launching services in TDD mode in their networks. Eighteen operators have used both FDD and TDD.

Ninety-seven LTE-Advanced systems were launched in 48 different countries, while more than 140 operators are investing in LTE-Advanced in more than 60 different countries.

The following figure shows the LTE

Category per standard and the Peak Data Rate supported:

The following figure shows the number of LTE-Advanced systems launched per category:

What Is 3GPP Standard Status?

3GPP is the body in charge of defining the standard ruling for the development of cellular devices and network infrastructure. The body includes main companies and key players in the cellular world.

All components, hardware and software of cellular infrastructure and devices must comply with the 3GPP standard.

The following figure shows the main 3GPP releases and their main Data Rate Characteristics:

The 3GPP body releases a new

updated version every three to six months, making major and minor improvements to the actual standards.

The following figure shows the relationship between 3GPP releases, timeline and future features:

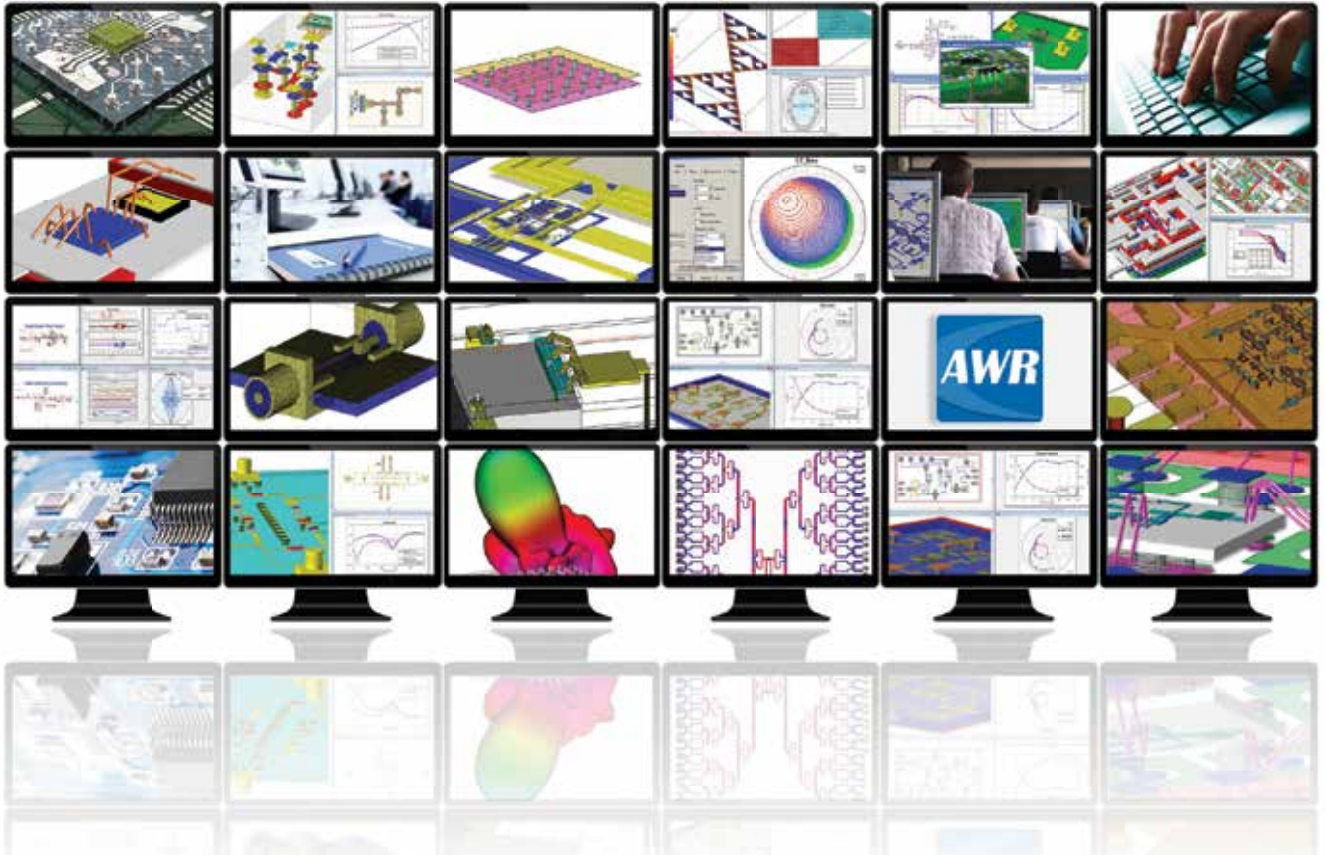
Device-2-Device (D2D)

An LTE Direct workshop organized by Qualcomm and Samsung in May 2013 brought together thought leaders from Deutsche Telekom, DOCOMO, KDDI, Orange, Placecast, Samsung, SAP, Sapien, SKT, Softbank, Tagged, and Verizon.

Workshop goals included understanding the business opportunity for proximate services in the mobile retail and social discovery space, discussing how operators can

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leverage LTE Direct to benefit from this space, and understanding key platform considerations for an LTE Direct deployment, which is currently being standardized in 3GPP as part of Release 12.

VoLTE (Voice Over LTE)

Current LTE M2M devices are classified not only by 3GPP category standards but also single or multi modes. A multi-mode LTE device supports fallback to 3G and even 2G when LTE coverage become weak or non-existent, while single-mode devices support LTE only. The voice call feature in a multi-mode device can be supported by falling back to GSM/WCDMA network service, then establishing the call.

In LTE only mode (or multi-mode devices implementing VoLTE), the call is established on LTE based on IMS (IP Mobile System) system network defined in 3GPP.

VoIP global status is growing fast, together with the new LTE network implementation. The current status is as follows:

- 111 operators are investing in VoLTE in 52 countries (deployments, trials, studies)

- 30 operators commercially launched VoLTE HD voice in 21 countries

LTE Category 1

The LTE Category 1 specifically addresses the needs of M2M device makers for an especially low cost solution. Cat 1 provides up to 10 Mbps in downlink and has been part of the earliest 3GPP LTE specifications, in Release 8. Cellular operators can deploy LTE Cat 1 device support with no need for new network equipment or major upgrades, allowing them to manage their networks more efficiently by not allocating excessive resources to devices that require low throughput. Cat 1 provides meaningful

UE CATEGORY	PEAK DOWNLINK Mbps	PEAK UPLINK Mbps
Cat 4	150	50
Cat 6	300	50
Cat 9	450	50
Cat 11	600	50

Figure 1

UE Category	Launched
Cat 4	14
Cat 6	78
Cat 9	4
Cat 11	1
Total	97

Figure 2

cost and power reductions compared to today's Cat 3 (up to 100Mbps) and Cat 4 (up to 150Mbps).

A few networks are already configured to allow Cat 1 devices, and more are expected to follow in the next few months. Now that LTE Cat 1 chipsets are available, we will see Cat 1 devices ramping up steadily in 2016.

Release 13 - LTE-M (MTC)

Category 0 (up to 1 Mbps) is still being defined in 3GPP's Release 12 LTE standard. 3GPP Release 12 introduces Cat 0 for the first time and defines features for M2M, specifically for what the 3GPP calls Machine Type Communications, or MTC. When it becomes fully defined, it will describe significant reductions in complexity and address the need for battery-powered devices consuming far less

power and at a lower cost than their 3G and 4G counterparts. Cat 0 will mean big changes for the operators in terms of the infrastructure and in the way they manage and allocate spectrum. LTE-M (up to 200 Kbps) is associated with the forthcoming Release-13 standard.

LTE-M will support the following capabilities:

- Reduced device bandwidth of 1.4 MHz in downlink and uplink
- Reduced maximum transmit power of 20 dBm
- Reduced support for downlink transmission modes
- Further device processing relaxations are under consideration

PSM Power-Saving Mode

In 3GPP Release 12, a device power-saving mode (PSM) was introduced, enabling a significant improvement in device battery life. If the device supports PSM, it asks the network for a certain active timer value during an attach or tracking area update procedure; the active timer determines the duration for which

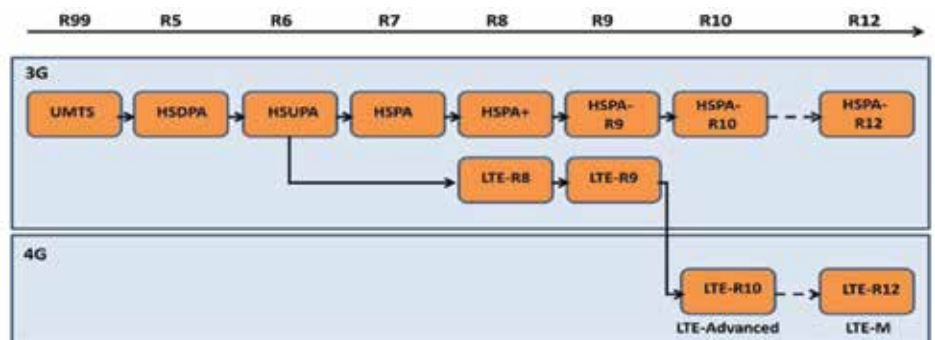


Figure 3

the device remains reachable for a mobile terminated transaction moving from connected to idle mode. The device starts the active timer when it transactions from connected to idle mode. When the active timer expires, the device moves to power-saving mode. While the device remains in power-saving mode, it is not reachable as it does not check for paging, but it is still registered with the network. The device remains in PSM until a mobile-originated transaction occurs.

The PSM will significantly increase and extend the device's battery life, increasing the DRX cycle (Discontinuous Reception) with different transaction cycles for an LTE-M device.

Using Release 12 PSM with 10 minutes' DRX cycle and a weekly transaction cycle may extend a typical 1500mAh battery's life to more than 10 years.

Main Characteristics of PSM:

- Enhanced power-saving mode (PSM) Efficiently turning OFF-ON modem, optimized for device-originated or scheduled applications

- Extended Discontinuous Reception (DRX)

Longer sleep cycles optimized for delay-tolerant, device-terminated

applications

- Connectionless Random Access Channel (RACH)

Data transmissions via a common channel for more efficient transition between states

- Less frequent Tracking Area Updates (TAUs) and measurements

Configurable for low-to zero-mobility M2M applications

Conclusion

It is widely accepted that LTE will be used for nearly everything that requires a wireless connection, including M2M and IoT applications where it was once deemed too expensive and complex. LTE means more than high throughput; it offers better spectral efficiency, longevity, scalability and economic benefits for device makers and operators. The migration to LTE has already started for M2M and IoT businesses, and all connected devices, from the high-tier smart phone to the lowest utility meter or wearable device, will be LTE.

LTE Category M will be on 3GPP implementation till the end of 2017, with commercial deployment in 2019.

In the current scheme of deployment of 3GPP Rel-12 and Rel-13 LTE for M2M

standards, looking at the long period of integration in M2M/IoT products/systems and regional carrier plans, it will take some time to transition and switch on toward full Machine Type Communications LTE-M support, while the LTE Category 1 will perfectly fit M2M needs in terms of complexity, price and functionality.

Quectel Is Developing LTE-Cat1 Module Tailored for M2M/IoT Applications

Quectel Wireless Solutions, a leading global supplier of GSM/GPRS, UMTS/HSPA/LTE and GNSS modules, solutions and services, will launch the LTE-Cat 1 module optimized specially for M2M and IoT applications in Q2, 2016. Samples of this module will be available in Q1, 2016.

Key Benefit of Quectel LTE-Cat1 Module:

- Low-cost, low-power LTE connectivity optimized for broadband IoT applications
- Worldwide LTE and UMTS/HSPA+ and GSM/GPRS/EDGE coverage
- MIMO technology meets demands for data rate and link reliability in modem wireless communication systems
- GNSS receiver available for applications requiring fast and accurate fixes in any environment
- Embedded power management unit (PMU) featuring ultra-low deep sleep current consumption

For more information visit our web site

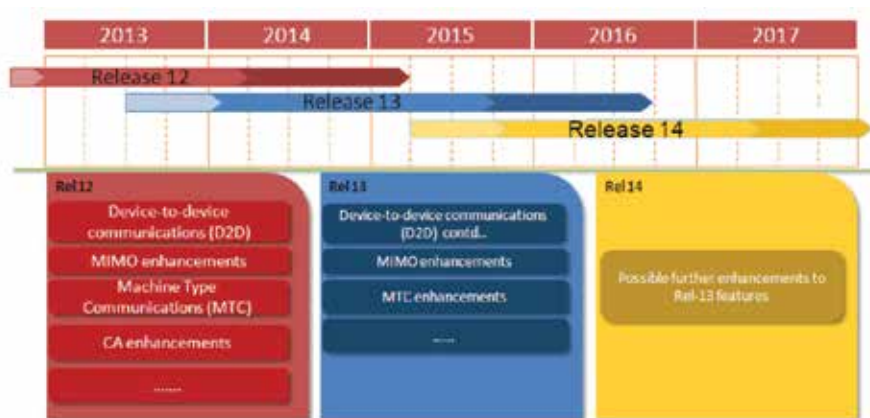


Figure 4



A Novel Approach to Software-Defined FPGA Computing

› **Stephane Monboisset, QuickPlay**

With the rise of the Internet of Things and Big Data processing, the need for transferring and processing data has skyrocketed, and CPUs alone can no longer address the exponential increase. Adding more processors and more virtual machines to run a given application just doesn't cut it, as there is only so much that can be parallelized on multiple CPUs for a given application. Field-programmable gate arrays, on the other hand, have the requisite I/O bandwidth and processing power, not only from a pure processing standpoint but, equally important, from a power standpoint. For data-center equipment manufacturers, the use of FPGAs has long been an appealing prospect. Intel's recent acquisition of the second-largest FPGA vendor is further testament that a CPU-only solution no longer suffices. The major roadblock to more-

widespread FPGA adoption has been the complexity of implementing them. Until now, the only way to develop an application on an FPGA-based platform has been to deal with some of the lowest levels of hardware implementation. This has kept a large potential customer base—software developers—away from the devices and has made life increasingly complicated for traditional FPGA designers.

Recent methodologies for FPGA design, centered on high-level synthesis (HLS) tools and leveraging software programming languages such as OpenCL™, C and C++, have provided a sandbox for software developers to reap the benefits of FPGA-based hardware acceleration in numerous applications. But the methodologies often fall short in one essential respect: enabling software developers to define and configure, on their own, the hardware infrastructure

best suited for their application. The industry has continued to pursue the holy grail of a high-level workflow for implementing applications on FPGA-based platforms that does not require specific FPGA expertise.

Over the past five years, PLDA has developed just such a workflow. Called QuickPlay, it efficiently addresses the implementation complexity challenge and enables multiple use models for FPGA development. But one of its core sources of value is the way in which it lets software developers take applications intended for CPUs and implement them, partially or fully, on FPGA hardware. QuickPlay leverages all of the FPGA resources, turning these powerful but complex devices into software-defined platforms that yield the benefits of FPGAs without the pain of hardware design.

Consider a software algorithm that can be broken down into two functions:

Data is processed into one function and is then sent to another for further processing. From a software perspective, this implementation is as simple as a call to Function1() followed by a separate call to Function2(), using pointers to the location of the data to be processed.

Implementing such an algorithm on an FPGA-based hardware platform without the right hardware abstraction tool flow would require the software developer to come up with a hardware design resembling that in Figure 1 (where Kernel 1 and Kernel 2 are the respective hardware implementations of Function 1 and Function 2). The hardware design would need to include two elements: the control plane and the data plane.

The control plane is the execution engine that generates clocks and resets, manages system startup, orchestrates data plane operations, and performs all housekeeping functions. The data plane instantiates and connects the processing elements, Kernel 1 and Kernel 2, as well as the necessary I/O interfaces required to read data in and write processed data out. In our example, those interfaces are Ethernet and PCI Express (PCIe), as Figure 1 shows, though different application requirements will call for different I/O interfaces.

A software developer could easily generate Kernel 1 and Kernel 2 using an HLS tool that compiles the software functions Function1() and Function2(), typically written in C or C++, into FPGA hardware descriptions in VHDL or Verilog, without requiring

specific hardware expertise. Every other element in the design that is not algorithmic in nature (interfaces, control, clocks and resets), however, could not be generated with HLS tools, and hardware designers would have to design them as custom hardware description language functions or IP. The job of sourcing those elements and connecting them poses yet another challenge, as some elements may not be readily available or may have different interfaces (type and size), clocking requirements, specific startup sequences and so on. Beyond the design work-and equally challenging-is the implementation work, which includes mapping the design onto the resources of the selected FPGA platform, generating the appropriate constraints, and confirming that those constraints are met after logic synthesis and implementation on the FPGA

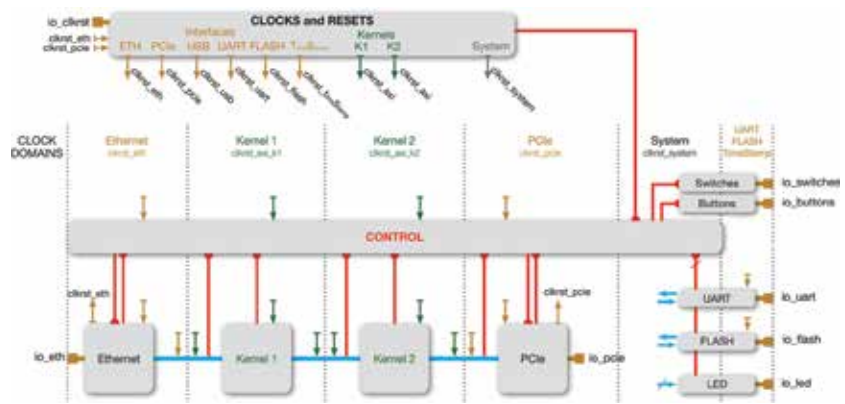


Figure 1: A detailed hardware implementation of a two-function algorithm using traditional FPGA tools

hardware. It can take even an experienced hardware designer weeks to achieve a working design on a new piece of FPGA hardware.

Thus, any tool that aims to enable software developers to augment their applications with custom hardware must be able to:

- create functional hardware from pure software code;
- incorporate existing hardware IP blocks if needed;
- infer and create all of the support hardware (interfaces, control, clocks, etc.);
- support the use of commercial, off-the-shelf boards and custom platforms;
- ensure that the generated hardware is correct by construction so that it requires no hardware debug; and
- support debug of functional blocks using standard software debug tools only.

PLDA engineered QuickPlay from the ground up to meet all of those requirements, thereby enabling pure software developers to specify, build and integrate FPGAs into their software architectures with minimal effort.

SOFTWARE-CENTRIC METHODOLOGY
The overall process of implementing a design using QuickPlay is straightforward:

1. Develop a C/C++ functional model of the hardware engine.

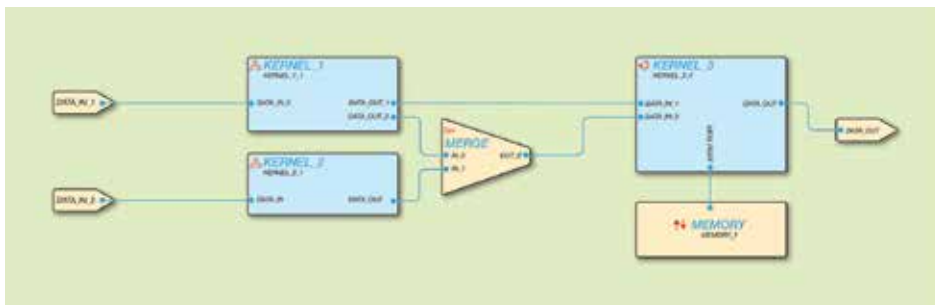


Figure 2 : A design example in QuickPlay

2. Verify the functional model with standard C/C++ debug tools.
3. Specify the target FPGA platform and I/O interfaces (PCIe, Ethernet, DDR, QDR, etc.).
4. Compile and build the hardware engine.

The process seems simple; but if it is to work seamlessly, it is critical that the generated hardware engine be guaranteed to function identically to the original software model. In other words, the functional model must be deterministic so that, no matter how fast the hardware implementation runs, both hardware and software executions will yield the exact same results.

Unfortunately, most parallel systems suffer from nondeterministic execution. Multithreaded software execution, for example, depends on the CPU, on the OS and on nonrelated processes running on the same host. Multiple runs of the same multithreaded program can have different behaviors. Such nondeterminism in hardware would be a nightmare, as it would require debugging the hardware engine itself, at the electrical waveform level, and thus would defeat the purpose of a tool aimed at abstracting hardware to software developers.

QuickPlay uses an intuitive dataflow model that mathematically guarantees deterministic execution, regardless of the execution engine. The model consists of concurrent functions, called kernels, communicating with streaming channels. It thus correlates well with how a software developer might sketch an application on a whiteboard. To guarantee deterministic behavior, the kernels must communicate with each other in a way that prevents data hazards, such as race conditions and deadlocks. This is achieved with streaming channels that are (1) FIFO-based, (2) blocking read and blocking write, and (3) point-to-point.

Those are the characteristics of a Kahn Process Network (KPN), the computation model on which PLDA built QuickPlay. Figure 2 shows a QuickPlay design example illustrating the KPN model.

The contents of any kernel can be arbitrary C/C++ code, third-party IP or even HDL code (for the hardware designers). QuickPlay then features a straightforward design flow (Figure 3). Let's take a closer look at each step of the QuickPlay design process.

Step 1: Pure software design. At this stage you create your FPGA design by

adding and connecting processing kernels in C and by specifying the communication channels with your host software. QuickPlay's Eclipse-based integrated development environment (IDE) provides a C/C++ library with a simple API to create kernels, streams, streaming ports and memory ports, and to read and write to and from streaming ports and memory ports.

In addition, the QuickPlay IDE provides an intuitive graphical editor that allows you to drag and drop kernels and other design elements and to draw streams.

Step 2: Functional verification. In this step, the focus is on making sure that the software model written in Step 1 works correctly. You do this by compiling the software model on the desktop, executing it with a test program that sends data to the inputs, and verifying the correctness of the outputs. The software model of the FPGA design is executed in parallel, with a distinct thread for each kernel to mimic the parallelism of the actual hardware implementation.

You would then debug your software model using standard software debug techniques and tools such as breakpoints, watchpoints, step-by-step execution and printf. (You will probably want to run more tests once the implementation is in hardware; we'll deal with that shortly.) From a design flow standpoint, this is where you do all of your verification. Once you are done with this debug phase and have fixed all functional issues, you will not need any further debugging at the hardware level.

It's important to remember that the functional model involves none of the hardware infrastructure elements. In the example above, the focus is on a simple, two-function model; none of the system aspects added in Figure 1 (such as the communication components, the control plane, and clocking and resets) are in play during this modeling and verification phase.

Step 3: Hardware generation. This

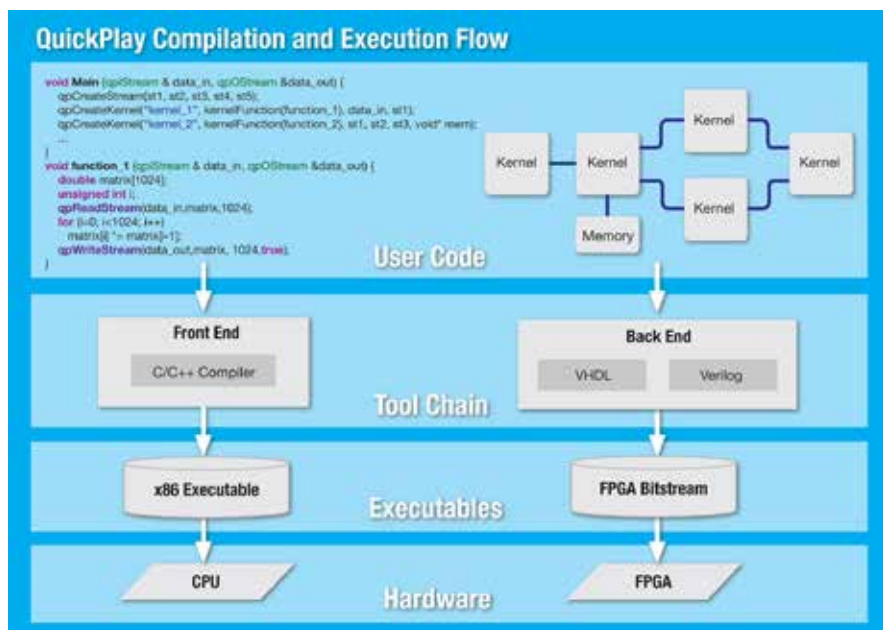


Figure 3: QuickPlay features a straightforward design flow



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step generates the FPGA hardware from your software model. It involves three simple actions:

1. Using a drop-down menu in the QuickPlay GUI, select the FPGA hardware into which you want to implement your design. QuickPlay can implement designs on a growing selection of off-the-shelf boards that feature leading-edge Xilinx® All Programmable FPGAs, PCIe 3.0, 10-Gbit Ethernet, DDR3 SDRAM, QDR2+ SRAM and more.

2. Select the physical interfaces (and therefore the protocols) to map to the design input and output ports. These are also simple menu selections. The choice will depend on the interfaces that are available on the FPGA board you have selected, such as PCIe, TCP/IP over 10-Gbit Ethernet and UDP over 10-Gbit Ethernet. Selecting the communication protocol automatically invokes not only the hardware IP block required to implement the connection, but also any software stacks layered over it, so that the complete system is created.

3. Launch the build process. This will run the HLS engine (creating hardware from C code), create the needed system hardware functions (the control plane logic in our original example) and run any other tools necessary (for example, Xilinx's Vivado® integrated design

environment) to build the hardware images that the board will require. No manual intervention is required to complete this process.

Step 4: System execution. This is similar to the execution of the functional model in Step 2 (functional verification), except that now, while the host application still runs in software, the FPGA design runs on the selected FPGA board. This means that you can stream real data in and out of the FPGA board and thereby benefit from additional verification coverage of your function. Because this will run so much faster, and because you can use live data sources, you are likely to run many more tests at this stage than you could during functional verification.

Step 5: System debug. Because you're running so many more tests now than you were doing during the functional verification phase, you're likely to uncover functional bugs that weren't uncovered in Step 2. So how do you debug now?

As already noted, you never have to debug at the hardware level, even if a bug is discovered after executing a function in hardware. Because QuickPlay guarantees functional equivalence between the software model and the hardware implementation, any bug in the hardware version has to exist in the software version as well. This is why

you don't need to debug in hardware; you can debug exclusively in the software domain.

Once you have identified the test sequence that failed in hardware, QuickPlay can capture the sequence of events at the input of the design that generated the faulty operation and replay it back into the software environment, where you can now do your debug and identify the source of the bug using the Eclipse debugger.

This is possible because QuickPlay automatically provisions hardware with infrastructure for observing all of the critical points of the design. You can disable this infrastructure to free up valuable hardware real estate. Figure 4 shows the example system with added debug circuitry. Figure 4 shows the example system with added debug circuitry. Without QuickPlay, some sort of debug infrastructure would have to be inserted and managed by hand; with QuickPlay, this all becomes automatic and transparent to the software developer.

The overall process is to model in software, then build the system and test in hardware. If there are any bugs, import the failing test sequences back into the software environment, debug there, fix the source code and then repeat the process. This represents a dramatic productivity improvement over traditional flows.

Step 6 (optional): System optimization. Once you have completed the debug phase, you have a functional design that operates on the FPGA board correctly. You may want to make some performance optimizations, however, and this is the proper time to do that, as you already know that your system is running correctly.

The first optimization you should consider is to refine your functional model. There are probably additional concurrency opportunities available; for example, you might try decomposing or refactoring functions in a different way. At this level, optimizations can yield spectacular performance improvements. Needless to say, doing so with a VHDL or Verilog

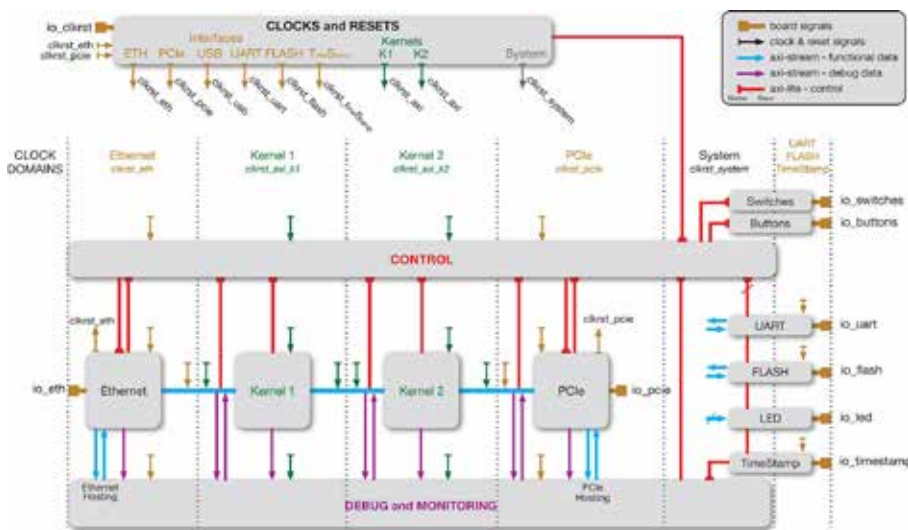


Figure 4: The debug infrastructure is automatically created

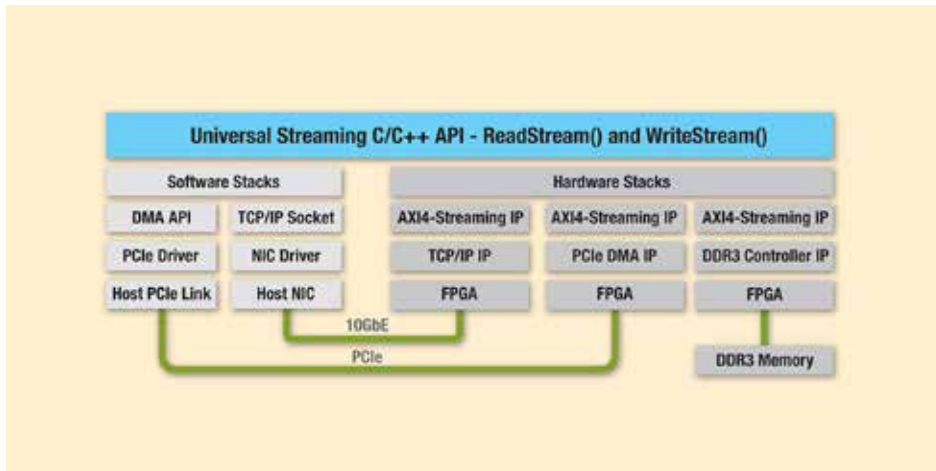


Figure 5: Selecting the desired protocol sets up the required hardware and software stacks

design would require significant time, whereas doing the modifications in C would be a quick and straightforward process.

Second, you may want to try a different FPGA board with a faster FPGA. Because the mapping from the functional model to the board is so easy, it's a simple matter to try a variety of boards in order to select the optimal one.

The third optimization has to do with the hardware kernels that QuickPlay creates via high-level synthesis. While the resulting hardware is guaranteed to operate correctly and efficiently, it may not operate as efficiently as hardware handcrafted by a hardware engineer. At this stage, you have several options: You can optimize your code and tune QuickPlay HLS settings to improve the generated hardware, use Vivado HLS to generate more-efficient hardware, or have a hardware designer handcraft the most critical blocks in HDL.

None of these optimization steps is mandatory, but they provide options when you need better-performing hardware and have limited hardware design resources available. A hardware engineer may be able to help with these optimizations. Once you have made any of these changes, simply repeat the build process.

A UNIVERSAL STREAMING CONDUIT
QuickPlay provides a universal streaming API that entirely abstracts away the

underlying physical communication protocol. Streaming data is received via the ReadStream() function and is sent out using the WriteStream() function. Those functions can be used to send and receive data between kernels, to embedded or board-level memory, or to an embedded or external host CPU, thus providing broad architectural flexibility with no need for the developer to comprehend or manage the underlying low-level protocols.

The selected protocol determines the hardware through which that data arrives and departs. At present, QuickPlay supports ARM® AMBA® AXI4-Stream, DDR3, PCIe (with DMA) and TCP/IP; more protocols are being added and will be added as demand dictates. Selecting the desired protocol sets up not only the hardware needed to implement the protocol, but also the software stacks required to support the higher protocol layers, as shown in Figure 5.

QuickPlay manages the exact implementation of these reads and writes (size, alignment, marshaling, etc.). The most important characteristic of the ReadStream() and WriteStream() statements is that they are blocking: When either statement is encountered, execution will not pass to the next statement until all of the expected data has been read or written. This is important for realizing the determinism of the algorithm.

The "binding" between the generic ReadStream() and WriteStream() statements and the actual underlying protocol hardware occurs at runtime via the QuickPlay Library. This not only prevents the communication details from cluttering up the software program, but also provides modularity and portability. The communication protocol can easily be changed without requiring any changes to the actual kernel code or host software. The ReadStream() and WriteStream() statements will automatically bind to whichever protocol has been selected, with no effect on program semantics. As a result of the abstraction that QuickPlay provides, the software algorithms remain pure, focusing solely on data manipulation in a manner that's completely independent of the underlying communication details.

PRODUCTION-QUALITY OUTPUT
Depending on the HLS tool being used, results might be improved by learning coding styles that result in more efficient hardware generation, but that is optional.

While in other situations the hardware platform you use may be viewed simply as a prototyping vehicle, the systems you create using QuickPlay are production-worthy. Going from a purely software implementation to a hardware-assisted or hardware-only implementation traditionally takes months. QuickPlay reduces that time to days.

The QuickPlay methodology achieves the long-sought goal of allowing software engineers to create hardware implementations of all or portions of their application. By working in their familiar domain, software engineers can make use of custom hardware as needed, automatically generating hardware-augmented applications that operate more efficiently and can be production-ready months ahead of handcrafted designs.



A Flexible Future for Cabling

> Molex Team

Italian-based manufacturer Flamar, a recent Molex acquisition, specialises in high performance cabling solutions for machine and process control. Deployed in industrial, automation, robotics, broadcast audio/video, and telecommunications applications, each cable is custom-designed by Flamar from first principles. Vittorio Bogoni, Export Sales Manager, Flamar looks at the company's history and how it is opening up its market offering for non-customised cabling products.

Founded in 1975, Flamar Cavi Elettrici was a family-owned company. The company started manufacturing coaxial cable for automotive and satellite applications. However, with its relatively simple design, manufacturing for the majority of this type of cable migrated to China in the mid-80s. Over the years, the company has matured a vast experience developing high quality cabling solutions for industrial automation, robotics, broadcast audio/video, and telecommunications and in applications where a high technical solution is required. Working very closely with its customers Flamar knows and understands the applications which

results in the best possible cable solution. Quality, reliability and accuracy are the key mantras for Flamar; the company's technologically advanced production facility backed by a flexible organisational structure, enables it to react quickly on a constantly changing market.

RF & Satellite cables

Today, Flamar still manufactures coaxial cable, though more on the sophisticated end of the design spectrum. They are predominantly used for RF signal transmission in fixed or mobile installations, both for industry (network, radio, broadcast) and consumer (HDTV, sound, security) applications. Their precise construction with tight tolerances, combined with use of high quality materials are key factors to guarantee accurate mechanical and electrical characteristics. This is because signal quality is often limited by the cable construction.

Flamar manufactures coax cables with single or double braided shield in plain and tin plated copper. For specific requirements this braid can also be combined with Aluminium/Pet foils with different thicknesses.

In professional broadcasting

applications, where high noise immunity is key, more focus is placed on the effectiveness of the shielding. To achieve the optimum shielding efficiency, Flamar has developed a technique that combines a braiding of either Aluminium/Pet or Aluminium foil. Some high flexibility cables from Flamar are designed with better thermal and mechanical characteristic specifically for OEMs looking to use coaxial cabling in the automation and automotive industry. For these dynamic applications, a foam or solid PE dielectric is used with different density levels.

In addition, Flamar offers coaxial cables with a variety of outer jacket materials, ranging from PVC, non-migration PVC, PE, LSOH materials and PUR, which is both water and UV resistant. They are available in a wide range of colours according to RAL or even custom colours. Printing is also available by ink-jet or by printing wheel.

Multimedia cables

The communication infrastructure is constantly developing, in 1975 it was mainly based on analogue technology and today it is much more digital. Although wireless technologies are more

frequently being used for the download of films to tablets and smart-TVs, the majority of digital information being transmitted for multimedia applications is via cable. Typical applications can be seen in sport centres, airports and conference centres, and for high-end applications in media centres, radio and TV stations, live shows and musical productions. Here, these cables have to perform with high precision, maintaining stable impedance values and low dielectric loss.

For optimum transmission quality, Flamar develops and manufactures braided and wrapped shielding in plain copper and tin. The use of very fine copper wires (0.10 mm) in combination with a high performance abrasion resistant outer jacket material, which can be also water and UV resistant, gives a range of products for high-end professional use.

Cables for Industrial Automation

Growing automatization in the industry and the support of robots, automation systems and process control to assist manual production processes makes this range of cables one of the most important ones. A comprehensive range of cables for Sensors, Measurement, Controls, Robotics and Drives applications, assuring excellent performance, quality and durability for this industrial sector, is available from Flamar.

Sensor cables are used to measure weight, temperature, pressure, flow position, level, vibration, and movement and can be terminated to M8 and M12 connector systems. A full range of sensor cables suitable for fixed and moving installations, for a broad spectrum of applications ranging from those found in the hygienic food and medical industries to oil & gas and other hazardous environments, is available.

Suitable for fixed and occasionally moving installations, control cables are mainly used in control and measuring equipment such as assembly line tools, conveyors, control panels and generally where connectivity is required. Ranging from 0.50 mm² up to 2.50 mm², control cables are constructed in a way that they are easy to handle, to strip, to

cut and to terminate.

Flamar uses copper and tin-plated copper braid, aluminium polyester foils and combinations of these to screen against the effects of EMI. In addition, flame retardant PVC, polyolefin compounds and a wide selection of polyurethanes can be used in combination to achieve a small bending radius, high-flex characteristics, low friction and mechanical stress properties and resistance to oils and chemical substances at a suitable price/performance level.

Cables for Drag Chains

Drag chains or cable chains are special chains designed to protect and guide flexible cable or hydraulic and pneumatic hoses connected to moving automated machines and equipment. Typical applications include machine tools, cranes, car wash equipment, medical and laboratory equipment, automatic warehousing, forklifts, industrial robots and offshore oil rigs. The purpose of these chains is to reduce wear and stress on the cables and hoses, as well as give them good protection against the operating environment and to also help improve operator safety.

For these applications, Flamar offers flexible and hi-flex cables that meet the highest quality levels and are available with UL/CSA approvals. A normal flexible cable might withstand 10,000 to 50,000 cycles, whereas a drag chain cable can handle between 1 and 5 million cycles. A key factor for these cables is that they are rigorously tested to prove operational reliability, which meets all applicable standards and directives.

To achieve these high performance levels, plain and tin-plated copper wires with pitch and stranding optimised for a longer life time are used. PP or TPE extruded insulation reduces cable dimensions and improves the mechanical properties.

Special & Hybrid Cables

Designing and manufacturing custom made hybrid cables, suitable for applications with low voltage and power conductors, together with coax data and transmission elements is one of the key characteristics Flamar is known for. In addition to combinations of copper conductors, these cables can

also contain a large number of other components such as pneumatic and hydraulic hoses that integrate aramid fibres for mechanical reinforcement. The integration of many different components into one hybrid cable takes less space and allows a faster installation than traditional individual elements.

Future Developments

As well as developing, manufacturing and supplying custom cable, the company will now offer a range of standard cables. One such cable is the Flamar-Flex cable. Designed for dynamic applications, the cable can operate reliably and safely in extremely small bending radius applications – as tight as 5x outside diameter.

Flamar-Flex cables are designed with performance in mind. Rather than have the insulation applied under pressure it is instead extruded over the copper strand. This makes the insulation easy to strip – especially for larger cross-sections (4 or 6mm²). The special extrusion technique allows space between each copper strands compared to insulation applied under pressure, which typically is very thick and difficult to strip. An additional benefit to the “tube” extrusion technique is that less insulation material is used, making it cheaper, more lightweight and flexible. These cables are tested and proven to more than 5 million cycles.

Another new concept of this cable is its outer jacket, which uses a new type of polyurethane. Typical UL/CSA outer jackets are rated for temperatures up to 80°C, however this new TPU is rated up to 90°C. The new type of polyurethane outer jacket of the Flamar-Flex cable has been tested to temperatures of at least 90°C - the cable is UL/CSA approved (style 21209 / 21757) for temperature ranges of -50 to +90°C. In addition, it is oil-resistant (EN 50363-10, VDE 7472-803/B and UL1581/758), flame-retardant (IEC 60332-1, VW1, FT1, UL Vertical Flame Test) and Halogen-free (IEC 60754-1, EN 50267-2-1, VDE 0472-815).



Hi-Rel Screening of LTCC Filters for Space Applications

› Sookai Ramkarran, Ron Beagle, Arthur Ackerman and Brandon Kaplan, Mini-Circuits

The extreme operating conditions of the space environment combined with lack of access for repairs and zero tolerance for failure necessitate intensive qualification of electronic parts used in space missions. Mini-Circuits has a successful track record of supplying components for space applications, and our experience in this area has led to robust testing and qualification processes for the parts we supply for these systems.

Qualification requirements for space applications vary by program, materials and component type. Mini-Circuits offers a variety of components available for hi-rel screening including amplifiers, mixers, filters, limiters, attenuators, and more. Mini-

Circuits' LTCC filters feature rugged ceramic construction, wide operating temperature range (-55 to +100°C), and high power handling in a tiny device size, making them excellent candidates for hi-rel applications. This article will describe the qualification process for a surface-mount LTCC low pass filter supplied for use in a particular spaceborne system. This is a case study intended to highlight Mini-Circuits' advanced capabilities in meeting qualification requirements to ensure high reliability for space missions, but is by no means an exhaustive representation of our qualification processes.

Screening Requirements

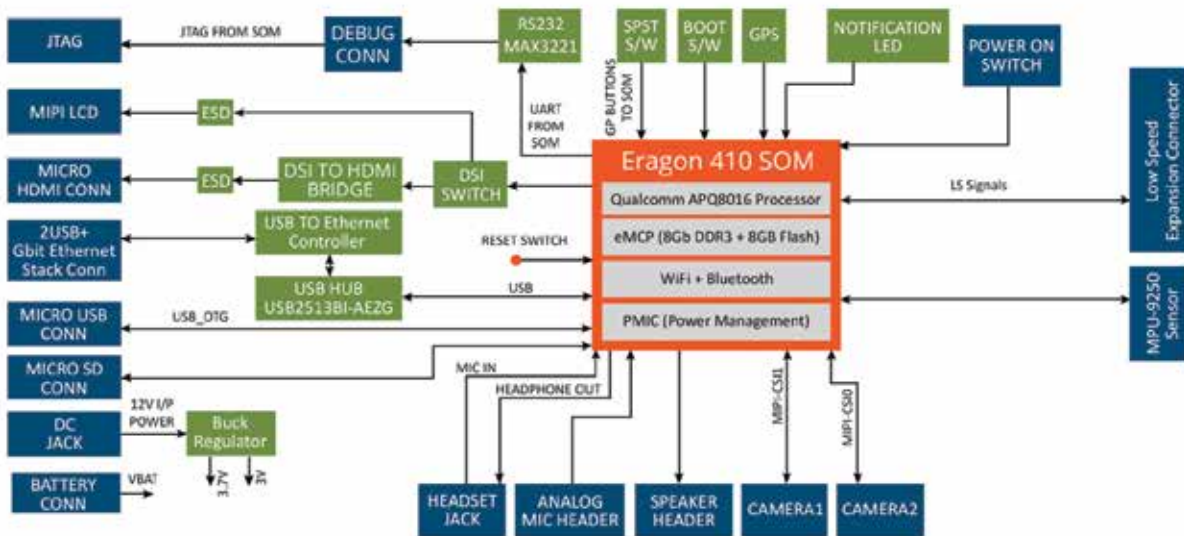
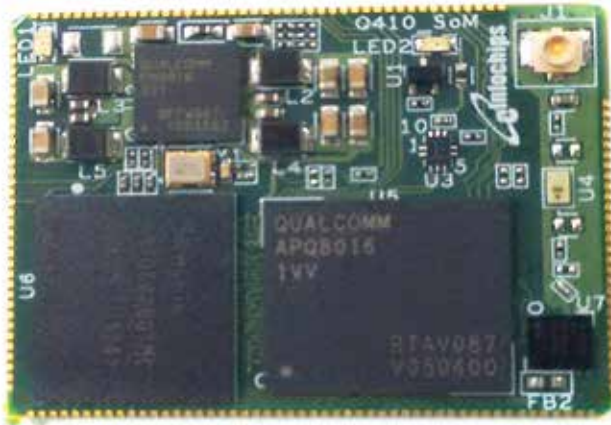
The LTCC filter screened for in this

case is a modification of standard model LFCN-8400+ satisfying a series of special screening requirements defined by a specific space flight program. The special model satisfies a material restriction that the unit terminations be constructed with tin-lead finish with a maximum tin content of 97%. This is a standard requirement to prevent tin whisker growth. The special part also satisfies a date code restriction that shipped parts may be from a maximum of two lot date codes. If parts are shipped from two lots, one lot must be from new production and both lots must have passed screening independently. Destructive Physical Analysis (DPA) is required on sample units from lots used for production to verify construction

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and termination composition. Units must also undergo a rigorous program of reliability testing including real time radiographic inspection in three views. The full qualification process performed to meet the program requirements is summarized below.

Qualification Process

1. Destructive Physical Analysis (DPA)

Prior to starting reliability testing, DPA is performed on 3 randomly selected sample units to verify the construction and termination composition on the lot to be used for production. MIL-STD-1580B is used to establish a general process for performing DPA on the units under test, but because pass/fail criteria for LTCC unites are not defined by the standard, it is used as a guideline, and the units under test are compared to determine if there are any apparent anomalies. The DPA pass/fail criteria are summarized in Table 1.

2. Reliability Testing

Following DPA, reliability testing consists of testing at 100% (Group A) and small sample testing (Group B) for a number of parameters summarized in Table 1.

Conclusion

The qualification process presented here satisfies requirements for an LTCC low pass filter to be used in a particular space application. Mini-Circuits' line of LTCC filters includes over 195 high-pass, low-pass and band-pass models available for hi-rel screening in addition to a wide selection of hi-rel mixers, amplifiers, attenuators, limiters, and other

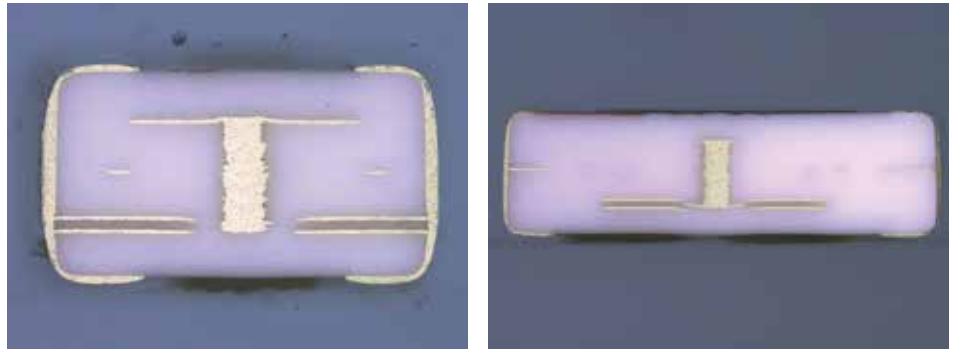


Figure 1: Overall view of sectioned device from DPA (Parallel and Transverse)

DPA					
Test	Condition/s	Duration or Cycles	Reference	Sample Size	Pass/Fail Criteria
DPA	Sample units sectioned along 2 planes (parallel and transverse)	-	MIL-STD-1580B Para. 14.1.1.1 Para. 14.1.1.3	3 Units	a) External visual inspection b) Prohibited materials analysis of external surfaces c) Internal visual inspection of sectioned devices
GROUP A – 100% Screening					
Test	Condition/s	Duration or Cycles	Reference	Sample Size	Pass/Fail Criteria
Thermal Shock	-55/+125°C	10 Cycles, 10 Min.	MIL-STD-202, Method 107	100%	Pass electrical
Bake-In	24 hr. stabilization bake exposure at +100°	24 hr.	QCP-06-21	100%	Pass electrical
Real Time Radiographic Inspection	3 views	-	MIL-STD-202 Method 209	100%	Voids in the insulator, alignment of internal elements, attachment between internal layers, foreign material, terminal attachment
Final Visual and Mechanical Inspection	10x magnification; 5 units inspected for dimension	-	-	100%	External Visual Inspection
GROUP B – Sample Screening					
Test	Condition/s	Duration or Cycles	Reference	Sample Size	Pass/Fail Criteria
Humidity	+85°C and +85RH, 1.3VDC ±0.25VDC test voltage applied	240 hr.	-	12 Units	a) Pass Electrical b) Visual Inspection
Destructive Electrical Screening	Standard Electrical Measurements @ +25°C, -55°C, and +100°C; samples soldered on PCB	-	-	10 Units	Pass Electrical at +25°C; Summary data provided for all testing
Solderability	Units soldered on test board and inspected per IPC-A-610	-	MIL-STD-202 Method 208	5 Units	Meet requirements of MIL-STD-202
Leach Resistance	Immersion in +260°C solder	10 sec.	MIL-STD-202	3 Units	a) Visual Inspection b) Electrical Test c) Bubble Test
Terminal Strength	Push force of 0.5mm/s applied to samples soldered to test board	until electrode pads are peeled off or ceramic is broken	MIL-STD-202 Method 211	3 Units	1 kg minimum solder strength

Table 1: Screening process summary

components suitable for space applications. Requirements vary widely depending on many factors including the component type, materials, and other details specific to the flight program. Mini-Circuits has successfully screened hi-rel components for a range of space requirements, and this experience has enabled us to develop well-established qualification processes for these demanding applications. For more information about qualifying parts for space applications, please contact our applications team

Qualification Flow

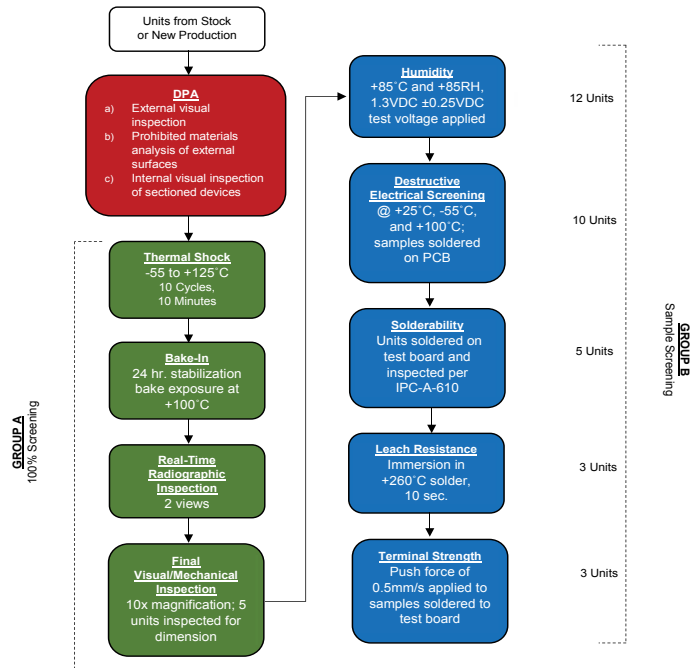


Table 1: Screening process summary



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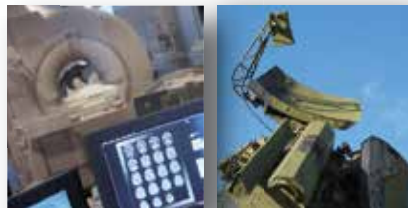
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A Revolutionary Approach to Eliminating Power

› Mike Salas, Ambiq Micro

One company in Austin, Texas is about to change the way electronics are powered.

The Internet of Things and the advent of ubiquitous computing have highlighted the importance of reducing power consumption throughout electronics.

If the immediate future will truly see the networking of all electronics and hitherto unconnected devices then the real prize is not to maximise the performance of the technology - the performance is fast enough to maintain an IoT already - it is to reduce energy consumption enough that the electronic things can function meaningfully within this new internet. Energy is consumed in two fundamental ways: as leakage, when

a circuit's state isn't changing, and dynamically as internal nodes are charged up and down. For realistic circuits in operation, dynamic power dominates - especially for the higher power supply voltages used in most designs today (see Figure 1).

Dynamic energy is determined by operating voltage

Sub-threshold techniques are a way to create circuits that consume dramatically less energy than those built using standard design practices. Sub-threshold design is challenging, but, given the right experience and diligence, it can be done and with immense benefits.

The results are circuits that provide

the same functions as more traditional ones but use a fraction of the energy. There is no compromise in performance, robustness, or reliability. These chips can operate alongside their traditional counterparts with no externally-visible difference - except for the amount of energy required to drive them. They can provide important energy savings to designers building energy-efficient systems.

Because of the fundamental nature of these innovations, sub-threshold design techniques can be applied to virtually any type of IC device.

Sub-threshold was proven decades ago

Sub-threshold design isn't a new concept. As far back as the 1970s,



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ⁱ See datasheet for suggested application circuit.

ⁱⁱ Flatness specified over 0.5 to 7GHz.

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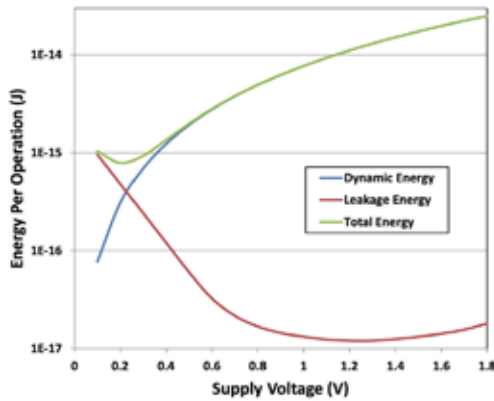


Figure 1 - Dynamic current dominates with higher operating voltage

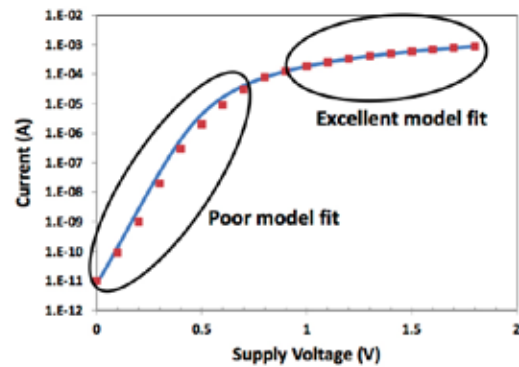


Figure 2 - Transistors haven't been well modeled below threshold

Swiss watchmakers noticed the potential of operating select transistors in the sub-threshold region. The idea was picked up for pacemakers and RFID tags, but never saw much acceptance beyond that.

What's changed since the 70s, when the first commercial sub-threshold devices were created, is the scale of implementation. Designs of the past used a few critical sub-threshold transistors - on the order of 10. At that level, each transistor can be optimized by hand.

Ambiq creates entire chips that primarily use sub-threshold transistors. This equates to millions of transistors and cannot be done by hand but relies on the standard design tools and flows used to create super-threshold chips. It is these that Ambiq has achieved in order to commercialize sub-threshold circuits.

Ambiq Micro's approach moves beyond the incremental improvements that other semiconductor companies have taken and makes revolutionary advances through a unique approach to the problem: sub-threshold circuit design. These considerations drove the development and commercialization of Ambiq's patented Sub-threshold Power Optimized Technology (SPOT™)

platform, which Ambiq uses to build reliable, robust circuits that consume dramatically less energy on a cost-effective, mainstream manufacturing process.

Electronics energy consumption

Because dynamic energy varies as the square of the operating voltage, that voltage becomes the biggest lever for reducing dynamic energy consumption (while also having a tangible, but less dramatic, impact on leakage). For example, when compared to a typical circuit operating at 1.8V, a "near-threshold" circuit operating at 0.5V can achieve up to a 13X improvement in dynamic energy. An even more aggressive "sub-threshold" circuit operating at 0.3V can achieve up to a 36X improvement!

Traditional digital designs use the transistor state - "on" or "off" - as a critical concept for implementing logic. Analog designs likewise assume that a transistor is "on" to some controlled degree, using it for amplification. But sub-threshold operation means that none of the voltages in the chip rise above the threshold voltage (V_{th}), so the transistors never turn on. Even a logic "high" voltage keeps

the transistors "off." This means that completely new design approaches are required.

The challenges of modern sub-threshold

Adapting the standard super-threshold flows and infrastructure for sub-threshold design presents numerous challenges, starting with the transistors themselves:

1. Poor transistor models

The transistor model forms the basis of everything in an integrated circuit design. All of the simulations, all of the abstractions and automation, the very process of design closure: they all rely on an accurate transistor model. Most transistor modeling has focused on the "on" characteristics of the device, with little attention given to "off." The entire region between 0 V and V_{th} typically does not get modeled as accurately, and so existing models are inadequate for sub-threshold design, as shown in Figure 2.

2. Logic swings and noise

The output response of a transistor in the sub-threshold regime is subtle; detecting it requires great sensitivity. Currents change exponentially in

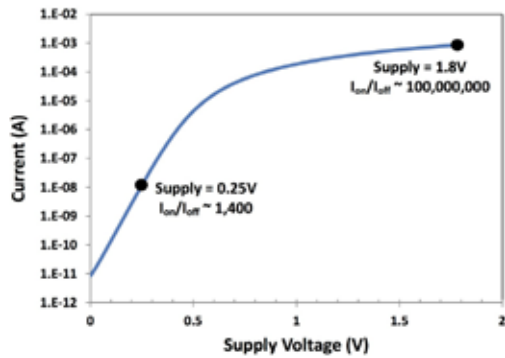


Figure 3 - The on/off current ratio is orders of magnitude smaller in the sub-threshold regime

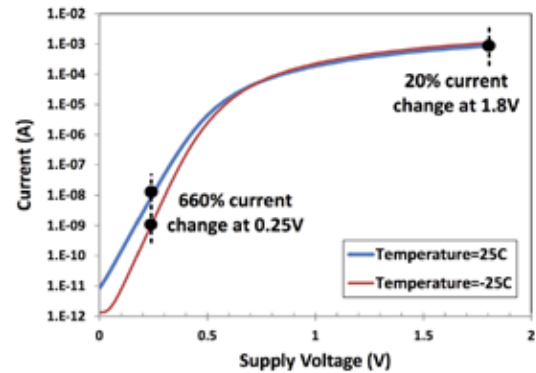


Figure 4 - Sub-threshold circuits are exponentially sensitive to temperature

response to changing voltages, but they're exceedingly small currents. In addition, the ratio of "on" to "off" current is on the order of 1000, orders of magnitude less than what super-threshold designs experience (see Figure 3). As can be expected, external noise can much more easily interfere with clean operation.

3. Sensitivity to operating conditions

Sub-threshold designs are also far more susceptible to process and environmental variation than are super-threshold designs. For example, the current in a slow process corner can be 10-100 times less than that for a nominal process. Given that the on/off current ratio (above) is only on the order of a thousand, this cannot be ignored.

Variations in temperature provide a good example of how environmental conditions create a challenge for the designer. V_{th} depends on temperature, and I_{on} depends exponentially on V_{th} (as shown in Figure 4 below). As a result, the "off" current at elevated temperature is similar in value to the "on" current at reduced temperature for an uncompensated circuit. Sub-threshold circuit design therefore

requires extra effort to ensure that the circuits will operate as expected under all specified operating conditions.

4. Logistical challenges

Much of the manufacturing flow is based upon assumptions that are reasonable for super-threshold designs but break down for sub-threshold designs. One obvious challenge can be found in the testers used to validate the silicon during production. The parametric measurement units (PMUs) that test voltages and currents are designed to measure microamps, not nano- or picoamps.

Even something as straightforward as device characterization has to be rethought simply because of the sensitivities that sub-threshold circuits have that super-threshold circuits don't have. Typical characterization flows may not be thorough enough to prove that the circuits operate properly under all conceivable conditions.

The fundamental nature of these challenges, combined with the fact that few engineers are skilled in dealing with sub-threshold issues, explains the challenge of commercializing sub-threshold-based circuits.

Possible solutions

Ambiq's SPOT technology addresses

and overcomes all of these challenges. Moreover, sub-threshold design techniques can be applied to virtually any type of IC device. For example, Ambiq demonstrated the viability of this innovative approach with the introduction of the world's lowest power real-time clock (RTC) in 2013. The upcoming release of the world's lowest power 32-bit ARM-based microcontroller (MCU) further demonstrates the viability of extending these techniques to a completely different platform. Ambiq Micro is committed to expanding the SPOT Platform - and to giving batteries a better life.



Mike Salas,
VP Marketing Ambiq Micro

Out Of the box

Meet Pepper - kindly, endearing and surprising.

Pepper is a humanoid robot, engaging, surprising and above all kind. Pepper is the first emotional robot. He was not designed for an industrial function, rather to be a true companion for daily life with a first focus on affection. Because of this, Pepper will truly change the way we live our lives.

Pepper is the first humanoid robot capable of recognising the principal human emotions and adapting his behaviour to the mood of his interlocutor.

To date, more than 140 SoftBank Mobile stores in Japan are using Pepper as a new way of welcoming, informing and amusing their customers. Pepper also recently became the first humanoid robot to be adopted in Japanese homes!

Emotional

Pepper is unique; a loyal friend, family member, and a kind accomplice. By the tone in your voice, the expression on your face, in your gestures and through the words you use, Pepper will progressively learn to detect your mood and adapt his behavior to relation to it.

Pepper's main objective is to communicate with you. He has a certain personality and expresses his own "emotions" through the color of his eyes, his gestures and words he uses.

Ultimate Interface

No need for a keyboard, mouse or screen, simply talk to Pepper, touch him or even approach him and watch him react.

Pepper communicates the same way you do, through voice and gestures. This is an example of how technology is using the simplest and most intuitive form of communication we know.



Interactive and Independent

Pepper is the first humanoid companion for the general public, able to interact in the real world and have a real presence among humans. His multiple sensors enable him to understand the world around him and adapt accordingly. Pepper can move, avoid obstacles, identify sounds, follow you and even recharge independently.

Scalable

Pepper is much more than the newest tech product, he is an artificial creature that was designed to learn, evolve and surprise you a little more each day. Pepper currently requires some assistance: he does not know everything! You teach Pepper through your discussions which, today, help him memorize names, faces, moods, tastes and habits. Tomorrow, the evolution of Pepper will also be fueled by an application library which

Out Of the box



either you or Pepper will be able to access to find new behaviors, activities and content to inform, entertain or surprise you.

The meeting of SoftBank/Aldebaran

The next revolution of robotics and innovation is engrained in the DNA of Softbank, a large Japanese group with over 1,300 subsidiaries and affiliates worldwide. Once the decision was made in 2011 to invest in personal robotics, SoftBank identified several companies worldwide that might assist them with this mission. Aldebaran proved to be the most advanced and experienced actor in this market, since 2005, and was the creator of a very specific concept: to create emotional, kind robots to improve the lives of people. Aldebaran and SoftBank then created a shared vision: to initiate a new era with a class of interactive humanoid robots capable, as did the Internet, computers and mobile phones, to enrich

success in the world of personal robotics.

Aldebaran

Founded by a French entrepreneur and lifelong robotics enthusiast, Aldebaran creates companion robots to help humans in everyday life. In less than 10 years, Aldebaran grew from a small start-up to the world leader in the humanoid robotics market, with robots being used in over 70 countries around the world. Today Aldebaran has about 450 employees with offices located in France, China, Japan and the United States. In 2005, a handful of robotic enthusiasts created the company Aldebaran, drawing the name of the brightest star in the Taurus constellation. A year later the first prototype of their humanoid robot was born and named NAO.

Thought to be an everyday companion, NAO was not yet finalized for this purpose but was already drawing attention by various academics and researchers. In 2008 NAO was selected to succeed the robot dog Aibo as the standard league platform for the RoboCup Soccer league. This university competition organizes soccer matches between robots with a specific goal in mind: to have robots play against the (human) World Cup champions by 2050!

Gradually NAO became a standard in the world of research and education. when 20 NAOs were invited to dance in the France Pavilion at the Shanghai World Expo. NAO was the main attraction with the pavilion being visited by more than 10 million people. Over time, new versions of the robot were created with improved features. Through these evolutions the scope of educational uses for NAO continue to widen to include secondary education. In 2011, ROMEO is born after two years of work in collaboration with research laboratories and institutions around Europe. This new robot, still only a research platform, aims to implement technologies in a larger sized robot to be able to physically help disabled people, at home or in nursing homes. The year 2013 was marked by the launch of the ASK NAO program which offers a new educational approach for teachers to assist children with autism and other special needs through the help of NAO and specifically developed applications.

STMicroelectronics Brings ARM® Cortex®-M7 Power to Even More Applications with New Graphics-Centric STM32 Microcontrollers

High-performance MCUs now available with up to 2MB Flash and 512KB RAM

STMicroelectronics' new STM32F767/769 microcontrollers (MCUs) with rich memory, graphics and communication peripherals bring ARM® Cortex®-M7 processing power and efficiency to a wider range of applications such as portable or wearable consumer devices, smart-building and industrial controllers, smart appliances, and personal or point-of-care medical equipment.

Particularly well suited to simplifying the design of high-performance controls and user interfaces, the latest members of the extensive STM32 MCU family feature a 216MHz/462DMIPS/1082 EEMBC® CoreMark® Cortex-M7 core with double-precision floating-point unit and DSP instructions. Integrated alongside the core are up to 2MB of dual-bank Flash, ST's Chrom-ART Accelerator™ for powerful graphics performance, a hardware JPEG accelerator, TFT-LCD controller, and MIPI®-DSI1 host controller.

The generous on-chip resources enable graphics applications to benefit from richness and rendering beyond the capabilities of other microcontrollers. There are also powerful audio features including an I2S interface, Serial Audio Interface (SAI), audio PLLs, and DFSDM (Digital Filter for Sigma-Delta Modulators) for connecting a digital microphone or external Sigma-Delta ADC.

The STM32F767/769 feature 512KB of integrated RAM, as well as large 16KB Data and Instruction caches, while the

Flexible Memory Controller (FMC) and Quad-SPI interface simplify off-chip memory expansion allowing practically unlimited application code size. In addition, the on-chip Flash allows read-while-write for seamless application performance and continuous operation even while simultaneously updating software.

The STM32F767/769 extend the performance potential of the STM32F7 series and provide the option of a crypto/hash engine (with STM32F777/779 devices) for security-conscious applications. As Cortex-M7 devices, they also provide an upgrade path from STM32F469/479 Cortex-M4 devices that have similar graphics and memory features. The associated ecosystem has features that help developers achieve high graphics performance for applications such as human-machine interfaces.

The STM32F767/769 microcontrollers are sampling now and will enter mass production in May 2016. Pricing for 10000-piece orders starts at \$10.95 for the STM32F779NIH6 (2MB Flash, 512KB RAM, TFT, MIPI-DSI, Crypto, TFBGA216) or \$7.96 for the entry-level STM32F767VGT6 (1MB Flash, 512KB RAM, TFT, LQFP100).



Toshiba Launches 15W Wireless Power Transmitter IC

Connected to a microcontroller, the new IC realizes a wireless power transmitter system compliant with Qi[1], the standard defined by the Wireless Power Consortium (WPC).

Toshiba's original cutting-edge CD-0.13 process realizes a small package and high efficiency, making system integration easy while securing a transmitter system with a small footprint. A 15W wireless transmitter formed with the new IC will recharge devices quickly, at a rate equal to or shorter than wired chargers. The IC is suitable for use in wide range of applications including mobile devices, such as smartphones and tablets, and industrial devices.

Wireless transmitters that use the new IC will be compatible with 5W receiver systems that use Toshiba's 5W receiver IC, "TC7764WBG," and 10W receiver systems that use the "TC7765WBG" 10W receiver IC, both of which are in mass production. In combination with a 15W wireless receiver control IC "TC7766WBG" compliant with the Qi v1.2 standard, the wireless system can receive up to 15W power.

Main features

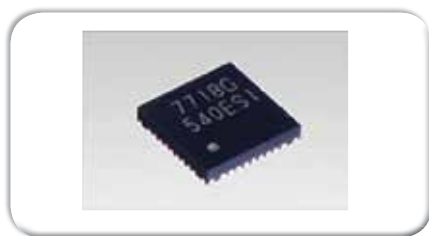
- WPC Qi v1.2 compliant (in combination with a microcontroller)
- Full-bridge gate driver (also compatible with half-bridge): 1ch
- Built in LPF[2] for recovery of ASK signal
- Built in LDO (3.3V output)

Application

Charging stand for mobile devices (smartphones, tablets) and industrial devices etc.

[1] Qi Standard: The international standard for wireless charging defined by Wireless Power Consortium

[2] LPF (Low Pass Filter): A filter that passes signals with a frequency lower than a certain cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency.



Samsung's New Mid-power LED Package Line-up, LM561B+, Offering Superior Performance and Higher Quality Light Color for Premium Luminaires

Samsung Electronics, a world leader in advanced components, announced that LM561B+, the company's new mid-power LED package line-up with high light efficacy, is now offered with 3-step MacAdam ellipse bins and quarter bins across the range of all CCTs (from 2700K to 6500K), for use in premium luminaires. By leveraging the chromaticity control standard with the LM561B+, manufacturers will be able to make lighting products that deliver greater uniformity and consistency in light color without any visible difference in the color output between packages.

"To date, we have achieved outstanding performance in all of our mid-power LED packages," said Jaewook Kwon, vice president, Lighting Marketing Group, LED Business Team, Samsung Electronics. "By now offering premium light quality to a greater number of customers with our LM561B+ LED package, we are able to provide superior performance on a much wider scale."

Since 2013, Samsung has been introducing high-performance mid-power LED packages such as the LM561 series for indoor lighting applications including LED Lamps, L-Tubes, ambient lighting and

downlights. Its latest LM561 LED packages—the LM561B+ and LM561C – provide 190lm/W and 200lm/W of light efficacy respectively, an industry-leading performance level. Later this year, Samsung will also extend its offering of 3-step MacAdam ellipse bins and quarter bins for the LM561C across all CCT levels.

In addition, for its high color rendering LM561B+ packages with over 90 CRI, Samsung plans to apply advanced phosphor control technology, which will lead to approximately 15 percent higher flux performance.

In supporting its LED lighting component customers more efficiently, Samsung is also strengthening its product certification program around the globe. Through cooperative relationships with recognized certification companies in the U.S., Korean, European and Chinese markets, Samsung is working to help minimize any difficulties that customers could encounter due to varying certification requirements for lighting quality, safety and power efficiency. The partnerships will simplify complex procedures, reduce time to market and ultimately have a positive impact on overall costs.



STMicroelectronics Launches USB Type-C™ and Power-Delivery Interfaces, Focused on Architectural Flexibility and Highly Integrated Protection

STMicroelectronics (NYSE: STM), a

global semiconductor leader serving customers across the spectrum of electronics applications, has announced a new solution for USB Type-C™ and Power Delivery with an interface IC aimed at clearing the "Rat's Nest" of cables in the office and living room currently used to charge and connect computers, smartphones, tablets, TVs, set-top boxes, gaming platforms, and a broad range of consumer, industrial, and IoT smart devices.

The USB Type-C connector and new standard Power Delivery modifies the USB ecosystem from a data interface capable of supplying limited power to a primary provider of power that includes a well-proven and widely adopted data interface. The connector offers reversible plug orientation and cable direction, delivering data rates up to 10Gbps and power up to 100W, making it ideal for consolidating numerous cables.

Manufactured using ST's 20V process technology, the STUSB16 interface IC integrates short-circuit, over-voltage, over-current protection, eliminating the need for external circuitry. Additionally, it offers plug power support (VCONN) with up to 600mA programmable current capability and, per the USB Power Delivery specification, it integrates Bi-Phase Mark Coded (BMC) Physical Layer (PHY) coding and decoding logic.

"Knowing well the frustration of being surrounded by numerous different cables with very limited interoperability, ST, as member of the USB-IF Board of Directors and an active player on the USB Implementers Forum, is working aggressively to build a strong and flexible portfolio of USB Type-C and power delivery solutions that include our STM32 microcontroller, ESD protection devices, and power-

management products,” said Andrea Onetti, Group Vice President and General Manager Volume MEMS Division, STMicroelectronics. “The new STUSB16 family embeds higher levels of circuit protection and a customer-configurable non-volatile memory, which enables IC configuration at power-up without software support. Overall, the ST portfolio delivers a low BOM cost and flexible hardware/software solution capable of meeting every power-profile requirement and customization need.”

ST has enabled the migration to the USB Type-C port through the simple addition of an STUSB16 companion chip to existing MCU-based designs, while minimizing MCU-resource requirements compared to alternate solutions. Together these features simplify software development and reduce time-to-market while allowing customers to focus on their own added-value differentiators.

The first member of the STUSB16 family, the STUSB1600QTR, is sampling to lead customers now at \$0.95 in 1ku.



■ Panasonic Develops Single Cable and Connector Solution for Transmission of Full-spec 8K Video Signals*1

Panasonic Corporation today announced that it has developed single cable and connector solution that enable the transmission of uncompressed full-spec 8K video

signals*1.

Currently, to transmit video signal via connector-equipped cables from an 8K signal source or other devices to an 8K display, 4K-equivalent images are transmitted using four HDMI cables, and then they are combined to show in 8K resolution by using image processing. Panasonic's newly-developed connector-equipped cable, which uses plastic optical fiber technology, can achieve the transmission of full-spec 8K video via a single cable, with improved bandwidth and length.

High-speed transmission over optical fiber connector can be achieved when the optical axes are completely aligned. However, when the equipment and the cable's connection portions are detachable, it is difficult to precisely align optical axes at the connection, leading to poor connectivity and other defects. That has hampered the deployment of optical fiber cables in video transmission cables with detachable connectors.

Working with KAI Photonics Co., Ltd., a venture from Japan's Keio University, Panasonic developed connector-equipped cables that adopt “plastic optical fiber and its connection technology using ballpoint-pen type interconnect*2.” Further, by applying Panasonic's technology for the multi-level modulation of broadband signals, a transmission bandwidth exceeding 100 Gbps was achieved with a single cable.

Professor Yasuhiro Koike of the Faculty of Science and Technology, Keio University, commented: “I am delighted that Panasonic successfully developed a prototype cable for transmitting 8K images based on ‘plastic optical fiber and its connection technology using ballpoint-pen type interconnect,’ which was developed

by Keio University. We would like to further cooperate with Panasonic to respond to the variety of needs for audiovisual transmission.”

Anticipating the spread of the corporate use of 8K devices in the B2B market, Panasonic aims to make this innovative connector cable technology an international standard. Technologies related to this proto model will be exhibited at the Panasonic booth at CES 2016 to be held in January in Las Vegas, U.S.A.

Notes:

*1 The term denotes an image of approx. 33 million pixels (7,680 × 4,320) and 120 frames/sec. A full HD image is composed of approx. 2 million pixels (1,920 × 1,080) and 60 frames/sec. and a 4K image approx. 8 million pixels (3,840 × 2,160) and 60 frames/sec.

*2 The ballpoint-pen type interconnect technology for plastic optical fiber connection has been developed jointly by Mitsubishi Pencil Co, Ltd. and Keio University's Professor Yasuhiro Koike.



■ New FCI USB 3.1 Type C connectors are reversible for quick and easy USB, power, audio and video connection: now available through TTI

Small form factor; supports SuperSpeed 10Gb/s for emerging designs

Now available in Europe through TTI, Inc., a world leading specialist distributor of electronic components,

FCI's new USB 3.1 Type C Connectors boast a small form factor design that is reversible for quick and easy connection whichever way it is inserted. The USB 3.1 Type C Connector is a new standard plug and receptacle which provides a multi-function single cable solution for USB, power, audio and video and is specifically designed by FCI to suit a wide range of emerging and future product applications.

The FCI USB 3.1 Type C connector provides outstanding performance that minimizes user waiting time – it supports SuperSpeed 10Gb/s speeds in each direction and power delivery up to 100W. It is extremely robust for applications such as laptop computers, tablets, and portable game stations. Its small form factor also suits very thin platforms like mobile phones and emerging devices such as smart watches and wearables. In addition to these consumer applications, FCI's USB 3.1 Type C connector is also targeted at the industrial and instrumentation markets.

Manufactured with a high-temperature thermoplastic housing, stainless steel shell and with copper alloy terminals, the devices have low-level contact resistance and deliver up to 5A maximum current, with configurable voltage of up to 20V. Operating temperature

is -55degC to +105degC. RoHS compliant, lead-free and halogen-free, the new USB 3.1 Type C meets environmental, health and safety requirements. Plugs and receptacles are available with vertical or right angle orientation and are supplied packaged on tape and reel for automated assembly.



LATTICE SEMICONDUCTOR LAUNCHES ICE40 ULTRA™ PLATFORM FOR WEARABLE DEVICE DEVELOPMENT

Feature Rich, Low-Power Platform in Compact Wrist Watch Form Factor Supports Multiple Wearable Applications

iCE40 Ultra FPGA featured in platform is 60 percent smaller than alternative microcontrollers
Broad range of hardware features make platform a fit for almost any consumer wearable device
Platform comes with user guide and demos to help expedite device

design

PORTLAND, OR – December 1, 2015 – Lattice Semiconductor Corporation (NASDAQ: LSCC), the leading provider of customizable smart connectivity solutions, today announced a development platform for use in designing low-power wearable devices for consumers. Based on the iCE40 Ultra™ FPGA, the platform features a large number of sensors and peripherals, making it a compelling platform for the design of a wide array of wearable devices.

The iCE40 Ultra FPGA uses a package that is 60 percent smaller than alternative microcontrollers. The iCE40 Ultra FPGA also supports a low power standby mode for always-on functionality, making it an ideal choice for consumer wearables that need to operate for days between charges.

Hardware features and sensors supported by the iCE40 Ultra Wearable Development Platform include a 1.54-inch display, MEMS microphone, high-brightness LED, IR LED, BLE module and 32MB of flash memory. The platform also supports sensors capable of

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measuring heart rate/SpO2, skin temperature, and pressure as well as an accelerometer and gyroscope. The platform comes in a wrist watch form factor (1.5-inches wide x 1.57-inches long x 0.87-inches high) with a wrist strap and a built in battery.

“One of the more popular applications to emerge from the growing Internet of Things market are wearable devices. However, with so many potential applications for wearables and their strict power requirements, it’s a challenge to find a semiconductor platform that features the right combination of low power operation and peripheral support,” said Ying Chen, product marketing manager at Lattice Semiconductor. “Our iCE40 Ultra Wearable Development Platform’s power usage and feature set make it an ideal choice for nearly any wearable application our customers can dream of.”

Included with the platform are a detailed user guide and several demos to showcase parallel RGB to MIPI DSI bridging, health monitor, pedometer, IR transmitter or flashlight functions.

The iCE40 Ultra Wearable Development Platform is available now direct from Lattice at a retail price of \$270. Please visit www.latticesemi.com/ultrawearable to learn more about the platform and for ordering information.



Freescale Kinetis MCU development solution provides comprehensive support for new ARM® mbed™ IoT Device Platform

Popular Freescale Freedom FRDM-K64F board supports ARM mbed software, tools and cloud services for rapid creation of IoT products spanning from end-node to cloud SANTA CLARA, Calif.–(BUSINESS WIRE)– (ARM TechCon 2015) — Designed in collaboration with ARM® mbed™, Freescale Semiconductor’s (NYSE: FSL) popular FRDM-K64F board is available now with comprehensive support for ARM mbed IoT Device Platform technologies, including ARM’s new mbed OS operating system.

Recognized earlier this year as one of the industry’s first development boards to fully support mbed, Freescale’s FRDM-K64F board enables end-to-end mbed solutions and works with a full complement of mbed technologies including the mbed OS, mbed Client, the mbed Device Connector service and associated mbed tools.

Freescale’s support for the new mbed OS reinforces Freescale’s proven track record of collaboration with ARM on mbed enablement, which includes the FRDM-K64F board serving as the processing platform for two of the first “IoT end device-to-cloud” solutions for mbed – the ARM mbed IoT Starter Kit for IBM® IoT Foundation and ARM’s mbed solution for Microsoft Azure IoT Suite. Freescale also recently delivered its advanced FNET TCP/IP software stack to the mbed ecosystem. This software will become the foundation of the mbed TCP/IP stack and serve as the connectivity heart of the ARM mbed OS architecture.

“ARM mbed IoT Device Platform fills a critical gap by providing a comprehensive, standards-based

platform for microcontrollers,” said Geoff Lees, senior vice president and general manager of Freescale’s MCU Group. “mbed helps our customers speed time-to-market with off-the-shelf technologies that support key IoT requirements such as connectivity and robust security.”

“Freescale’s FRDM-K64F has been a valuable test platform during the internal development prototyping and validating of mbed OS with the other mbed IoT Device Platform capabilities,” said Zach Shelby, vice president of marketing, IoT business, ARM. “The feedback we have received from mbed developers implementing designs with Freescale’s FRDM platform has been strong. We expect to see more next generation designs based on the FRDM-K64F given its applicability to a variety of IoT applications.”

Easily add wireless functionality to the Freescale Freedom FRDM-K64F board

The Freescale Freedom FRDM-CR20A development board for the MCR20A 2.4 GHz wireless transceiver connects with the mbed Enabled™ Freescale FRDM-K64F, forming an mbed supported solution. The FRDM-CR20A board provides a low-power 802.15.4 radio, and when combined with the FRDM-K64F board, creates the basis for a fully functional, wireless, cloud-connected IoT platform, further enabling new technologies including Thread low-power mesh wireless networks.

“Zebra Technologies has selected the Freescale FRDM-K64F as one of the first IoT reference examples to work with Zatar, our mbed Enabled cloud service for IoT, due to its widespread support in the ARM mbed ecosystem,” said Thomas Kurian, senior director of New Growth Platforms at Zebra. “We look forward to collaborating with Freescale to help customers take advantage of chip-to-cloud reference designs for IoT.”



Level VI Compliant Ac-Dc Power Supplies Feature Interchangeable Input Blades for Global Use

CUI Inc today announced a family of Level VI compliant external ac-dc power supplies ranging from 5 W to 36 W that feature interchangeable ac input blades. Designed for global use, the wall plug-in SMI5-USB, SMI6, SMI18, SMI24 and SMI36 include ac blade options for North America, Europe, the United Kingdom, Australia and China. The series are all designed to meet the stringent Level VI standards which aim to significantly lower the amount of power consumed when the end application is not in use or is no longer connected to the system. Any domestic or global manufacturer seeking to market their end-product with an external adapter in the United States must meet these new performance standards mandated by the US Department of Energy (DOE) by February 10th, 2016.

The 5 W, 6 W, 18 W, 24 W and 36 W multi-blade adapters feature a wide universal input voltage range of 90~264 Vac and are available in single output voltages from 5~48 Vdc depending on the series. All models meet the Level VI standard's no load power consumption requirement of < 0.1 W. Protections for over voltage, over current and short circuit are also included and

vary by series.

The SMI5-USB comes with an integrated USB connector and offers UL/cUL, GS and RCM safety approvals, while the SMI6 series also includes CCC and PSE safety approvals. The SMI18 and SMI24 series both offer UL/cUL, GS and PSE safety approvals, while the SMI36 series also holds the CCC safety approval. All models meet FCC Part 15 Class B standards for EMI/EMC and bear the CE mark. The new SMI5-USB, SMI6, SMI18, SMI24 and SMI36 series are available immediately through distribution with prices starting at \$7.93 per unit at 100 pieces. Please contact CUI for OEM pricing. (<http://www.cui.com/contact>)

For more information on the US Department of Energy's upcoming Level VI regulations, click here. (<http://www.cui.com/efficiencystandards>)

Summary

Product name: SMI5-USB, SMI6, SMI18, SMI24, SMI36
Availability: Stock to 12 weeks

Possible users: Consumer, industrial and mobile device designers

Primary features: Level VI efficiency, interchangeable ac input blades

Cost: \$7.93 per unit at 100 pieces through distribution



1 W DC/DC converter with 6.4kVDC isolation

RECOM introduces its latest converter series RK/H6 and RH/H6, a reliable choice for a wide range of low-power

applications in industrial electronics, measuring technology and sensor systems where high isolation voltage is particularly important.

Both converter series are rated for 1 W and offer up to 6.4kVDC isolation between the input and output for 1 second. In contrast to the RK/H6 series, the RH/H6 series comes with dual outputs. Both models are available for input voltages of 5VDC, 12VDC, 15VDC and 24 VDC and supply 3.3VDC, 5VDC, 12VDC and 15VDC (RK series) or ± 3.3 VDC, ± 5 VDC, ± 12 VDC and ± 15 VDC (RH series) at the outputs. They have an efficiency of up to 80%, are permanently short-circuit proof and can be operated without a minimum load.

Both converter series come in the compact SIP7 housing (19.6 x 7 x 10.2 mm) and can be operated at full load over a temperature range of -40 °C to + 90 °C. They are IEC / UL60950-1 certified and come with a 3-year manufacturer warranty.



300mV Start-Up, 1.6µA IQ Synchronous Buck-Boost DC/DC Converter with Integrated PowerPath for Low Power Wireless Sensor Applications

Linear Technology announces the LTC3106, a highly integrated, 1.6µA quiescent current 300mV start-up buck-boost DC/DC converter with PowerPath™ management, optimized for multisource, low power systems. The LTC3106

is ideal for powering low power wireless sensors from rechargeable or primary batteries supplemented by energy harvesting. The LTC3106 incorporates maximum power point control (MPPC) making it compatible with common high impedance power sources, including photovoltaic cells, thermoelectric generators (TEGs) and fuel cells.

The LTC3106 operates over an input voltage range of 300mV to 5.5V from the primary power source when a backup source, typically a battery, is present. The LTC3106 is compatible with both primary and rechargeable batteries connected to the backup power input. Without a backup source, it operates from 850mV to 5.5V and down to 300mV after start-up. If the primary power source is unavailable, the LTC3106 seamlessly switches to the backup power source. The primary power source, which can be derived from harvested energy, can optionally trickle charge the battery whenever surplus energy is available as well as providing power to the load.

The LTC3106 provides 300mA steady state and 650mA peak load current at up to 92% efficiency. Its Burst Mode® operation offers a quiescent current of only 1.6µA, further optimizing converter efficiency over all operating conditions. Zero power “shelf mode” ensures that the backup battery will remain charged if left connected to the LTC3106 for an extended time. An accurate RUN pin and a dedicated MPP pin are provided for input voltage control. Either can be user programmed to set the input source MPP, maximizing the energy that can be extracted from the input source. The LTC3106 is ideal for powering wireless sensors

and data acquisition applications. Surplus or ambient energy can be harvested and then used to supplement or replace traditional wired or battery power, resulting in significant periodic maintenance cost savings for the user. Typically, such applications, including wireless sensors, require very low average power, but require periodic pulses of higher load current. For example for transmission bursts.

Additional features include a 90mA peak current limit setting for lower power applications, user-selectable overvoltage and undervoltage protection for a rechargeable battery, thermal shutdown, preset selectable output voltages and a power good output voltage signal. The combination of the LTC3106's small package options and minimal external components ensures a very compact solution footprint.

The LTC3106 is available in 20-lead 3mm x 4mm QFN and TSSOP-20 packages. Prices start at \$2.94 each in 1,000-piece quantities. Both are available from stock. For more information, visit www.linear.com/product/LTC3106.

Summary of Features: LTC3106

- Dual Input Low Voltage Buck-Boost DC/DC Converter
- Integrated PowerPath Manager
- Maximum Power Point Control for
- High Impedance Sources
- VIN Range (With Backup Source): 300mV to 5.5V
- VIN Range (Without Backup Source): 850mV to 5.5V, Maintains Operation Down to 300mV After Start-Up
- Compatible with Primary or Rechargeable Backup Batteries
- Digitally Selectable Output Voltages
- Burst Mode® Operation: $I_Q =$

1.6µA

- Battery Backup Trickle Charger
- Shelf Mode Disconnect Function to Preserve Battery Shelf Life
- Accurate Turn-On Threshold
- Power Good Indicator
- Selectable Peak Current Limit 90mA/650mA
- 20-Lead 3mmx4mm QFN or TSSOP-20 Package.



Würth Elektronik eiSos expands its series of terminal block push-on connectors

Würth Elektronik eiSos expands its series of terminal block push-on connectors: new products and additional contact-space pitches Waldenburg, Germany, 16 September 2015

Würth Elektronik eiSos is expanding its range of terminal block push-on connectors in the WR-TBL series, based on the wire-protection principle, with a number of new products. A total of eight new series now complement the already available product portfolio – both in the classic 5.00 mm pitch as well as in the form of new push-on connectors in the contact-space pitches 7.5 and 10 mm. The terminal blocks are all UL/cULus- and VDE-listed. They feature a current-carrying capacity of up to 24 A/750 VAC and are suited for applications involving operating temperatures between -30 and +120 °C.

The terminal blocks, some of which

can be modularly connected in series, support a broad spectrum of cable cross-sections from AWG30 (0.05 mm²) up to a maximum of AWG12 (3.31 mm²).

All products are directly available from stock; free-of-charge samples of the new WR-TBL products can be sent out on request.

For further information please visit www.we-online.de



ERNI Electronics Introduces Optimized High-Speed Connectors

Introducing the new ERmet ZDpro connector family, ERNI Electronic paves the way to 100G ATCA systems. The ERmet ZDpro connectors are an enhancement of the ERmet ZD family. This high-speed differential Hard Metric connector system enables data rates of >25 Gbit/s and is the first connector system that meets the requirements for 100G ATCA technology. The high data rates and the improved transmission behavior are mainly based on the reduced size of the signal termination, designed for vias with a diameter of only 0.30mm. The drilling hole diameter for the shielding contacts is specified with 0.46mm. The fact that the reduction of the vias leads to an improved crosstalk behavior was the motivation to the further miniaturization of the press-fit zone. The communication technology

shows an ongoing trend to increasing data rates and higher bandwidths. This means there is a strong need for 100 Gigabit Ethernet (GbE) data transmission. Typical applications are the next generation of internet backbones, data centers or cloud computing. The new ERmet ZDpro connectors fulfill the requirements and challenges of the important interface between backplane and daughter cards in these high speed systems.

The ERmet ZDpro is based on the mechanical design of the proven ERmet ZD and ERmet ZDplus with the same dimensions. ERmet ZDpro connectors are backwards mating compatible to ERmet ZD and ZDplus connectors. This means, that existing backplane designs do not need layout changes on the backplane side, if customers want to upgrade their daughter cards in the first step before upgrading the whole system. Of course the layout on the daughter cards has to be modified, if ERmet ZDpro receptacles are used.

To benefit from the maximum performance of the new ERmet ZDpro the usage of backdrilling is recommended. Decreasing via stub length and the related "stub effect" by backdrilling significantly reduces the reflections and the overall BER (Bit Error Rate) of the connection.

Availability

The first products of the ERmet ZDpro family are the 4-pair right angle female connector and the related straight male connector with press-fit termination. Both will be available starting September 2015. The connectors provide 40 signal pairs. The male connectors are available with different contact lengths (3.8mm or 5.3mm). While

the standard variants with 3.8mm contacts offer an optimized impedance behavior the male connectors with 5.3mm contact lengths provide a 1.5mm higher wipe length of 2.9mm.



TE Connectivity's UIC series connectors, now available at TTI, provide robust reliability for railway and mass transit applications

Toshiba Corporation's (TOKYO: 6502) Semiconductor & Storage Products Company today announced the launch of a new generation of highly efficient transistor arrays, the TBD62064A series and TBD62308A series, with a DMOS FET[1] type sink-output[2] driver. The new series succeed the TD62064A series and TD62308A series of bipolar transistor arrays that found wide use in applications including motors, relays and LED drives, and are the industry's first[3] DMOS FET transistor arrays with a 1.5A sink-output driver.

TBD62064APG

Mass production of TBD62064A series products is scheduled to start in February 2016. Sample shipments of TBD62308A series products start today, with mass production slated for March 2016. The new products are equipped with 4 channels of 50V/1.5A rated output, suitable for driving constant voltage unipolar stepping motors. Toshiba adopted DMOS FET output

drivers for its new products to secure the high efficiency customer requires to reduce power loss-D MOS FET do not require a base current, and can accept high current density per device area, keeping on-resistance low.

Main Features of New Products

High efficiency drive

TBD62xxxA series transistor arrays cut power loss by about 38%[4] compared with the TD62xxxA series.

High-voltage, large-current drive

The absolute maximum output rating is 50V/1.5A.

Packages to suit various needs.

The line-ups include a DIP type, strongly demanded by the equipment market for hobbies, amusements and industrial fields, and an HSOP type with a heat sink that realizes both high current(1.5A) drive and surface mounting.



Mini-Circuits' Ultra-Wideband Instrument Amplifier Supports Applications from 0.8 to 21GHz

Mini-Circuits' TVA-82-213A+ benchtop instrument amplifier provides extremely wideband performance with 25dB gain and ± 3.0 dB gain flatness across the entire 0.8 to 21GHz frequency range, ideal for wideband test

instrumentation and lab use. This model achieves +24 dBm output power at 1dB compression, +30dBm OIP3, 3dB noise figure, 70dB reverse isolation, and good input/output matching across its entire operating frequency range (1.35 input VSWR, 1.4 output VSWR). The amplifier is unconditionally stable and is capable of withstanding open and short loads while delivering output power up to P1dB. It features a built in 110/220VAC power supply, making it easy to use in most lab environments, and it comes in a compact, light-weight aluminum alloy case (15.35x8.27x3.25") with SMA connectors, perfect for bench-top use.

www.minicircuits.com



Antenova announces two flexible antennas: Bentoni and Asper for positioning applications with GNSS and 2.4-2.5GHz

Antenova Ltd, manufacturer of antennas and RF antenna modules for M2M and the Internet of Things, is adding two new positioning antennas, Bentoni and Asper, to its range of flexible FPC antennas.

Bentoni is a positioning antenna for all of the global public satellite constellations: GPS, GLONASS, Beidou and GALILEO. It is designed to be used in trackers, portable

devices, network components, drones and wearable electronics.

Asper is a dual antenna with two separate antenna systems in a single form factor. It combines a 1559 – 1609 MHz antenna with a 2.4 – 2.5 GHz antenna in the same part for positioning applications with wireless connectivity as well. This antenna is suitable for sports cameras, trackers, dash cams, portable devices, network devices and wearable electronics.

Both antennas offer high performance and maintain good isolation in situ within a device.

Bentoni and Asper are the latest flexible FPC antennas in Antenova's flexiiANT product range. They are supplied with an I-PEX MHF connector and a 1.13 mm RF cable in a choice of three lengths. They can be folded to save space in operation within a device.

Antenova's antenna design team aims to create antennas that a product designer can integrate with the other circuits in a design in a convenient way, rather than designing a product to fit around the antenna. The aim of these antenna designs is plug and play simplicity – they are self-adhesive mounted so that they can easily be fixed inside an electronic device.

Bentoni antenna and Asper antennas are available to order now.



Fairview Microwave Releases New Coaxial High Power RF, Microwave and Millimeter Wave Limiters

RF Limiters with High CW Power Handling Up to 200 Watts Peak Power New from Fairview Microwave

Allen, TX – Fairview Microwave Inc., a supplier of on-demand microwave and RF components, introduces a new family of broadband, high power limiters that aid in protecting sensitive RF receivers and components such as LNAs that are in close proximity to high power signals.

The new high power limiters from Fairview Microwave operate over broad frequencies ranging from 0.5 GHz to 40 GHz depending on the model. This release contains seven limiter designs featuring limiting thresholds between 3 to 10 dBm and low leakage power of 10 to 15 dBm. Fairview's new selection of coaxial limiters exhibits high CW power handling up to 200 Watts peak power and fast recovery times of 10 to 100 nanoseconds

Fairview Microwave's new high power, broadband limiters are constructed with high-rel, ruggedized packages that are designed to meet MIL-STD-202 environmental conditions for humidity, shock, vibration, altitude and temperature cycle. These components are also guaranteed to operate over temperature ranges from -54° C to +85° C. The 50 Ohm hybrid designs utilize limiting diode circuitry and do not require any external matching components.

“Our new portfolio of high power RF limiters provides designers and engineers the components needed to protect their sensitive RF receiver components from high power signals that could result in irreparable damage to the system,” says Brian McCutcheon, Vice President and General Manager at Fairview Microwave. “These high power limiters offer industry-leading performance and are well suited for applications such as electronic warfare, instrumentation, fiber optic communication systems, radar, SATCOM, point-to-point radio, telecom and R&D.

Fairview's new selection of high power coaxial limiters are now in-stock and available to ship today. You can view this line of new products by visiting <http://www.fairviewmicrowave.com/rf-products/broadband-high-power-coaxial-limiters.html> directly. Fairview Microwave can be contacted at +1-972-649-6678.



IZT RF Receiver R4000 Combines 120 MHz Bandwidth with 32768-Point FFT

Precise detection of frequency-agile signals and bursts

Erlangen, December 02, 2015 – The IZT GmbH launched a new option for its powerful R4000 RF receiver. The 32768-point FFT

option in combination with the 120 MHz real-time bandwidth ensures reliable detection of fast bursts and frequency-agile signals. Even the most advanced hoppers with extremely high hop rates are detected under demanding SNR environments. The Hopper Detector plugin provides real-time information about detected hoppers containing bandwidth, dwell time and time-of-arrival information.

Using the 32768-point FFT, the real-time frequency resolution is less than 5 kHz over the full 120 MHz bandwidth. The transformation is processed in a high-performance FPGA. The continuous detection without any gaps makes the R4000 a very powerful real-time signal analyzer.

In parallel to the PSD (Power Spectral Density), IQ content of sub-bands or even the full bandwidth can be retrieved and forwarded to the sensor controller. This allows to detect and analyze thousands of signals in parallel.

Utilizing the 4096-point FFT option, the time resolution of the spectrum can be as fast as 25.6 µs per spectrum. This is orders of magnitude faster than swept analysis techniques and meets the demand for systems being able to capture today's hopping, transient signals.



New Cadence Modus Test Solution Delivers Up to 3X Reduction in SoC Test Time

Physically aware 2D Elastic Compression architecture reduces test logic wirelength by up to 2.6X and enables compression ratios to scale beyond 400X without impacting design size

Cadence Design Systems, Inc. (NASDAQ:CDNS) today announced the new Modus™ Test Solution that enables design engineers to achieve an up to 3X reduction in test time, thereby reducing production test cost and increasing silicon profit margins. This next-generation test solution incorporates patent-pending, physically aware 2D Elastic Compression architecture that enables compression ratios beyond 400X without impacting design size or routing.

To address the challenges that come with testing designs, the Cadence® Modus Test Solution includes the following innovative capabilities:

2D compression: Scan compression logic forms a physically aware two-dimensional grid across the chip floorplan, enabling higher compression ratios with reduced wirelength. At 100X compression ratios, wirelength for 2D compression can be up to 2.6X smaller than current industry scan compression architectures.

Elastic compression: Registers embedded in the decompression logic enable fault coverage to be maintained at compression ratios beyond 400X by controlling care bits sequentially across multiple scan cycles during automatic test pattern generation (ATPG).

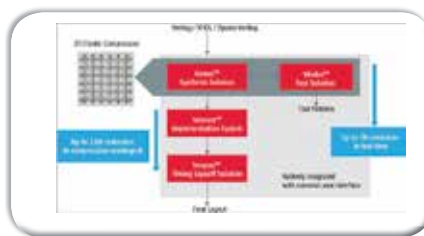
Embedded memory bus support: A shared test access bus can

be inserted to perform at-speed programmable memory built-in self test (PMBIST) across multiple embedded memories in an IP core. New soft programmable test algorithms for FinFET SRAMs and automotive safety applications are also included with this feature.

Powerful common scripting and debug environment: Design for test (DFT) logic insertion and ATPG capabilities use a new, unified Tcl scripting and debug environment that is shared with the Cadence Genus™ Synthesis Solution, the Innovus™ Implementation System and the Tempus™ Timing Signoff Solution.

“Our next-generation Modus Test Solution delivers new, innovative patent-pending technology that fundamentally changes the way design and test engineers address the test problem,” said Dr. Anirudh Devgan, senior vice president and general manager of the Digital and Signoff Group at Cadence. “By using a physically aware approach in a 2D grid, and compressing patterns sequentially as well, the Modus Test Solution can significantly reduce digital test time in comparison to traditional approaches, thereby giving Cadence customers yet another significant profitability advantage.”

For more information on the Modus Test Solution, please visit www.cadence.com/news/modus.



Samsung Launches New LED Module Lineup, inFlux, for High-Flux Industrial Lighting

Samsung Electronics, a world leader in advanced components, introduced inFlux, a new lineup of high-flux (extremely bright), linear LED modules optimized for industrial lighting applications such as plants, parking lots and warehouses. The LED modules serve as a replacement for conventional T8 and T5HO (high output) tubes and are suitable for high-flux LED luminaires covering up to 40,000lm (luminous flux*).

“By providing a wide variety of installation layout options and brightness intensities, our new inFlux linear module will deliver greater design flexibility and convenience for lighting designers, as well as high performance and reliability for fixture manufacturers,” said Jaewook Kwon, Vice President, Lighting Marketing Group, LED Business Team, Samsung Electronics. “We will continue to reinforce our well-differentiated LED lighting engine lineups to be able to meet more diverse market needs.”

The Samsung inFlux LED module incorporates the company’s mid-power LED package (LM301A), which features advanced “flip chip” technology that enables a shorter junction-to-base distance and less thermal barrier layers in each package, while avoiding the need for metal wire bonding. This leads to lowering the thermal resistance of the packages, and permits each package to handle a wide range of current with improved light efficacy.

Fully embracing the flip chip LED approach, the new inFlux modules can provide better light performance, wider current alternatives and much lower heat resistance than modules using a conventional epi-up chip package.

High-efficacy mid-power packages bring additional benefits to customers, compared to using high-power packages. Mid-power packages can be placed more densely than high-power packages, which results in minimizing light deviation and increasing light uniformity of the inFlux module lineup. By utilizing a mid-power package, the inFlux lineup also brings cost benefits to manufacturers.

Samsung inFlux modules are available in six product types. Each type comes in a different flux range between 1,310lm and 9380lm with a length option, either 280 millimeters (mm) or 560mm, and offers several CCT color variations, including 3000, 3500, 4000 and 5000K. These product alternatives will offer lighting fixture makers more design flexibility in addressing a wide variety of application requirements. Through a combination of different module types, LED fixture manufacturers can vary their lamp flux from 6,000lm to 40,000lm.

The Samsung inFlux modules have been UL/cUL certified (U.S.), as well as CE and ENEC certified (Europe), and carry a 10-year warranty.

Samsung also makes it easier for fixture makers to take their lighting products through industry certification processes, thanks to cooperative relationships that Samsung LED has established with

recognized certification companies in the U.S., Korean, European and Chinese markets. These “partnerships” will simplify complex procedures, reduce time to market and ultimately have a positive impact on overall costs.



New Power Monitoring IC From Microchip Provides Highly Accurate Real-Time Power Monitoring of Multiple Loads

Highly Integrated Advanced Features Facilitate System Design and Reduce System Cost of Industrial, Commercial and Consumer Power-Hungry Applications.

Microchip Technology Inc. (NASDAQ: MCHP), a leading provider of microcontroller, mixed-signal, analog and Flash-IP solutions, announced today an expansion to its power-monitoring IC portfolio with the addition of the MCP39F511N. Capable of providing popular standard power calculations and event monitoring of two electrical loads, this highly integrated and accurate device facilitates system design and reduces system cost of power-monitoring wall outlets and smart plugs, power strips, AC/DC power supplies and power distribution

applications. It includes three analog to digital convertors (ADCs) for voltage and two current load measurements, a 16-bit calculation engine, EEPROM and a flexible 2-wire interface.

To learn more about the MCP39F511N, visit <http://www.microchip.com/MCP39511N-020116b>. View a short video on Microchip's metering products, here: <http://www.microchip.com/Metering-020116a>.

An integrated low-drift voltage reference in addition to the 94.5 dB of SINAD performance on each current measurement channel allows the MCP39F511N to monitor two current loads with just 0.5 % error across a wide 4000:1 dynamic range. The ability to measure active, reactive and apparent power, active and reactive energy accumulation, RMS current and RMS voltage, line frequency, and power factor combined with advanced, integrated features allows system designers of high-performance devices to reduce bill of materials and reduce time-to-market. 160120-MSLD-DIAG-MCP39F511N-7x5

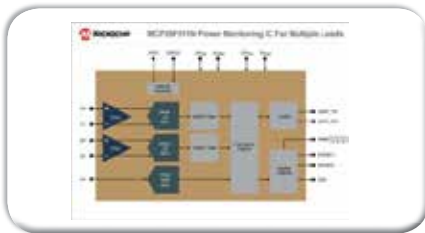
Development Support

The MCP39F511N is supported by Microchip's MCP39F511N Power Monitor Demonstration Board (Part # ADM00706), which is available now for \$200 via any Microchip sales representative or authorized worldwide distributor, or from microchipDIRECT(<http://www.microchip.com/mDirect-020116a>).

Pricing & Availability

The MCP39F511N is available now for sampling and volume production in a 28-lead, 5x5 mm

QFN package. It is priced at \$1.82 each, in 5,000-unit quantities. For additional information, contact any Microchip sales representative or authorized worldwide distributor, or visit Microchip's Web site at <http://www.microchip.com/MCP39F511-042115a>. To purchase products mentioned in this press release, go to microchipDIRECT or contact one of Microchip's authorized distribution partners.



TI drives high-voltage batteries with industry's first 100-V high-side FET driver

Unprecedented flexibility and power protection for advanced industrial battery applications

Texas Instruments (TI) (NASDAQ: TXN) today introduced the first single-chip 100-V high-side FET driver for high-power lithium-ion battery applications, delivering advanced power protection and control. The bq76200 high-voltage solution efficiently drives high-side N-channel charge and discharge FETs in batteries commonly used in energy storage systems and motor-driven applications, including drones, power tools, e-bikes and more. For more details, see www.ti.com/bq76200-pr.

Compared to typical 50-V low-side FET driver solutions, the 100-V high-side FET driver provides greater protection against possible inductive transient events in motor-driven applications, which can cause battery voltages to jump as much as 200

percent above normal. The bq76200 also helps maintain constant battery monitoring and enhanced system diagnostics – even when charging and discharging is disabled.

Key features and benefits of the bq76200: chip-01

Versatile supply voltage range: Compatible with a variety of battery architectures, capacities and voltage ranges from 8-V to 75-V, with an absolute maximum of 100-V.

Advanced-protection FET control: The fast-switching feature minimizes fault response time and disables the discharge FET if a battery has been severely discharged.

Quick development time and reduced overhead: The adaptable driver works with small to large power FET arrays by simply scaling the charge-pump capacitor, reducing engineering overhead and speeding development time.

High integration and small package size: The bq76200 integrates a high-voltage charge pump and dual FET drivers into one 5-mm by 4.4-mm by 1-mm thin shrink small outline package (TSSOP).

The bq76200 can be used in conjunction with the bq76940 battery-monitoring family, allowing for the application to move to a high-side FET drive and ensure that communication is always possible. The bq76200 can also drive TI's CSD19531Q5A 100-V NexFET™ power MOSFET as showcased in the bq76200 evaluation module.

Pricing and availability

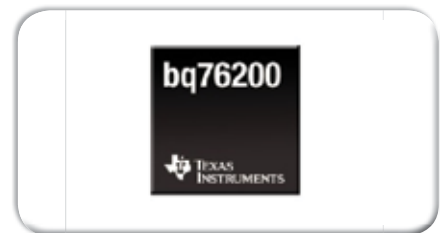
The bq76200 is available now in the TI store and through the company's authorized distribution network. The driver is packaged in a 16-pin TSSOP and is priced at US\$1.69 in 1,000-unit quantities.

Find out more about TI's battery-

management solutions:

Read the blog post, "Why high-side vs. low-side FET switching matters." Watch the videos, "TI's bq76200 100V Battery High-Side FET Driver" and "Introduction to the bq76200 EVM."

Visit the TI E2E™ Community Battery Management forum to search for solutions, get help, share knowledge, and solve problems with fellow engineers and TI exp



Cypress Unveils the World's Most Flexible One-Chip ARM Cortex-M0 Solution

New PSoC® 4 L-Series Reduces Costs and Gets Embedded Designs to Market Faster with the Ability to Develop Premium User Interfaces and Product Variations Rapidly

Cypress Semiconductor Corp. (Nasdaq: CY) today introduced a new series from its PSoC® 4 programmable system-on-chip architecture. The new PSoC 4 L-Series is the industry's most integrated single-chip solution with a 32-bit ARM®-Cortex®-M0 core, adding up to 256KB flash memory, 98 general purpose I/Os, 33 programmable analog and digital blocks, a USB device controller, and a control area network (CAN) interface. The PSoC 4 L-Series is ideal for a broad range of industrial and consumer applications, leveraging the flexibility of the PSoC architecture to address multiple product variations and Cypress's industry-leading CapSense® capacitive touch-sensing

technology to implement reliable and elegant user interfaces.

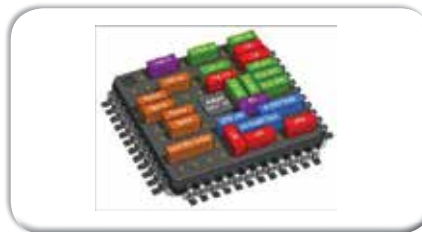
“The award-winning PSoC 4 portfolio has enabled customers to easily migrate from proprietary 8-bit and 16-bit MCUs to the industry’s most integrated ARM Cortex-M0 System-on-Chip,” said John Weil, vice president of MCU marketing at Cypress. “The PSoC 4 L-Series introduces new capabilities such as dual-mutual CapSense blocks with up to 94 channels for large, capacitive-touch home appliance applications and USB and programmable digital blocks to create bit-perfect digital audio solutions. Additionally, it provides all the resources needed to create new products for the emerging USB Type-C market.”


The PSoC 4 L-Series delivers up to 13 programmable analog blocks including 4 high-performance opamps, 4 current-output digital-to-analog converters (IDACs), 2 low-power comparators, a 12-bit SAR ADC and dual CapSense blocks with up to 94 capacitive-sensing channels. The programmable analog blocks enable engineers to create on-chip, custom analog front ends to support new end-product features, without increasing product costs, size or power consumption.

The PSoC 4 L-Series delivers up to 20 programmable digital blocks including 8 timer/counter/PWM blocks, 4 serial communication blocks and 8 Universal Digital Blocks (UDBs)—programmable digital blocks that each contain two programmable logic devices, a programmable data path and status and control registers. UDBs can be configured as coprocessors to offload compute-intensive tasks from the ARM Cortex-M0 core. The blocks also enable engineers to implement custom digital peripherals, state

machines or glue logic. Traditional MCUs typically require additional ICs to implement this functionality.

The scalable PSoC 4 architecture is complemented by the easy-to-use PSoC Creator™ Integrated Design Environment (IDE), which simplifies system design and accelerates time-to-market by enabling concurrent hardware and firmware design, and PSoC Components—free embedded ICs represented by an icon in the IDE. Together they enable rapid prototyping of end applications while minimizing PCB spins and firmware changes that are typically required.



 **Phoenix Contact’s highly reliable AC charging cables and AC charging controllers for E-mobility now available through TTI, Inc.**

Now available in Europe through TTI, Inc., a world leading specialist distributor of electronic components, is Phoenix Contact’s highly reliable range of AC charging cables and AC charging controllers for E-mobility applications. The devices enable the implementation of various concepts for intelligent charging infrastructures which can be used to promote cost-effective operation.

Ergonomically designed AC vehicle connectors Type 2 have been developed for the European market on the basis of IEC 62196-2 and allow charging electric vehicles safely (thanks to a locking mechanism), and conveniently (thanks to additional

gripping components). Depending on the cable diameter and the number of phases (single-phase or three-phase) charging with a rated voltage of 250V or 480V and rated current of 20A or 32A is possible. Highly robust and made of high-quality materials, the components benefit from strong strain relief and low insertion and withdrawal forces.

AC charging controllers ensure a high degree of security and interoperability with electric vehicles according to IEC 61851-1. The EV Charge Control Basic is a compact, cost-effective controller solution specifically designed for simple charging points (wall boxes for home garages, carports, and underground garages). It features configurable inputs, outputs, and charging currents. A standardized interface (Modbus RTU Slave) allows for fast and simple integration. The EV Charge Control Advanced is the solution for commercial applications and enables the connection to load and energy management systems including fleet management (company premises and semi-public parking lots). All necessary charging point controller functions are integrated. An Ethernet interface allows for configuration and operation. Any arrangement of scalable charging infrastructures can be set up. Charging initiation, status monitoring, and energy monitoring is done via Modbus TCP.



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New-Tech
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www.new-techeurope.com

The image features a word cloud with terms like TECHNOLOGY, NETWORKING, COMMUNICATION, ANALYSIS, and TEAMWORK. A tablet in the foreground displays the New-Tech Europe website interface, showing various articles and navigation options.



Scalable Memory Expansion, Enhanced Security and Flexible I/O Capabilities

Kinetis K8x MCU Family

The K8x MCU family offers the security, scalability, and flexibility to address the challenges of creating smart devices for the Internet of Tomorrow.

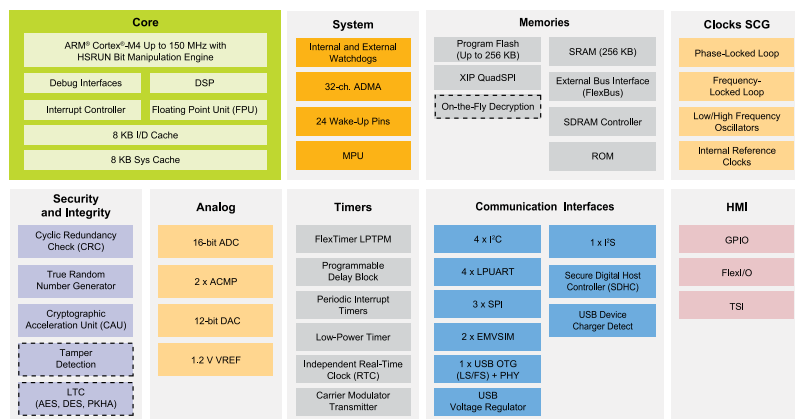
TARGET APPLICATIONS

- ▶ Building control
- ▶ Home automation and security
- ▶ IoT data concentrators
- ▶ Point-of-sale
- ▶ Portable healthcare
- ▶ Smart energy gateways
- ▶ Wearables

The Kinetis K8x MCU family extends the Kinetis MCU portfolio with advanced security capabilities including:

- ▶ Boot ROM to support encrypted firmware updates
- ▶ Automatic decryption and execution from external NOR flash memory
- ▶ Hardware AES acceleration with side band attack protection
- ▶ Support for public key cryptography

KINETIS K8x MCU FAMILY BLOCK DIAGRAM



Optional



TECHNOLOGY
DAY

22 March 2016 Dan Panorama Hotel, Tel Aviv



