New-Tech Europe November 2016

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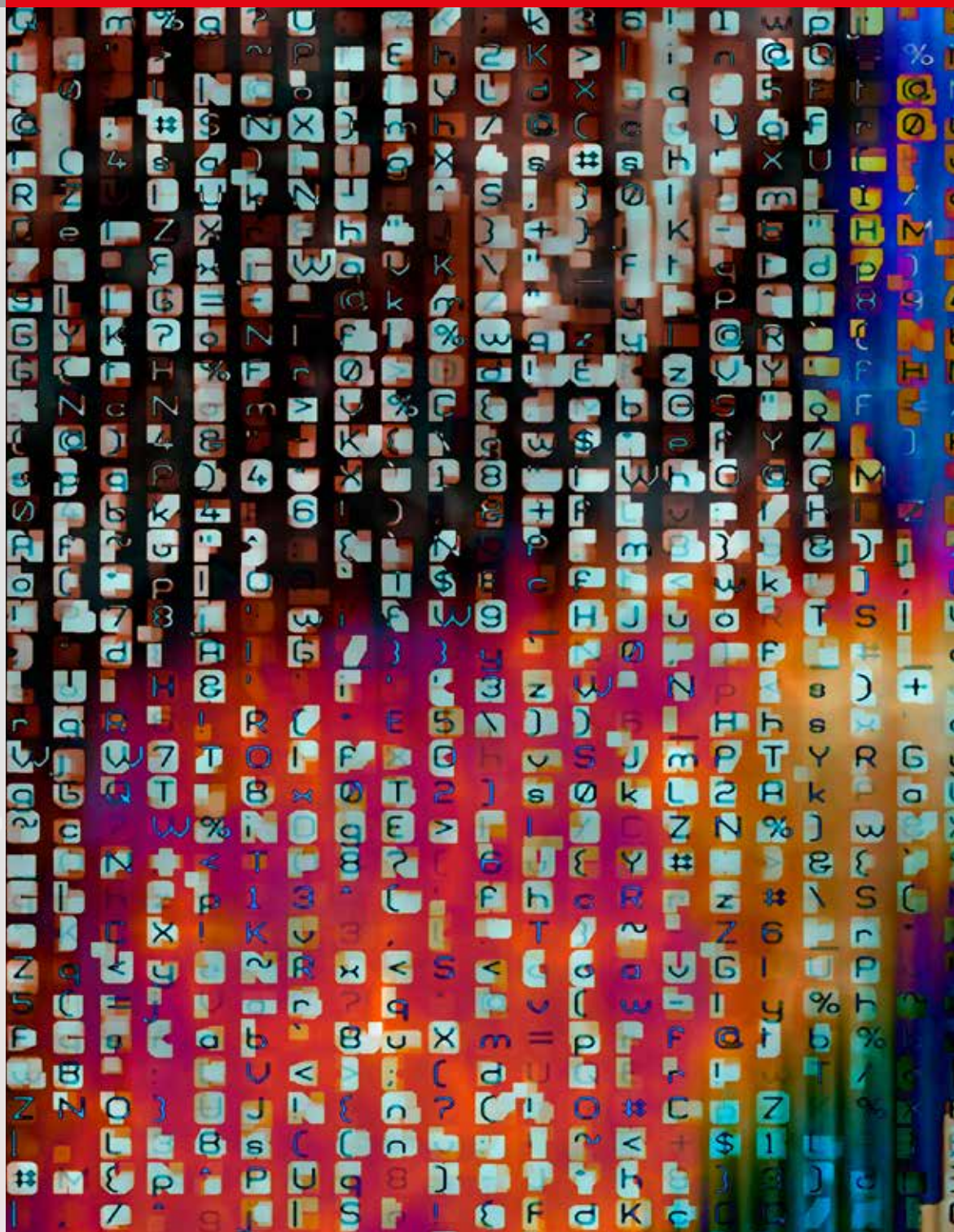

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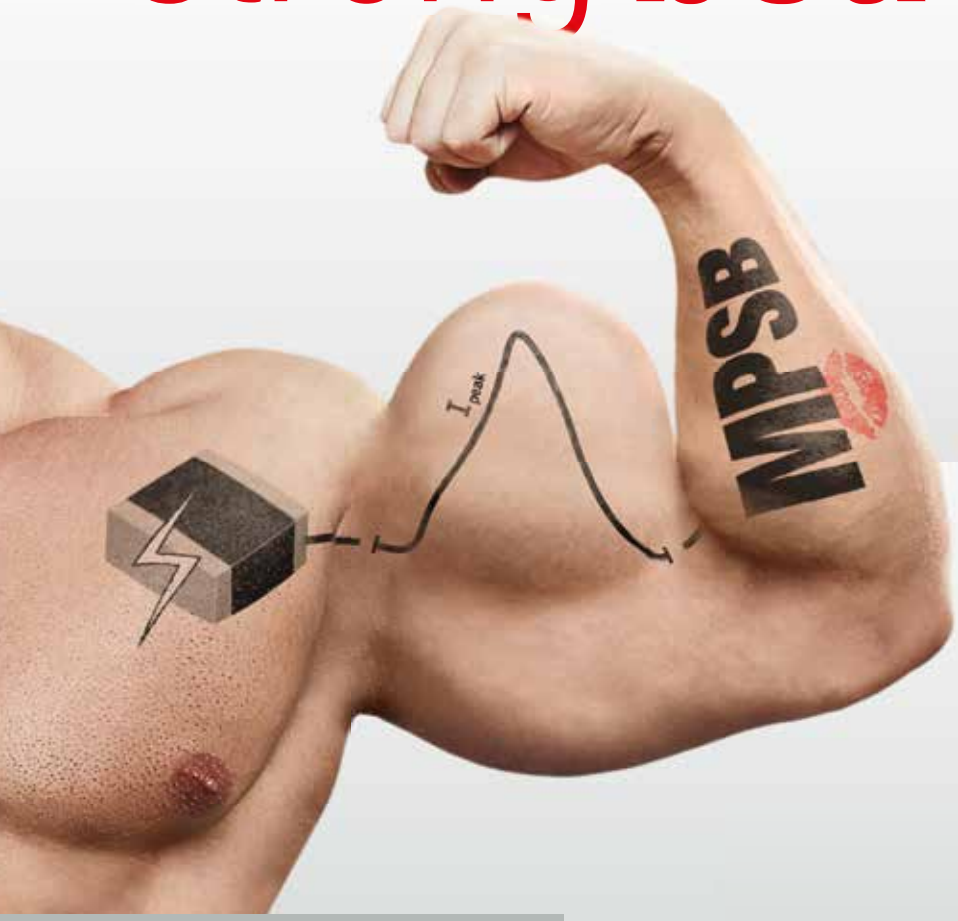

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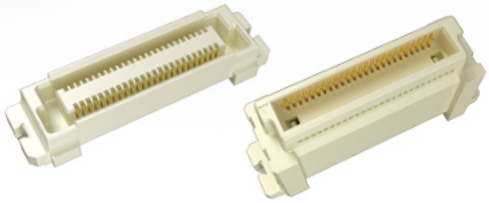

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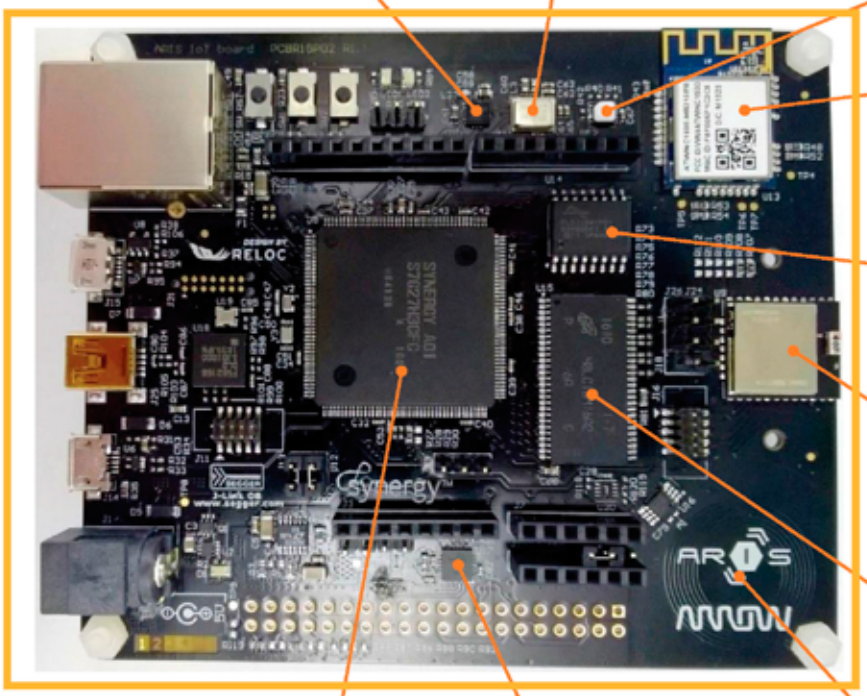

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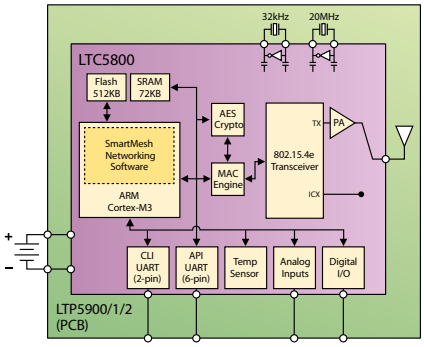

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New-Tech Europe

Read To Lead

November 2016

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About New-Tech Magazines Group

'New-Tech Magazines' A world leader in publishing high-tech and electronics, producing top quality publications read by tens of thousands professionals from all over the world especially from Europe, innovative electronics, IoT, microwave, homeland security, aerospace, automotive and technological industries.

Our specialized target audiences prefer New-Tech Europe because they know that our publications are a reliable source of the latest information in their respective fields. Our multidimensional editorials, news items, interviews and feature articles provide them with a full, well-rounded picture of the markets in which they operate - an essential asset for every technological leader striving to stay ahead, make the right decisions, and generate the next global innovation.

Moreover, as an attractive platform for advertisers from around the world, New-Tech Europe has become a hub for bustling international commercial activity. Here, through ads and other promotional materials, Israeli readers obtain crucial information about developers and manufacturers worldwide, finding the tools, instruments, systems and components they need to facilitate their innovative endeavors.

Targeting the needs of both the global and european industries and global advertisers, New-Tech Magazines Group constantly expands and upgrades its services. Over the years, the company has been able to formulate a remarkably effective, multi-medium mix of offerings, combining magazine publications with useful online activities, newsletters and special events and exhibitions.

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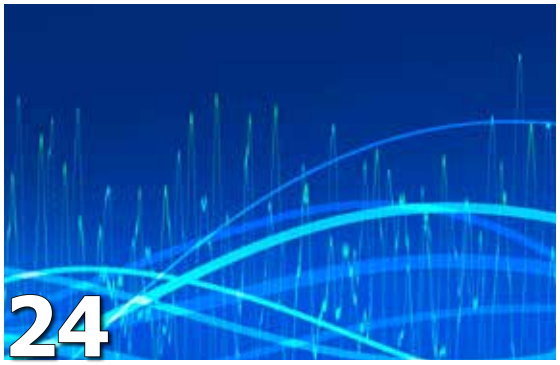


Students at electronica Win Great Prizes Sponsored by Digi-Key

THIEF RIVER FALLS, Minnesota, USA – Fourteen lucky students attending Student Day at electronica in Munich won prizes sponsored by Digi-Key Electronics, a global electronic components distributor. At the end of Student Day, "Captain Jack Sparrow" announced the winners of the raffle giveaway in true pirate fashion. Students won one of 4 e-bikes or 10 InstaLab kits.

The InstaLab was created to have enough gear to turn an electronics student's dorm room into their own maker space. The kit includes over 20 different products from many of Digi-Key's trusted supplier partners. Some of the products include an oscilloscope, function generator, a HTU21D Humidity, Temperature Sensor Xplained Pro Platform Evaluation Expansion Board, and a Digi-Key Ruler.

Digi-Key Electronics was a Platinum Sponsor of Student Day at electronica Munich as part of their continuous commitment to supporting education and STEM at all levels. They also encourage students to attend the 2018 electronica event where there will be more exciting giveaways and great opportunities to learn about the electronics industry.

Paris Saint-Germain announces digital experience partnership with Ericsson

Ericsson will provide football club Paris Saint-Germain with a range of solutions and services that will transform the digital experience for fans, players and support staff This will include a sports performance information system, a digital experience backend system, and technology consulting and innovation services Together with Paris Saint-Germain's staff, Ericsson will ensure that the international club becomes one of the most technologically advanced In a press conference held at the iconic Parc des Princes stadium today, Paris Saint-Germain and Ericsson (NASDAQ: ERIC) announced their official partnership, focused on building the new digital experience of the Parisian club. With Ericsson's expertise, the club will become one of the leaders of sports technology.

Under the terms of the four-year agreement, Ericsson will become an Official Partner and provide Paris Saint-Germain with a range of solutions and services that will transform the digital experience for fans, players and support staff alike. Ericsson will provide Paris Saint-Germain with three main types of support: a sports performance information system; a digital experience backend system; and technology consulting and innovation services.

This partnership will allow Ericsson to showcase its digital know-how and engage with football fans globally thanks to the club's growing international footprint.

Frédéric Longuépée, Paris Saint-Germain Deputy General Manager, says: "We are delighted to welcome Ericsson to the Paris Saint-Germain family. One of our aims as a club is to become one of the top sports franchises in the world, and digital transformation is clearly a key priority. We are confident signing with Ericsson represents a major step forward. We aim to make the most from existing and future technology to further enrich the experience of all the club's stakeholders."

Helena Norrman, Senior Vice President and Chief Marketing and Communications Officer, says: "We are very excited with this agreement that will both help Paris Saint-Germain to improve its sports performance and its fan experience, as well as allow Ericsson to show its technological leadership. Together with Paris Saint-Germain's staff, we will ensure that one of the most successful football clubs is also one of the most technologically advanced."

From left to right: Frederic Longuépée, Deputy General Manager at Paris Saint-Germain, Patrick Kluivert, Director of Football at Paris Saint-Germain, Helena Norrman, Senior Vice President and Chief Marketing and Communications Officer at Ericsson, Franck Bouetard, Head of Ericsson France, and Boris Serapian, Chief Information Officer at Paris Saint-Germain

Ericsson will create, operate and manage a sports performance information system as a service for Paris Saint-Germain. The information system will consist of a centrally managed data storage platform that stores, manages and controls data captured from all of Paris Saint-Germain's sports-related businesses.

Secondly, Ericsson will create, operate and manage a digital experience backend system which will be the single point of access to data and services required by all of Paris Saint-Germain's digital platforms, including its web site, mobile apps, onsite fan experience solution, and in-stadium big screens and monitors.

Thirdly, Ericsson will provide Paris Saint-Germain with technology consulting and innovation services. A joint team of Ericsson and Paris Saint-Germain staff will analyze and define new solutions, innovations and improvements.

New Automotive Chips from STMicroelectronics Bring High-End Graphics, Audio, and Video to Entry and Mid-Range Vehicles

Full-digital instrument panels that give a high-end feel to any car are coming to the mid and entry ranges, enabled by new technology from STMicroelectronics (NYSE: STM) , a global semiconductor leader serving customers across the spectrum of electronics applications and a top supplier of advanced automotive ICs.

ST's new Accordo 5 family of automotive processors meet crucial display-performance and security demands in a low-power compact platform suitable for lower-cost vehicles. The devices enable state-of-the-art digital instrument clusters and Audio/Video/Navigation (AVN) head units to become more affordable than ever by integrating the complete graphics, video, and audio functionality on-chip to save design costs and simplify assembly.

Accordo 5 devices provide features that have high value for car drivers, including smartphone mirroring that gives access to content such as music and navigation services on the phone safely through the vehicle's own user interface. The state-of-the-art host processor and high-performance video and graphics engines can present complex information displays, such as simultaneous user-interface plus rear-view camera with navigation and video preview. There is also video playback for major formats including H.264 and DivX®, 2D and 3D graphics with effects such as blending and overlays, as well as USB connections and SD-Card interfaces.

Less visible to users, but critically important to today's increasingly connected cars, Accordo 5 chips integrate a high-performance microcontroller that secures the interface between the head unit and the main vehicle network. Built-in features of this microcontroller include boot-code authentication, secure interconnect, and high-performance data encryption.

The Accordo 5 family is the latest generation of ST's successful Accordo line and leapfrogs other digital-infotainment chips, leveraging ARM® Cortex®-A7 processor as the main computing CPU. The Cortex-A7 architecture is highly area-efficient, and therefore cost-effective, with high processing and memory-streaming performance. The Accordo 5 range gives designers a choice of single-core Cortex A7 with a 16-bit interface to high-performing off-chip DDR3, or dual-core Cortex-A7 with a 16/32-bit DDR3 interface.

Although targeting mid-range vehicle markets, Accordo 5 delivers best-in-class graphics performance from its 500MHz 3D graphics processor core. The architecture supports 2D and 3D graphics up to 1080p resolution, in well-known formats like OpenVG, OpenGLES-2.0, and is capable of effects such as flexible blending of up to four layers with multiple modes and video overlay. The multi-format video subsystem provides post-processing for effects such as picture-in-picture, and virtuoso audio performance comes from a high-performance audio DSP, six stereo-audio analog channels, and support for multiple industry-standard audio interfaces. The built-in display controller supports TFT-LCD touch panels up to Full HD definition.

The new family further strengthens security by dedicating an ARM Cortex-M based microcontroller for managing the secure CAN interface between digital instruments and the main vehicle network. This microcontroller integrates three CAN ports including support for the latest CAN FD high-speed standard, a hardware accelerator for crypto algorithms including SHA-2, PK and AES, and One-Time-Programmable (OTP) memory for master-key storage and tamper prevention. The microcontroller draws very little current in standby mode, and complements careful power management throughout the chip to minimize drain on the vehicle's electrical supply.

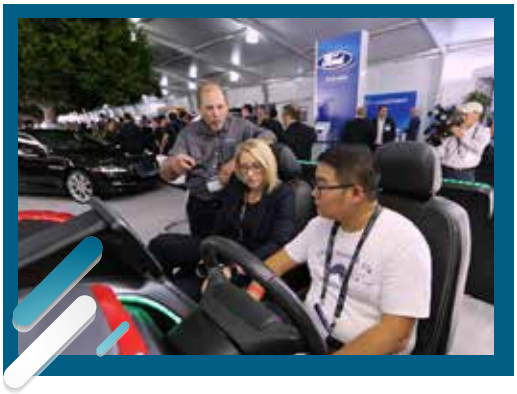
Analog Devices Acquires Laser Beam Steering Technology from Vescent Photonics to Enable Mainstream Adoption of Automotive LIDAR Systems

Analog Devices, Inc. (ADI) announced the acquisition of a solid-state laser beam steering technology from Vescent Photonics, Inc., a privately held company based in Golden, Colorado. Vescent's innovative non-mechanical beam steering technology enables more robust integrated LIDAR1 systems that overcome many of the major drawbacks associated with today's bulky mechanical offerings such as reliability, size, and cost. This acquisition strengthens ADI's position as a major automotive safety system technology partner for next generation ADAS and autonomous driving applications and builds on ADI's 20-year history in advancing automotive safety.

"From inertial MEMS sensors used in airbag and electronic stability control applications2 to 24 GHz and 77 GHz automotive RADAR, ADI solutions have helped save lives for over two decades," said Chris Jacobs, general manager of Automotive Safety, Analog Devices. "And now, this innovative technology will play an important role in making LIDAR systems more compact, more robust, and an affordable feature in every new car worldwide."

Today's ADAS systems must rely on a suite of sensor technologies that include cameras, RADAR, and LIDAR to effectively provide advanced safety features such as forward collision warning, blind spot detection, pedestrian detection, and autonomous driving functions. Cameras are used widely for object recognition while RADAR uses radio-frequency electromagnetic waves to measure distance. LIDAR uses laser beams to measure the distance and can also recognize objects. Scanning LIDAR systems can be used to detect objects on or near the roadway and fill the blind spots known to exist when using RADAR & cameras.

Intel Announces $250 Million Investment for Autonomous Driving



Delivering his keynote address at the LA Auto Show's AutoMobility conference, Intel CEO Brian Krzanich announced that Intel Capital is targeting more than $250 million of additional new investments over the next two years to make fully autonomous driving a reality. This is the first time Intel is keynoting at an automotive conference, signifying how critical the automotive market has become for the company.

These investments will drive the development of technologies that push the boundaries on next-generation connectivity, communication, context awareness, deep learning, security, safety and more. Drilling down into the areas that will be fueled by the fresh investments, Krzanich highlighted technologies that will drive global Internet of Things (IoT) innovation in transportation; areas where technology can directly mitigate risks while improving safety, mobility, and efficiency at a reduced cost; and companies that harness the value of the data to improve reliability of automated driving systems.

Addressing a large crowd of automotive and technology industry representatives, Krzanich talked about how the automotive industry is on the cusp of a major transformation, demanding unprecedented levels of computing, intelligence and connectivity. With the variety of sensors, sonar, LIDAR and cameras that will come embedded in autonomous cars, he highlighted the need for the industry to be prepared for the data deluge with over 4,000 GB of data coming from a single car each day.

The announcement is part of Intel's ongoing work with automakers and system suppliers to help integrate advanced technologies into cars. The automotive industry is on the cusp of a technological revolution that is set to have tremendous social, cultural and economic effects on our lives. Self-driving vehicles, which seemed like figments of our imagination even five years ago, can decrease accidents and save human lives. They can save the U.S. economy $121 billion a year in wasted time and fuel, and offer unprecedented levels of mobility to the elderly and disabled.

Delivering on this promise will require the full depth and breadth of Intel's portfolio and expertise.

To meet the needs of the auto industry, Intel has developed a platform solution that spans both hardware and software for Advanced Driver Assisted Systems (ADAS), Software Defined Cockpits and the heavy compute capabilities required for the fully autonomous cars of tomorrow. These solutions include scalable compute architectures stretching from the Atom to Xeon processors, coupled with capabilities in vision processing, 5G, cloud, machine learning and security. This allows automakers the freedom to realize their unique IP, provide experiences to consumers not yet imagined, and deliver the ability to securely update their platforms with new algorithms and features over the lifetime of the vehicle. The Intel advantage is a consistent architecture that the industry can work with that scales literally from a developer's laptop to the data center.

A proven partner for automakers and suppliers, Intel has booked more than $1 Billion worth of design win revenue in the past 12 months. The company also has 49 design wins with leading global car manufacturers including BMW, Daimler, Hyundai, Infiniti, Jaguar XF, Kia, Lexus, Mini Cooper, Rolls Royce, Toyota, Tesla and others.

World's fastest gas detector to prevent global warming

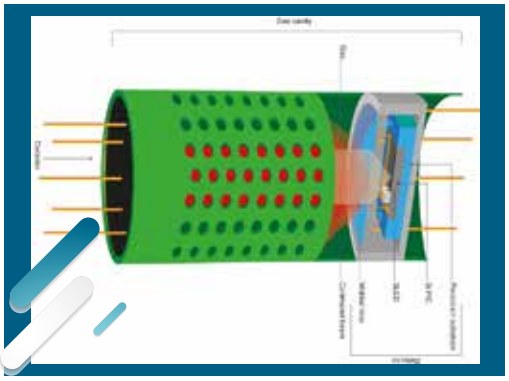
sing new photonics technology, European scientists are developing a multi-gas detector that can spot dozens of harmful emissions with a single sensor in milliseconds, delivering a breakthrough for the prevention climate change.

The Intergovernmental Panel on Climate Change (IPCC) estimates that concentrations of Methane (CH4) in the atmosphere are roughly two and a half times those of pre-industrial times. The primary component of natural gas, Methane is over 20 times more effective at trapping heat than carbon dioxide and can remain in the atmosphere for more than a decade.

With natural gas and petroleum systems being the largest source of CH4 emissions from industry, and with the USA pledging

a 40-45% reduction in methane emissions from 2012 levels by 2025, it has never been more important to have effective monitoring equipment.

Exploiting new photonics technology, the H2020 project MIREGAS ('Mid-IR source for Gas Sensing') has come up with their solution: a novel, low cost sensor that has the potential to be programmed to detect an unlimited number of gases.



The first of its kind, MIREGAS aims to deliver a single, multi-band gas sensor that can be easily deployed in strategic points of methane emissions, such as on oil rigs or in industrial areas, and monitor dozens of Greenhouse gasses all at once.

While current technology can take up to 10 seconds to produce a positive ID, the device can detect dozens of harmful emissions in milliseconds, making it several thousand times faster state of the art gas sensors, and, effectively a real-time instrument.

The device can pick out poisonous gases from a mixture of emissions, including methane, ethane, butane, propane, CO2, carbon monoxide, hydrogen sulphide and benzene, all from one compact filter.

Combining the principles seen in fibre optic communications, the MIREGAS light source exploits multiplexing-to-demultiplexing filters, modulating and wavelength tuning, with Mid-IR spectroscopic sensing technologies, a process never seen before.

Professor Pentti Karioja from the VTT Technical Research Centre of Finland Ltd, explains:

"Because the MIREGAS device is adjustable, it is possible to use only one light source instead of several lasers. This means that we can make multiple readings and monitor several harmful gases simultaneously through one sensor."

While Mid IR spectroscopic equipment exists, current sensors are based on the use of filters, spectrometers or tuneable lasers, meaning a several lasers would be needed for corresponding gases.

Initially the MIREGAS device is expected to be deployed in several industrial fields such as building ventilation, process control and safety, gas leakage monitoring, personal, pipeline and explosion safety. However the capabilities for observing dangerous greenhouse gasses in our atmosphere will provide practical tools for tackling climate change.

At the foreseen manufacturing cost of below €300 per unit, the proposed approach is extremely competitive against conventional gas sensors which can cost in excess of €75,000.

Coordinated in Finland by VTT, the MIREGAS project has received a grant of €3,588,262 from H2020 via the Photonics Public Private Partnership. MIREGAS is comprised of a consortium of members from Finland, Poland and Norway, including Tampere University of Technology, Vaisala OYJ, the Instytut Technologii Materialow Elektronicznych, Airoptic, Vigo System S.A. and Gassecure AS.

DELTA Microelectronics Expands UK Presence, Partners with Solution in Silicon Copenhagen

DELTA Microelectronics, the European leader in ASIC supply chain services, announces today that it has partnered with Solution in Silicon to augment UK sales and customer support.

Solution in Silicon has a rich experience offering ASIC sales and support services to companies in a wide range of industries including consumer products, medical equipment, communications, IoT and security.

The new partnership will provide UK customers access to DELTA's extensive supply chain services including wafer procurement and probing, packaging, component testing, storage and IC distribution.

DELTA operates the largest microelectronics testing facilities in Europe, which ensure the highest quality control measures and a low-risk path to production. David Waller, Solution in Silicon founder CEO added: "Our collaboration with a leading ASIC service provider like DELTA will provide our fabless customers a complete, high-quality supply chain management service from GDSII tape to tested and packaged parts.

"With this step we are responding to an increase in demand for our ASIC supply chain services," said Gert Jørgensen, DELTA's VP of Sales & Marketing. "The UK is a key market for us and Solution in Silicon is an outstanding partner that will step up our response to customers."

Rolls-Royce and VTT Technical Research Centre form a strategic partnership to develop smart ships

Rolls-Royce and VTT Technical Research Centre of Finland Ltd have announced a strategic partnership to design, test and validate the first generation of remote and autonomous ships. The new partnership will combine and integrate the two company's unique expertise to make such vessels a commercial reality.

Rolls-Royce is pioneering the development of remote controlled and autonomous ships and believes a remote controlled ship will be in commercial use by the end of the decade. The company is applying technology, skills and experience from across its businesses to this development.

VTT has deep knowledge of ship simulation and extensive expertise in the development and management of safety-critical and complex systems in demanding environments such as nuclear safety. They combine physical tests such as model and tank testing, with digital technologies, such as data analytics and computer visualisation. They will also use field research to incorporate human factors into safe ship design. As a result of working with the Finnish telecommunications sector, VTT has extensive experience of working with 5G mobile phone technology and wi-fi mesh networks. VTT has the first 5G test network in Finland.

Working with VTT will allow Rolls-Royce to assess the performance of remote and autonomous designs through the use of both traditional model tank tests and digital simulation, allowing the company to develop functional, safe and reliable prototypes.

Karno Tenovuo, Rolls-Royce, Vice President Ship Intelligence, said: "Remotely operated ships are a key development project for Rolls-Royce Marine, and VTT is a reliable and innovative partner for the development of a smart ship concept. This collaboration is a natural continuation of the earlier User Experience for Complex systems (UXUS) project, where we developed totally new bridge and remote control systems for shipping."

Erja Turunen, Executive Vice President at VTT, said: "Rolls-Royce is a pioneer in remotely controlled and autonomous shipping. Our collaboration strengthens the way we can integrate and leverage VTT's expertise in simulation and safety validation, including the industrial Internet of Things, to develop new products and in the future, enable us to develop new solutions for new areas of application as well."

IBM Launches Experimental Platform for Embedding Watson into Any Device

IBM (NYSE: IBM) today unveiled the experimental release of Project Intu, a new, system-agnostic platform designed to enable embodied cognition. The new platform allows developers to embed Watson functions into various end-user device form factors, offering a next generation architecture for building cognitive-enabled experiences.

Project Intu, in its experimental form, is now accessible via the Watson Developer Cloud and also available on Intu Gateway and GitHub.

Project Intu simplifies the process for developers wanting to create cognitive experiences in various form factors such as spaces, avatars, robots or other IoT devices, and it extends cognitive technology into the physical world. The platform enables devices to interact more naturally with users, triggering different emotions and behaviors and creating more meaningful and immersive experience for users.

Developers can simplify and integrate Watson services, such as Conversation, Language and Visual Recognition, with the capabilities of the "device" to, in essence, act out the interaction with the user. Instead of a developer needing to program each individual movement of a device or avatar, Project Intu makes it easy to combine movements

that are appropriate for performing specific tasks like assisting a customer in a retail setting or greeting a visitor in a hotel in a way that is natural for the end user.

Typically, developers must make architectural decisions about how to integrate different cognitive services into an end-user experience – such as what actions the systems will take and what will trigger a device's particular functionality. Project Intu offers developers a ready-made environment on which to build cognitive experiences running on a wide variety of operating systems – from Raspberry PI to MacOS, Windows to Linux machines, to name a few. As an example, IBM has worked with Nexmo, the Vonage API platform, to demonstrate the ways Intu can be integrated with both Watson and third-party APIs to bring an additional dimension to cognitive interactions via voice-enabled experiences using Nexmo's Voice API's support of websockets.

The growth of cognitive-enabled applications is sharply accelerating. IDC recently estimated that "by 2018, 75 percent of developer teams will include Cognitive/AI functionality in one or more applications/services." * This is a dramatic jump from last year's prediction that 50 percent of developers would leverage cognitive/AI functionality by 2018.

"IBM is taking cognitive technology beyond a physical technology interface like a smartphone or a robot toward an even more natural form of human and machine interaction," said Rob High, IBM Fellow, VP and CTO, IBM Watson. "Project Intu allows users to build embodied systems that reason, learn and interact with humans to create a presence with the people that use them – these cognitive-enabled avatars and devices could transform industries like retail, elder care, and industrial and social robotics."

Project Intu is a continuation of IBM's work in the field of embodied cognition, drawing on advances from IBM Research, as well as the application and use of cognitive and IoT technologies. Making Project Intu available to developers as an experimental offering to experiment with and provide feedback will serve as the basis for further refinements as it moves toward beta.

Computers Made of Genetic Material? HZDR researchers conduct electricity using DNA-based nanowires

Tinier than the AIDS virus – that is currently the circumference of the smallest transistors. The industry has shrunk the central elements of their computer chips to fourteen nanometers in the last sixty years. Conventional methods, however, are hitting physical boundaries. Researchers around the world are looking for alternatives. One method could be the self-organization of complex components from molecules and atoms. Scientists at the Helmholtz-Zentrum Dresden-Rossendorf (HZDR) and Paderborn University have now made an important advance: the physicists conducted a current through gold-plated nanowires, which independently assembled themselves from single DNA strands. Their results have been published in the scientific journal Langmuir.

At first glance, it resembles wormy lines in front of a black background. But what the electron microscope shows up close is that the nanometer-sized structures connect two electrical contacts. Dr. Artur Erbe from the Institute of Ion Beam Physics and Materials Research is pleased about what he sees. "Our measurements have shown that an electrical current is conducted through these tiny wires." This is not necessarily self-evident, the physicist stresses. We are, after all, dealing with components made of modified DNA. In order to produce the nanowires, the researchers combined a long single strand of genetic material with shorter DNA segments through the base pairs to form a stable double strand. Using this method, the structures independently take on the desired form.

"With the help of this approach, which resembles the Japanese paper folding technique origami and is therefore referred to as DNA-origami, we can create tiny patterns," explains the HZDR researcher. "Extremely small circuits made of molecules and atoms are also conceivable here." This strategy, which scientists call the "bottom-up" method, aims to turn conventional production of electronic

components on its head. "The industry has thus far been using what is known as the 'top-down' method. Large portions are cut away from the base material until the desired structure is achieved. Soon this will no longer be possible due to continual miniaturization." The new approach is instead oriented on nature: molecules that develop complex structures through self-assembling processes.

Golden Bridges Between Electrodes

The elements that thereby develop would be substantially smaller than today's tiniest computer chip components. Smaller circuits could theoretically be produced with less effort. There is, however, a problem: "Genetic matter doesn't conduct a current particularly well," points out Erbe. He and his colleagues have therefore placed gold-plated nanoparticles on the DNA wires using chemical bonds. Using a "top-down" method – electron beam lithography – they subsequently make contact with the individual wires electronically. "This connection between the substantially larger electrodes and the individual DNA structures have come up against technical difficulties until now. By combining the two methods, we can resolve this issue. We could thus very precisely determine the charge transport through individual wires for the first time," adds Erbe.

As the tests of the Dresden researchers have shown, a current is actually conducted through the gold-plated wires – it is, however, dependent on the ambient temperature. "The charge transport is simultaneously reduced as the temperature decreases," describes Erbe. "At normal room temperature, the wires function well, even if the electrons must partially jump from one gold particle to the next because they haven't completely melded together. The distance, however, is so small that it currently doesn't even show up using the most advanced microscopes." In order to improve the conduction, Artur Erbe's team aims to incorporate conductive polymers between the gold particles. The physicist believes the metallization process could also still be improved.

He is, however, generally pleased with the results: "We could demonstrate that the gold-plated DNA wires conduct energy. We are actually still in the basic research phase, which is why we are using gold rather than a more cost-efficient metal. We have, nevertheless, made an important stride, which could make electronic devices based on DNA possible in the future."

Publication: B. Teschome, S. Facsko, T. Schönherr, J. Kerbusch, A. Keller, A. Erbe: Temperature-Dependent Charge Transport through Individually Contacted DNA Origami-Based Au Nanowires, in Langmuir, 2016, 32 (40), pp 10159–10165 (DOI: 10.1021/acs.langmuir.6b01961)

Xilinx Unveils Details for New 16nm Virtex UltraScale+ FPGAs with High Bandwidth Memory and CCIX Technology

Xilinx, Inc. (NASDAQ:XLNX) today unveiled details for new 16nm Virtex® UltraScale+™ FPGAs with HBM and CCIX technology. Containing the highest memory bandwidth available, these HBM-enabled FPGAs offer 20X higher memory bandwidth relative to a DDR4 DIMM and 4X less power per bit versus competing memory technologies. The new devices are architected to support the higher memory needs of compute-intensive applications such as machine learning, Ethernet connectivity, 8K video, and radar. They also contain CCIX IP, enabling cache-coherent acceleration to any CCIX-enabled processor to address compute acceleration applications.

"In package integration of DRAM represents a massive leap forward in memory bandwidth for high end FPGA-enabled applications," said Kirk Saban, senior director of FPGA and SoC Product Management at Xilinx. "HBM integration in our industry leading devices provides a clear path to multi-terabit memory bandwidth and our acceleration enhanced technology will enable efficient heterogeneous computing for our customers' most

demanding workloads and applications."

Based on the proven 16nm Virtex UltraScale+ FPGA family, which started sampling in 2015, the HBM-optimized Virtex UltraScale+ products offer the lowest-risk approach to HBM integration. The family is built using 3rd generation CoWoS technology—co-developed by TSMC and Xilinx and now the industry standard assembly for HBM integration.

Detailed device tables and product documentation is available on all four new devices at https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html.

Siemens and Bentley Systems Advance Strategic Alliance Including Joint Investment Initiatives

Siemens and Bentley Systems announced today that they have formalized a strategic alliance agreement to drive new business value by accelerating digitalization to advance infrastructure project delivery and asset performance in complementary business areas. Siemens and Bentley Systems will initially invest at least Euro 50 million in developing joint solutions to enlarge their respective offerings for infrastructure and industry to the benefit of the end-customers. This work will uniquely leverage new cloud services for a connected data environment to converge respective digital engineering models from both companies. In addition to those elements of the agreement, approximately Euro 70 million of secondary shares of Bentley's common stock have been acquired by Siemens, under a company program that will continue until such time as Bentley Systems' stock is publicly traded.

Siemens and Bentley Systems have a track record of complementing their respective portfolios through the licensing of each other's technology to provide solutions in the Digital Factory and Process Industries & Drives divisions, where respective software offerings have already been integrated. For example, Bentley's reality modeling software has been integrated into Siemens Process Simulate to leverage laser-scanned point clouds in modeling the existing context of brownfield industrial environments. The automotive industry manufacturer Turnkey Manufacturing Systems (TMS) successfully employed the innovative point cloud capabilities to create a "digital twin" of their production line to significantly enhance their planning and validation processes, while saving time and costs.

The new investment initiatives will involve virtually all Siemens divisions. The major benefit will be accumulating intelligence from Siemens solutions throughout Bentley's complementary applications for design modeling, analytical modeling, construction modeling and asset performance modeling. As a result, the integrated and accessible digital engineering models, such as the "digital twin" viewed through an immersive 3D interface, will enable unprecedented operational performance, visibility and reliability. This work will uniquely converge digital engineering models: physical engineering models in their 3D physical reality context by way of Bentley's software solutions and the corresponding functional engineering 2D models within Siemens' solutions.

Siemens and Bentley Systems have identified opportunities to work together in Energy Management, Power Generation, Building Technology and Mobility where each company can leverage their respective technology and industry expertise to bring new business value to the market. For example, Bentley's applications for the 3D modeling and structural analysis of industrial and infrastructure assets complement Siemens' solutions and unparalleled domain expertise in electrification and automation. Siemens and Bentley Systems will each provide software from the other to deliver complete solutions from either company to the benefit of their respective customers in order to improve their project and asset performance through simulation and virtual commissioning. Development work will benefit from and extend Siemens' and Bentley Systems' established commitments to openness and interoperability.

Klaus Helmrich, member of the Managing Board of Siemens AG, said, "This move further extends our industry software ecosystem from 2D to 3D software solutions, taking the simulation portfolio in our Digital Enterprise offering to a new dimension. We're rigorously executing our 'digital twin' vision from virtual planning to the real product to the benefit of our customers who themselves are driving digitalization across their value chains. Bentley Systems' independence, track record in interoperability and leadership in engineering- and design-software make them our ideal partner for this undertaking."

Bentley Systems CEO Greg Bentley said, "Only with

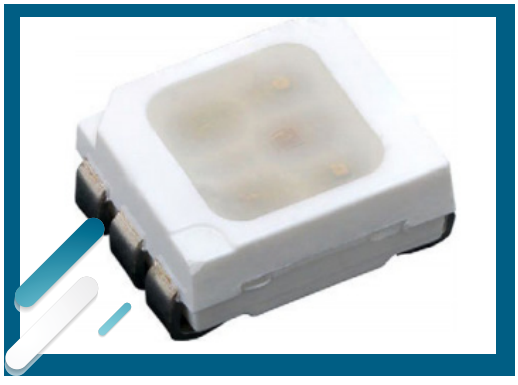
Siemens could we so purposefully advance beyond merely linking the 'Industrial Internet of Things' to ultimately leverage digital engineering models for visual operations and connected infrastructure asset performance. Given our long history of sharing complementary technologies, we are very excited to now contribute so broadly to Siemens' industrial digitalization leadership."

Siemens AG (Berlin and Munich) is a global technology powerhouse that has stood for engineering excellence, innovation, quality, reliability and internationality for more than 165 years. The company is active in more than 200 countries, focusing on the areas of electrification, automation and digitalization. One of the world's largest producers of energy-efficient, resource-saving technologies, Siemens is No. 1 in offshore wind turbine construction, a leading supplier of gas and steam turbines for power generation, a major provider of power transmission solutions and a pioneer in infrastructure solutions as well as automation, drive and software solutions for industry. The company is also a leading provider of medical imaging equipment – such as computed tomography and magnetic resonance imaging systems – and a leader in laboratory diagnostics as well as clinical IT. In fiscal 2015, which ended on September 30, 2015, Siemens generated revenue of €75.6 billion and net income of €7.4 billion. At the end of September 2015, the company had around 348,000 employees worldwide. Further information is available on the Internet at www.siemens.com.

Bentley Systems is a global leader in providing architects, engineers, geospatial professionals, constructors, and owner-operators with comprehensive software solutions for advancing the design, construction, and operations of infrastructure. Bentley users leverage information mobility across disciplines and throughout the infrastructure lifecycle to deliver better-performing projects and assets. Bentley solutions encompass MicroStation applications for information modeling, ProjectWise collaboration services to deliver integrated projects, and AssetWise operations services to achieve intelligent infrastructure – complemented by worldwide professional services and comprehensive managed services. Founded in 1984, Bentley has more than 3,000 colleagues in over 50 countries, more than $600 million in annual revenues, and since 2009 has invested more than $1 billion in research, development, and acquisitions. Additional information about Bentley is available atwww.bentley.com.

Vishay Intertechnology RGB LED Provides Independent Control of Red, Green, and Blue Chips for Wide Color Range

Vishay Intertechnology, Inc. (NYSE: VSH) today introduced a new high-brightness, tricolor LED optimized for interior automotive lighting, RGB displays, and backlighting. Featuring separate red, green, and blue LED chips inside the compact 3.5 mm by 2.8 mm by 1.45 mm PLCC-6 surface-mount package, the Vishay Semiconductors VLMRGB6112.. enables individual control of each chip, making it possible to realize every color within the color room defined by the gamut triangle area inside the CIE 1931 color space through color mixing.



With its wide color range, the LED released today is ideal for custom "welcome illumination" in next-generation automobiles; large-format, full-color message and video display boards; backlighting in consumer devices and appliances such as PDAs, televisions, ovens, and microwaves; and a wide range of accent and decorative lighting. For these applications, the device utilizes high-brightness AlInGaP and InGaN technologies to deliver luminous intensity to 1800 mcd at 20 mA and features a ±60° angle of half intensity. Providing high reliability, the Automotive Grade VLMRGB6112.. offers a wide temperature range from -40 °C to +110 °C, excellent corrosion robustness and sulfur resistance (H2S), and a UV-stable, diffused silicone casting compound for a long lifetime. The LED is AEC-Q101-qualified, offers a Moisture Sensitivity Level (MSL) of 2, and withstands ESD voltages up to 2 kV in accordance with JESD22-A114-B. Compatible with IR reflow soldering, the device is RoHS-compliant, halogen-free, and Vishay Green.

RED new radio equipment directive for Europe

› Heinz Mellein, R&S

The new radio equipment directive (RED) is effective from mid-June onward. The directive also covers radio receivers; they will have to meet minimum performance requirements in terms of sensitivity and selectivity.

Radio transmissions only with permission

Whoever wants to transmit or receive radio signals in Europe must comply with the relevant European directives governing the approval of radio equipment. These directives are developed in close cooperation between the European Commission as a body taking an active part in political decision-making, the European Electronic Communications Committee (ECC) within the European Conference of Postal and Telecommunications Administrations (CEPT), both of them guardians of the ever more valuable frequency resources, as well as the European Telecommunications Standards Institute (ETSI, Fig. 1). In addition to general requirements relating, for example, to the protection of health and safety or environmental compatibility, the directives also contain fundamental technical requirements. All radio equipment must fulfill what is referred to as "essential requirements" in the applicable directives, during normal operation and under the operating conditions specified by the manufacturer (ambient temperature, humidity, etc.). Evidence of compliance must be furnished by the radio equipment manufacturer or operator as a prerequisite for obtaining approval for operating the equipment and putting it on the market. To this end, the manufacturer or operator must submit a test report that has been issued by a certified test laboratory using validated measuring equipment, for example from Rohde & Schwarz. Technical details on the diverse radio applications and frequency bands falling under the directives are specified in the "harmonized standards" developed by ETSI, along with possible test methods to demonstrate compliance. Harmonized standards become effective as European standards (EN) following a thorough examination by the regulatory bodies. Fig. 2 presents important examples of these standards. The currently applicable European standards are listed in the Official Journal of the European Union. An overview can be found on the ETSI website (www.etsi.org).

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	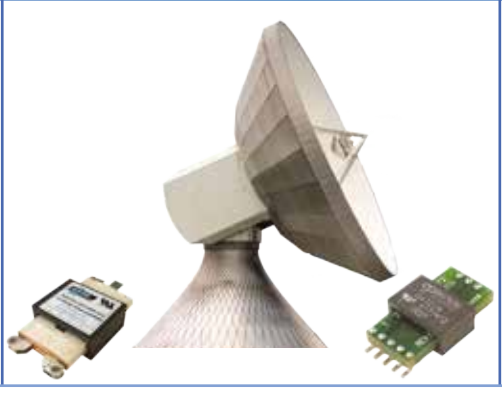	

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Ti - 400V – 12V/500W High Frequency Resonant Converter Reference Design Using High Voltage GaN Devices

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Fig. 1: Regulatory bodies governing radio operation in Europe.

European standard	Equipment and frequency ranges covered by the standard	Test solution
EN 302 571	Intelligent transport systems (ITS), e.g. modules for car-to-car communications 5855 MHz to 5925 MHz	R&S®TS-ITS100 RF conformance test system
EN 300 328	Wideband transmission systems, e.g. WLAN modules 2400 MHz to 2483.5 MHz (ISM band)	R&S®TS8997 regulatory test system for wireless devices
EN 301 893	5 GHz high performance RLAN, e.g. WLAN modules 5.15 GHz to 5.35 GHz and 5.47 GHz to 5.725 GHz	R&S®TS8997 regulatory test system for wireless devices
EN 301 908-13	IMT cellular networks, e.g. LTE user equipment E-UTRA frequency bands 1, 3, 7, 8, 20, 33, 34, 38, 40, 42, 43	R&S®TS8980 RF test system family
EN 303 340	Digital terrestrial TV broadcast receivers; harmonized standard covering the essential requirements of article 3.2 of Directive 2014/53/EU	R&S®BTC broadcast test center

Fig. 2: Important examples of radio standards defining the technical details for compliance with the RED.

The new directive also covers receivers According to the Official Journal of the European Union L 153/62 of May 22, 2014, the previous directive RTTED 1999/5/EC, better known as R&TTE, has been replaced by the new radio equipment directive RED 2014/53/EU published on April 16, 2014. Replacement took effect on June 13, 2016, with an additional transition period of one year, subject to approval by the national legislative and regulatory bodies.

Technical aspects are essentially covered by Article 3.2, both in the previous and the new directive. In the previous directive, this article stipulated that a radio should only use the allowed frequency bands while avoiding interference with other bands. To fulfill these requirements, the transmitter section of a radio had to meet specified technical standards. Radio receiver sections and mere radio receivers (RX-only products) had always been exempt from the regulation.

The new RED adds an inconspicuous but crucial requirement to Article 3.2. Radios must make efficient use of the available spectrum. This is a consequence of the growing economic importance of radio resources. The directive now explicitly covers the receiver sections of radio equipment as well as mere radio receivers, and requires that they achieve a minimum level of performance in terms of sensitivity and selectivity, which must be demonstrated by appropriate measurements.

ETSI Recommendation EG 201 399 lists the typical radio transmitter and receiver parameters to be tested.

Transmitters
(in line with previous (R&TTE) and new (RED) directive)

- Frequency accuracy and stability
- Transmit power
- Adjacent-channel power
- Spurious emissions
- Intermodulation attenuation
- Transient behavior
- Modulation accuracy
- Duty cycle

Receivers
(in line with new directive (RED))

- Dynamic range and sensitivity
- Co-channel rejection
- Adjacent-channel selectivity
- Spurious response rejection
- Intermodulation response rejection
- Blocking / desensitization
- Spurious emissions
- Multipath sensitivity

Fig. 3: Essential requirements on radio transmitters and receivers in accordance with ETSI EG 201 399, and the associated parameters

Fig. 3 shows a selection of these parameters.

Summary

The new European radio equipment directive raises the demands on radio equipment of all types, calling for higher spectral efficiency. This means that from mid-2016, radio receivers will also have to meet regulatory minimum performance requirements, and consequently will have to be tested. Rohde & Schwarz offers all the necessary T&M equipment, both as lab instruments and as fully automatic, complete turnkey solutions tailored to provide the tests for a given regulatory scenario.

Minimizing Impedance Mismatches with Fixed Attenuators

Mini Circuits

Fixed attenuators are invaluable problem-solvers for circuit-level and system-level designers. In addition to controlling amplitude levels, fixed attenuators can improve the impedance match between impedance-sensitive devices such as amplifiers and filters, and provide the isolation needed to stabilize oscillators.

Unfortunately, not all RF components and transmission lines are created equal. Although most components are nominally specified at 50Ω (and, in the case of cable-television or CATV systems, 75Ω), their impedances are comprised of complex, reactive elements which can add and subtract under different phase conditions. Under ideal conditions, when a load is perfectly matched to a source, maximum power available from that source is transferred to the load. Under these ideal conditions, there are no reflections, and the reflection coefficient is zero. But when the operating conditions are less than ideal (as in all real-world applications), not all of the source power is absorbed by the load; the remaining power is reflected back to the source. When the load is an open or short circuit, all of the power is reflected back to the source, and the reflected voltage is the same as the forward voltage, resulting in a reflection coefficient of unity. In simple terms, when the load impedance of a device differs from the characteristic impedance of a system or other device, the voltage between the two units will fluctuate.

The reflection coefficient can be expressed in terms of the load impedance and the characteristic impedance as:

$$\rho = (Zload - Z0)/(Zload + Z0)$$

The ratio of the peak voltage to the minimum voltage, which is known as the voltage standing wave ratio (VSWR), can be expressed in terms of the load and characteristic impedances as:

$$VSWR = [1 + |(Zload - Z0)/(Zload + Z0)|]/[1 - |(Zload - Z0)/(Zload + Z0)|]$$

The VSWR is a figure of merit for impedance match (or mismatch). In an attenuator, it is a measure of the deviation from 50Ω or 75Ω of the component's input and output impedances. A perfect match is represented by a VSWR of 1.0:1, while a worse-case mismatch is represented by an infinite VSWR of ∞ : 1. A VSWR that is slightly higher than 1.0:1 represents a slight mismatch from the ideal match, and is generally the goal sought by adding attenuators to a multiple component design or test system.

A fixed attenuator can help to lower the VSWR of cascaded (connected) components by providing isolation between the impedances, effectively masking the impedance mismatches. It is important to note that in a receiver, an attenuator will also play a part in the system noise figure, since the unit's attenuation value can also be thought of as its noise figure. For example, a 3-dB fixed attenuator

TABLE 1

The effects of mismatches on maximum VSWR.

VSWR 1	VSWR 2	VSWR max	Return Loss	Insertion loss	Uncertainty
			dB	Plus dB	Minus dB
1	1	1		0	0
1.01	1	1.01	46.06	0	0
1.1	1.1	1.21	20.44	0.02	0.02
1.15	1.15	1.32	17.15	0.042	0.042
1.2	1.2	1.44	14.88	0.071	0.072
1.25	1.25	1.56	13.17	0.107	0.108
1.5	1.25	1.88	10.33	0.191	0.195
1.5	1.5	2.25	8.3	0.341	0.355
1.75	1.5	2.63	6.97	0.461	0.487
1.75	1.75	3.06	5.89	0.623	0.671
2	1.25	2.5	7.36	0.316	0.328
2	1.5	3	6.02	0.561	0.599
2	1.5	3.5	5.11	0.756	0.828
2	1.75	4	4.44	0.915	1.023
2.5	1.25	3.13	5.76	0.404	0.424
2.5	1.5	3.75	4.75	0.714	0.778
2.5	1.75	4.38	4.04	0.96	1.08
2.5	2	5	3.52	1.16	1.339
2.5	2.5	6.25	2.8	1.465	1.763
3	1.5	4.5	3.93	0.828	0.915
3	2	6	2.92	1.339	1.584
3	2.5	7.5	2.33	1.686	2.095
3	3	9	1.94	1.938	2.499

***Table 1 was created with a handy Windows-based program called VSWR Calculator, detailed by author Steve Hageman of Agilent Technologies (Santa Rosa, CA) in his article, "Program predicts VSWR-mismatch RF uncertainties," appearing in the February 1, 2001 issue of EDN.**

that is inserted prior to a low-noise amplifier (LNA) in a receiver front end will effectively set the noise figure of the receiver to a minimum of 3 dB. The cascaded effects of the noise figures and losses of the components following the attenuator, including the LNA, will increase the noise figure considerably beyond 3 dB, however.

Similarly, the use of attenuators in a test system with a spectrum analyzer, for example, will affect the test-system dynamic range. Since the dynamic range is essentially the difference between the highest-level signal and the minimum discernible signal, the dynamic range will decrease by an amount equal to the total attenuation added.

In test setups, even minimal-valued attenuators, such as 1-dB units, can aid in minimizing mismatch errors. The choice of attenuator depends on the sensitivity of the measurement equipment, the type of device under test (DUT), and the maximum allowable signal level to the test equipment. If an active device, such as an amplifier, is under test, with a rated output level of +27 dBm, but the maximum input rating of the spectrum analyzer is +25 dBm, an attenuator with rating of 5 dB or more will provide adequate protection for the analyzer while also serving to minimize mismatch uncertainty. Of course, based on the attenuation flatness of the device, it may be possible to specify a lower-valued attenuator, provided that its variations in attenuation (attenuation flatness) are within acceptable limits. In this case, a 4-dB attenuator with better than ±1 dB attenuation flatness (which means that its attenuation ranged from 3 to 5 dB) would still provide adequate protection for the spectrum analyzer's input mixer.

Several lines of surface-mount and coaxial fixed attenuators are available from Mini-Circuits at attenuation values from 1 to 40 dB and for frequencies from DC to 40 GHz. These attenuators are available for both 50Ω and 75Ω systems, with attenuation flatness ranging from ±0.2 dB for lower-valued attenuators to a still modest ±0.6 dB for 40-dB attenuators. Minimum and maximum VSWRs are given for all units to help anticipate the effects of a particular attenuator (beyond the basic signal attenuation) on a communications or test system.

When attempting to determine the total VSWR created by the connection of two components, it is generally safe to assume that two VSWRs will tend to multiply rather than add. For example, when connecting a component with a VSWR of 3.0:1 to a second component with a VSWR of 1.50:1, the resulting maximum VSWR will be 4.50:1, with a corresponding return loss of 3.93 dB. Because of this, the effects of mismatch can be minimized by selecting an attenuator with the lowest possible VSWR. Table 1 shows the effects of combining two components in terms of their maximum VSWR and return loss. The ideal condition, where both VSWRs are 1.0:1 and there are no reflections, results in infinite return loss. But as the VSWR for each component increases, the maximum VSWR increases as the product of the two individual VSWRs.

5G THE MICROWAVE PERSPECTIVE

› Thomas Cameron, Analog Devices Inc.

With 5G rising on the horizon, it's an exciting time to be an RF engineer. As we embark on the road to 5G, the next-generation wireless communications system, there are countless challenges and opportunities emerging for the engineering community. 5G represents both an evolution and a revolution of mobile technologies that reaches the various high level goals that have been published to date by various members of the wireless ecosystem.

5G is widely seen as the generation of wireless that will enable cellular to expand into a completely new set of use, case, and vertical markets. While 5G is generally seen in technology that delivers ultrabroadband services, including HD and ultraHD video streaming, 5G technology will also enable cellular to enter the world of machines. It will contribute to autonomous vehicles and be used to connect millions of industrial sensors and a multitude of wearable consumer devices, to name a few applications.

The evolutionary path to 5G consists of incremental enhancements of 4G in the conventional cellular bands and extending up in frequency to emerging bands in the 3 GHz to 6 GHz range. Massive MIMO has industry momentum and will evolve from first systems based on LTE to adopt new waveforms designed to improve throughput, latency, and cell efficiency.

Spectrum is seen as the lifeblood of the cellular industry and the spectrum in the legacy cellular bands (sub-6 GHz) just cannot support the exponentially growing demand in upcoming years. As such, the bands above 6 GHz are currently under study to test the viability of deploying wireless access in frequency allocations above 6 GHz. While the collective global spectrum available below 6 GHz is on the order of hundreds of MHz, the amount of potential spectrum above 20 GHz is in the tens of GHz. The taming of this spectrum is considered essential to achieve the 5G vision of a truly connected world.

As a result, a segment of 5G is likely to operate on much higher frequencies (possibly up to millimeter waves) and will likely adopt new air interface technologies that are not backward compatible to LTE.

The frequency bands discussed among key industry players include higher frequency bands such as 10 GHz, 28 GHz, 32 GHz, 43 GHz, 46 GHz to 50 GHz, 56 GHz to 76 GHz, and 81 GHz to 86 GHz. However, these bands are currently in the proposal stages and much work remains to be completed in channel modeling prior to the radio systems definitions and standards deliberations.

The ITU recently published a plan for 5G standardization with a target to

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CBL	All-purpose workhorse cables for highly-reliable, precision 50Ω measurement through 18 GHz	DC-18	SMA, N
APC	Crush resistant armored cable construction for production floors where heavy machinery is used	DC-18	N
ULC	Ultra-flexible construction, highly popular for lab and production test where tight bends are needed	DC-18	SMA
FLC	Flexible construction and wideband coverage for point to point radios, SatCom Systems through K-Band, and more!	DC-26	SMA
NEW! VNAC	Precision VNA cables for test and measurement equipment through 40 GHz	DC-40	2.92mm (M to F)

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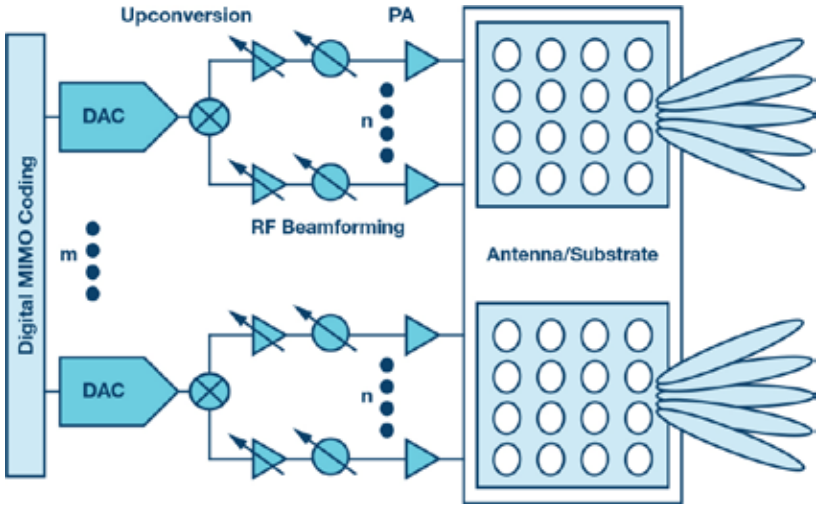


Figure 1. Block diagram of hybrid beamforming transmitter.

publish the first generation of IMT-2020 specifications around year 2020.

Given that the 5G is still in its infancy, much work needs to be completed in the channel modeling, radio architecture definition, and finally chipset development before the first commercial systems will be deployed.

However, there are certain trends and requirements already agreed upon and problems to be solved that will lead to the final 5G systems.

Let's consider 5G access systems at microwave and millimeter wave frequencies. One of the major hurdles in implementing radio access at microwave frequency is overcoming the unfavorable propagation characteristics. Radio propagation at these frequencies is highly affected by atmospheric attenuation, rain, blockage (buildings, people, foliage), and reflections. Microwave point-to-point links have been deployed for many years but these are generally line of sight systems. The fact that they are stationary makes the link manageable, and the systems have been developed in recent years, which support very high throughput using high order modulation schemes. This technology continues to evolve and we will leverage the microwave link technologies into 5G access.

Early in the cycle, it has been acknowledged that adaptive beamforming will be required to overcome the propagation challenges for access systems.

Unlike point-to-point systems, the beamforming will need to adapt to the users and the environment to deliver the payload to the user. It is generally agreed in the industry that hybrid MIMO systems will be used in the microwave and low millimeter wave bands, while in V bands and E bands - where bandwidth is plentiful - the systems will likely only employ beamforming to reach the required throughput goals.

The diagram in Figure 1 depicts a high level block diagram of the hybrid beamforming transmitter. The receiver can be envisioned as the reverse. The MIMO coding is performed in the digital section along with the typical digital radio processing. There may be a multitude of MIMO paths processed in the digital section from the various data streams feeding the antenna system. For each data stream, the DAC converts the signal into analog at either a baseband or IF frequency depending on the selected architecture. The signal is upconverted and split into the constituent RF paths to feed individual antennae. In each RF path, the signal is processed to set the gain and phase to form the beam out of the antenna.

While the block diagram is simplistic, the system challenges and tradeoffs are complex. In this short treatment of the topic only a few issues will be discussed, but let's focus on the architecture and radio challenges. It is critical to design this system with power, size, and cost in mind from the start to bring these systems to reality.

While such radios can and are being built today for prototype 5G systems using discrete (mainly GaAs) devices from Analog Devices and our peers, we need to bring the same high levels of integration to bear in the microwave space as what has been implemented in cellular radios.

High integration and high performance make a tough problem for the industry to solve.

But integration alone is not the solution to this problem facing the industry.

It needs to be smart integration. When we think of integration, we need to first consider architecture and partition to leverage the benefits of integration. In this case mechanical and thermal design also need to be considered as the circuit layout and substrate are interrelated.

First of all, an architecture conducive to integration needs to be defined. If we consider the examples of highly integrated transceiver ICs for cellular base stations, many use a zero IF (ZIF) architecture to either eliminate or minimize the filtering in the signal path. Particularly at microwave frequency, one must minimize the loss in the RF filters, as RF power is expensive to generate. While ZIF will reduce the filter issue, of course the trade-off is LO suppression, but we shift the

problem from physical structures to signal processing and algorithms. Here we can leverage Moore's law, whereby passive microwave structures do not follow the same scaling dynamics. It is necessary to take advantage of the ability to optimize analog and digital simultaneously to reach our goals. There are many algorithms and circuit techniques that have been employed at cellular frequency that may bring benefits to the microwave space.

Next, consider the semiconductor technology requirements. As mentioned above, state-of-the-art microwave systems are generally implemented with GaAs components. GaAs has been the mainstay of the microwave industry for many years, but SiGe processes are overcoming the barriers of high frequency operation to rival GaAs in many of the signal path functions. High performance microwave SiGe Bi CMOS processes enable a high level of integration required for these beamforming systems encompassing much of the signal chain as well as auxiliary control functions.

GaAs PAs may be required, depending on the output power required at each antenna. However, even GaAs PAs are inefficient at microwave frequency as they are generally biased in the linear region. Linearization of microwave PAs is an area ripe for exploration in the 5G era, more than ever before.

What about CMOS? Is it also a contender? It is well documented that CMOS is suited for high volume scaling and this is being proven out in WiGig systems at 60 GHz. Given the early stage of development and uncertainty of the use cases, it is difficult to say at this point if or when CMOS will be a technology choice for the 5G radios. Much work needs to be done first in the channel modeling and use cases to conclude the radio specifications and where microwave CMOS may fit in future systems.

The final consideration in the 5G systems is the interdependency of the mechanical design and RF IC partitioning. Given the challenges to minimizing losses, the IC needs to be designed with the antenna and substrate in mind to optimize the partition. Below 50 GHz, the antenna will be part of the substrate and it is expected that the routing and some passive structures may be embedded in the substrate. There is a body of research ongoing in the area of substrate integrated waveguides (SIW) that looks promising for such integrated structures. In such a structure it will be possible to mount much of the RF circuitry on one side of the multilayer laminate and route to the antennae on the front face. The RF ICs may be mounted in die form on this laminate or in surface-mount packages. There are good examples in the industry literature of such structures for other applications.

Above 50 GHz, the antenna elements and spacing become small enough that it is possible to integrate the antenna structure in or on the package. Again, oing research that may push 5G systems forward.

In either case, the RF IC and mechanical structure must be codesigned to ensure symmetry in routing and to minimize losses. None of this work will be possible without powerful 3D modeling tools for the extensive simulations required for these designs.

While this is a brief perspective on the challenges 5G brings to the microwave industry, there are boundless opportunities to bring forth RF innovations in the coming years. As mentioned previously, a rigorous systems engineering approach will yield the optimum solution by leveraging the best technologies throughout the signal chain. There is much work to be done as an industry from processes and materials develop to design techniques and modeling, to high frequency test and manufacturing. All disciplines have a role to play in reaching the 5G goals. Analog Devices brings a strong contribution to the 5G microwave effort with our unique bits to microwave capability. Our broad technology portfolio and continued RF technology advances combined with our rich history in radio systems engineering put ADI in a leading position to pioneer new solutions for our customers at microwave and millimeter wave frequencies for the emerging 5G systems.

As mentioned in the beginning of the article, it is an exciting time to be an RF engineer in the wireless industry. 5G is just starting and there is much work ahead of us to realize commercial 5G radio networks by 2020.

About the Author

Dr. Thomas Cameron is the CTO for the Communications Business Unit at Analog Devices. In this role he contributes to industryleading innovation in integrated circuits for radio base stations and microwave backhaul systems. He is currently working on research and development of radio technology for 5G systems in both cellular and microwave frequency bands. Prior to his current role at Analog Devices he was Director of Systems Engineering for the Communications Business.

Dr. Cameron has over 30 years of experience in research and development of technology for telecom networks including cellular base stations, microwave radios, and cable systems. Prior to joining Analog Devices in 2006, he had worked on developing numerous RF circuits and systems over his career at Bell Northern Research, Nortel, Sirenza Microdevices, and WJ Communications.

Dr. Cameron holds a Ph.D. in electrical engineering from the Georgia Institute of Technology.

Contactless Connectivity Unshackles Robotic Systems

Industrial manufacturing and production may be the first to benefit from a new way of thinking about connections

› Benjamin Mang, TE Connectivity & Rich Miron, Digi-Key

Post burn-in, connectors are a major point of failure of an electronic system due to mechanical and environmental stresses, and in some cases, poor design. This becomes increasingly significant as electronics, particularly robotics, permeate industrial and manufacturing applications where maximum flexibility must be combined with minimum downtime.

To meet and overcome these dual challenges, designers need to understand the function and failure modes of connectors and match the right connector to the application. Factors to be considered include environmental, functional, and mechanical stress requirements. All conditions and usage models need to be considered before making a final connector choice.

While it's important to understand the fundamentals to ensure longevity, it's just as important to look for and review the latest advances in connector technology to help achieve the optimum balance of performance, reliability, flexibility and cost.

What exactly is a connector?

This question can be answered in two ways, functionally and structurally. Functionally, a connector provides a separable connection between two elements of an electronic system without unacceptable signal distortion or power loss. There are two important parts to this definition, the "separable connection" and the "unacceptable" performance. Both depend on the connector application and its electrical and environmental requirements.

The separable connection is the reason for using a connector in the first place, to provide easy repair, upgrading, maintenance or interconnectability. Requirements on the separable interface include mating-force limitations and meeting a specified number of mating cycles.

"Unacceptable" performance includes a large range of characteristics, but this discussion will concentrate on the limitations the connector introduces into the electronic system. The traditional approach is to use a standard, full-contact wired power and signal connector. There are many advantages and disadvantages to this approach.

As mentioned, a separable connection provides a separate connection between two elements of an electronic system without unacceptable degradation of performance. The separable connection and unacceptable performance depend on the connector application and its electrical and environmental application. Factors to consider when choosing a connector include:

- Power distribution: Joule heating, which is proportional to the connector resistance, can result in increases in the connector operating temperature, a major factor in connector degradation. Both magnitude and stability of contact resistance are

Data Link	Pro	Challenges
Capacitive coupling	Low EMI. Also suitable for ring structures	Requires significant plate area, challenging for tiny rotating couplers, sensitive to changes of material/ fluids
RF, 60 GHz (OOK, ASK, QAM)	Large bandwidth (>1Gbps), low latency (nanoseconds)	Should generate a circular polarized wave to support rotation
RF, 2.4/5 GHz (e.g. GFSK, MSK, ASK)	Easy near field antenna design (simple loop), RF solutions widely available	No high bandwidth without OFDM, but that increases latency
RF, sub GHz (e.g. FSK)	Easy near field antenna design (simple loop), RF solutions widely available	Low bandwidth (sub Mbps)
Via ICPT power link	No separate antenna needed	Low bandwidth (10-100kbps)
Optical	Very high bandwidth possible (>10Gbps)	Sensitive to dust and dirt, precision optics & lenses needed

Figure 1. There are numerous options for a contactless data link, including 2.45-GHz RF, but power links are for now best achieved using inductively coupled power transfer

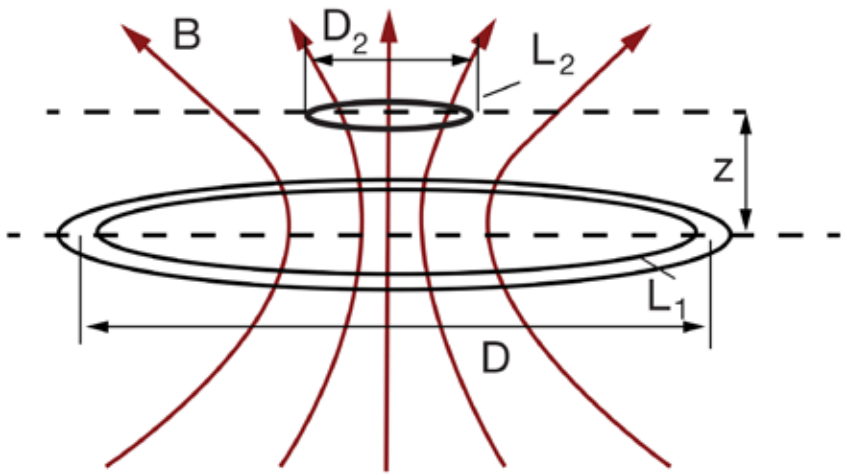


Figure 2. In inductive coupling, the coupling is determined by the distance (z) and the ratio of D2/D, while the efficiency of power transfer between transmitting coil L1 and receiver coil L2 depends on the coupling (k) between the inductors and their Q factor

critical for power connectivity. Arcing is also significant in power applications, especially where there are hazardous gas environments.

- Signal distribution: Signal distribution requirements center around maintaining the integrity of the signal waveform. For high-data-rate systems, this may involve controlled-impedance connector designs and careful attention to signal-to-noise ratios. The magnitude of the required connector resistance is strongly dependent upon the devices in the circuitry the connector must interconnect. For many devices, high connector resistance - hundreds of milliohms - can be tolerated.
- Environmental considerations: Harsh environments, such as deep ocean or vibration sensitive surroundings, may constrain the traditional connector application and design. There may also be harsh and safety-critical applications, such as gaseous environments, which limit the application of contact technology.
- Corrosion: Corrosion occurs in many forms and can be classified by the cause of the chemical deterioration of a metal. The most common form of corrosion is rust or ferric oxide. Galvanic corrosion, or dissimilar metal corrosion, occurs when two different metals are located together in a corrosive electrolyte.
- Movement: Cabled solutions are generally constrained in their movements. Wear and tear on cables coupled to motor-driven, rotating subsystems, such as robotic arms, can lead to downtime, severely affecting productivity. A classic example is a robotic arm, which may have to move along multiple axii.

Traditionally, rotation with reliable connectivity is achieved using slip rings that are connected to stationary rings via brushes. Cables are used to position these copper rings in close proximity to enable physical contact with carbon brushes.

- Mating cycles: The connector may be designed to meet specified mating frequency and cycles from a few hundred to thousands. Cycle-life requirements affect the design and

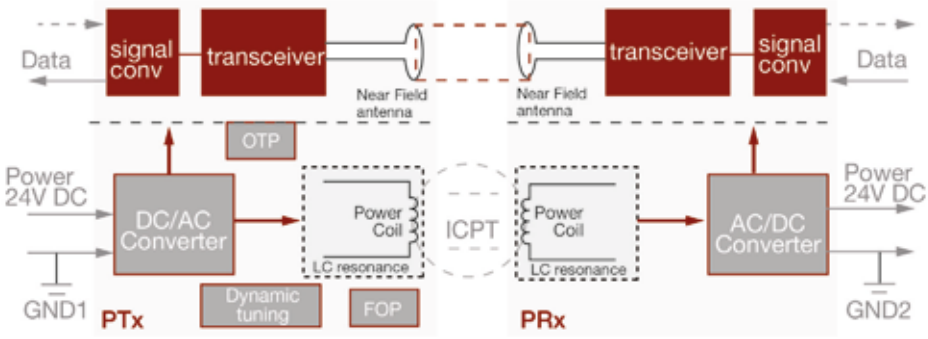
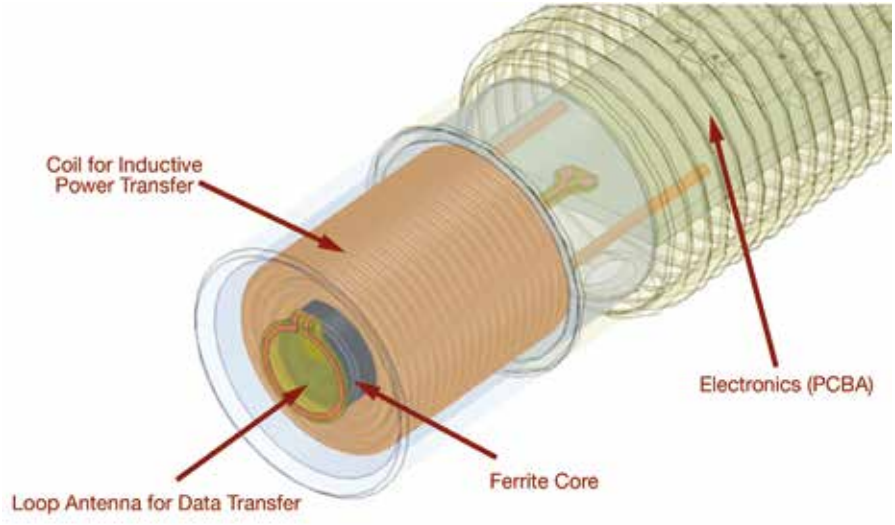


Figure 3. A complete contactless connectivity design integrates ICPT for power transfer and 2.45-GHz wireless for data transmission, all within an M30-type form factor. [Image courtesy of TE Connectivity]



4. Implemented in an M30-type connector, the near-field loop antenna design for a contactless connectivity-based data link is symmetrical to allow for rotation. [Image courtesy of TE Connectivity]

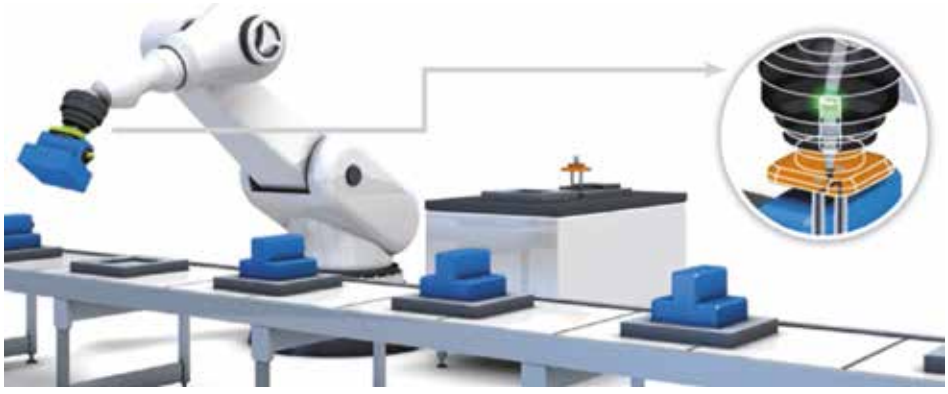


Figure 5. A contactless connectivity option implemented on a robotic arm allows 360 degrees of freedom with no brush wear typical of current slip-ring designs. Integrated sensors also enable "gentle touch" sensitivity. [Image courtesy of TE Connectivity]

materials used in manufacturing the connector.

- Other factors: Cost, size, efficiency and the ability to transmit over certain distances may also be design criteria that need to be considered for each application.

The ability to transmit over "certain distances" as mentioned above is particularly interesting. There are instances where power and data need to be transferred wirelessly across small distances, such as through a wall or other material. Also, more connector freedom may be needed without mechanical wear and tear, or the environment may be too hazardous to introduce any possibility of arcing.

It's at this point that advances in contactless connectivity need to be considered.

Contactless connectivity

"Contactless connectivity requires both contactless power and contactless data technology which can easily connect over a short distance without physical contact" [TE Connectivity (TE)].

There are many benefits to be accrued from contactless over traditional connectors which should be considered when deciding how to meet the design specification most effectively. These include:

- Improved reliability: Delivers robust power and data without wires or physical contact. Also, the connectors are hermetically sealed ensuring environmental integrity.
- Greater flexibility: There is an unlimited range of motion, allowing 360° movement, tilt, angle and misalignment.
- Unlimited mating cycles: There are unlimited mating cycles in wet and dusty environments. This is particularly suitable where slip rings or spring cables reach their limit.
- Connection through walls or materials: Contactless technology allows connection through walls or materials, which is not possible with traditional connectors.

Figure 6: Free from the strictures of contact, contactless interconnects provide greatly improved flexibility and reliability, while magnetic coupling protects against explosions in gaseous or otherwise flammable environments.

- Improved safety: There is no arcing, which is a major plus in hazardous environments such as gas-filled chambers.
- Cost savings: There is no wear and tear thus improving the uptime and reducing maintenance.

However, a truly contactless connector must be able to transmit both data and power. For power, there are few options. Capacitive power transfer (CPT) has the advantage of being able to penetrate (floating) metal and has low EMI, but it suffers from low power density and short range. Some generalized comparisons of various wireless options, using pros and cons, are shown for easy reference (Figure 1.)

For contactless power transfer, an inductively coupled power transfer (ICPT) option proves to have more pros than cons. It is has high power density at reasonable distance, is well known with widely available product and technology solutions, and high efficiency is possible. The downside is that it cannot penetrate metal.

For data transmission, there are a number of options. Capacitive coupling's low EMI is also an advantage for data transfer, but such coupling requires significant surface-plate area, which can be challenging for tiny, rotating couplers. Inductive coupling for data suffers from low bit rates. Other options include RF at 60 GHz, 2.45 or 5 GHz, sub-GHz, and ICPT, as well as optical links. Each has pros and cons, as shown in Figure 1.

The 2.45-GHz industrial, scientific, medical (ISM) band is also unlicensed, with global acceptance and wide usage, most notably as "wireless Ethernet" under the moniker of Wi-Fi.

In the final analysis, it turns out that a hybrid architecture, RF for data and inductive coupling for power, is the best approach for contactless connectivity.

Defining induction

Inductive power transfer has been with us for quite some time, but for the sake of clarity a quick run through of how it works is useful in understanding its utility as a wireless power-transfer mechanism.

Faraday's law of induction states that the induced electromotive force in any closed circuit is equal to the rate of change of the magnetic flux enclosed by the circuit, or mathematically as:

$$\mathcal{E} = -\frac{d\Phi_B}{dt}$$

Where is the electromotive force (EMF) and ΦB is the magnetic flux.

The basic principle of an inductively coupled power-transfer system is shown (Figure 2). It consists of a transmitter coil L1 and a receiver coil L2. Both coils form a system of magnetically coupled inductors. An alternating current in the transmitter coil generates a magnetic field, which induces a voltage in the receiver coil. The efficiency of the power transfer depends on the coupling (k) between the inductors and their quality, defined as their Q factor.

The coupling is determined by the distance between the inductors (z) and the ratio of D2/D. The shape of the coils and the angle between them further determines the effective coupling.

The performance of a wireless power link can be improved using resonant inductive coupling. Resonance of a circuit involving capacitors and inductors occurs because the collapsing magnetic field of the inductor generates an electric current in its windings that charges the capacitor, and then the discharging capacitor provides an electric current that builds the magnetic field in the inductor. This process is repeated continually.

At resonance, the series impedance of the two elements is at a minimum and the parallel impedance is at maximum. Resonance is used for tuning and filtering, because it occurs at a particular frequency for given values of inductance and capacitance.

To cancel the influence of the inductive reactance and the capacitive reactance they should have equal magnitude, ωL = 1/ωC, so:

$$\omega = \frac{1}{\sqrt{LC}}$$

Where L is the inductance in Henrys, C is the capacitance in Farads , and ω = 2πf, in which f is the resonance frequency in Hertz. In low-power systems and for high power efficiency, higher k and Q are required.

Applications of inductive coupling

Taking inductive coupling a step further, the idea of using it to transmit power wirelessly has been around since the mid 19th century. Nikola Tesla initially experimented successfully with the lighting of gas-discharge lamps wirelessly over a distance of approximately 15 feet. This sparked interest in wireless power transfer technology and applications involving microwaves, lasers, and solar cells capable of transmitting power from space.

Closer to home, modern power mats used to charge mobile devices use resonant inductive coupling, but use a "handshake" between the charging surface and the device, and then energy is transferred to the device. It is an intelligent system and will only send power to identified devices and only at a rate determined by the charging profile of the device's battery.

Inductive power transfer is also the operating principle behind passive RFID tags, toothbrushes, and contactless smart cards.

Integrating wireless power and data

The principle challenges with a contactless connector are integrating the power coils and near-field antenna into a very small form factor that is relatively easy to manufacture. This requires knowledge of mechanical design and power electronics, as well as magnetics, RF circuit design and antennas.

The power-transmit portion takes the 24-V DC supply, puts it through a circuit protection section, followed by a DC-DC converter and a DC-AC converter. The converter output feeds the transmit primary coil, which has a capacitor in parallel as part of a resonant tank that allows it handle variable loads and distance. The receiver side also contains a resonant tank. The received power is rectified, put through a DC-DC converter to deliver 24 V DC to the point of load.

The inductive power link itself has an efficiency of approximately 95%, while the output power is always 12 W. The overall system efficiency depends on the data link and includes the losses on the board, e.g. through the DC-DC conversion.

Using this circuit and techniques, an M30-diameter implementation can provide 12 Watts of output power. The effective power over distance is 7 mm (Z) distance for M30. In addition, the coupling is tolerant of misalignment up to 5 mm.

For contactless data transmission, the data is sent separately through a signal converter to a 2.45-GHz transceiver and out to a near-field antenna (Figure 3). On the receive side, the process is reversed.

The first variant is designed for sensor applications and supports up to eight PNP channels, unidirectionally from receiver to transmitter, with a switching frequency of 500 Hz (maximum). Development of higher data rates is on going, with a goal of supporting industrial Ethernet at 100 Mbits/s.

The data connection happens upon physical connection, and is by necessity dynamic, occurring without user interaction. The range is short, up to a couple of millimeters, which is good for security and RF emissions purposes. The connector can accommodate up to eight digital PNP channels, with the current variant.

To enhance reliability, the data link uses redundancy in the 2.4-GHz channel, has minimal far-field interference and the antenna design is symmetrical to allow for rotation (Figure 4). It's also tolerant of misalignment, rotation and tilt.

The full system efficiency, meaning the efficiency of the power and data link together, is ~ >75% (output power of receiver end/input power to the transmitter). Of course, this depends on the load, the distance and other factors, but it also includes the losses through the data link and PC-board assemblies.

In rugged or dangerous environments, connectors are hermetically sealed to IP67, even if they are not connected with each other.

Unleash the robots

The challenge of integrating contactless data and power translates to relatively high cost, so the target applications are those where the capabilities of classic connectors have reached their limit in terms of mating cycles or environmental conditions, or where the application requires complex harness construction, and especially for new applications, such as connecting through walls and materials, or connections on the fly.

One such application is robotic systems, which are being increasingly adapted to manufacturing and production processes that require greater complexity and precision. Given the rigors of the environment and the cost of downtime, maximizing reliability through dependable connectivity can pay dividends in the long term.

In a typical robotic application, cables limit the range of motion and the constant movement and friction of the mechanical parts also creates wear and tear. Robots also need to move rotationally to perform complex tasks. Traditionally, rotation is enabled with rotating connectors, spring cables, or slip rings, the latter of which are mechanically connected to stationary rings via brushes. Cables are used to position these copper rings in close proximity to enable physical contact with the carbon or metal brushes. The brushes then transfer the electrical current to the ring, creating rotation.

This constant friction creates wear and tear on the moving contacts, slip rings and brushes, which must be replaced frequently. This results in increased downtime and reduced productivity.

With contactless connectors, the deterioration of moving components is no longer a limiting factor (Figure 5.)

Issues typically affecting connectivity

in harsh environments, such as water, dust or vibrations, no longer impact the reliable delivery of power, data and signals. Contactless connectivity can replace complex and expensive harness constructions and slip rings, enabling connectivity where you could not connect before. The ability to integrate sensors within the robotic graspers or "fingertips" for force feedback to the system also enables "gentle touch" sensitivity for delicate items.

Data to date shows that the total cost of ownership (TCO) using contactless connectors versus traditional solutions is positive within the first few months through increased efficiency, reduced downtime, maintenance savings and increased output.

It may be the case that contactless connectivity will provide designers with an entirely new way of thinking about mechanically designed machines.

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My Inventions: Nikola Tesla's Autobiography
Nikola Tesla

TE Connectivity

*Definition and Benefits of Contactless Connectivity

For factory and industrial environments where dust, liquids, and gases combine with friction, power and robotic system wear and tear through multiple axii of rotation, designers need a new approach to connectivity. This new approach needs to be able to overcome these many environmental and operational challenges to secure, reliable, flexible, and robust connectivity – for both power and data.

The solution lies in a new interconnection system, based on both contactless power and contactless data technology, which can easily connect (and disconnect) over a short distance without using any mechanical contact, demonstrated in the ARISO connectors from TE Connectivity.

To date, contactless, or wireless, data has come in many forms, from cellular to Wi-Fi, Bluetooth and ZigBee; however, for low-data-rate sensor data, these interfaces have a lot of packet-processing and network-interface and mesh networking overhead. This costs the designer, both in terms of real estate and power consumption, as well as direct component costs.

For its part, wireless power has undergone a revolution of late, thanks to the efforts of groups such as the Wireless Power Consortium, pushing Qi, as well as the now merged Alliance For Wireless Power and Power Matters Alliance. These have developed standards for the transmission of power levels of up to 5 W, with a usable range of up to 30 mm, to charge mobile devices, particularly handsets. The standards use variations of inductive and resonant power at various frequencies to achieve this, but all require a relatively large footprint, while also being relatively costly.

The trick is to find the sweet spot in terms of data rates, cost and power consumption for wireless data, and in terms of range and cost for wireless power, such that both interfaces can fit within the confines of a typical M30- or M12-type sensor head.

Thanks to the work that been done to date in terms of RF function integration to lower cost, as well as increases in the efficiency of wireless power transmission, this sweet spot is attainable by matching the wireless data and power transmission circuits to the application's low power and short range requirements.

For data, the 2.45-GHz unlicensed band was chosen as it can be implemented using a near-field antenna design with a simple loop

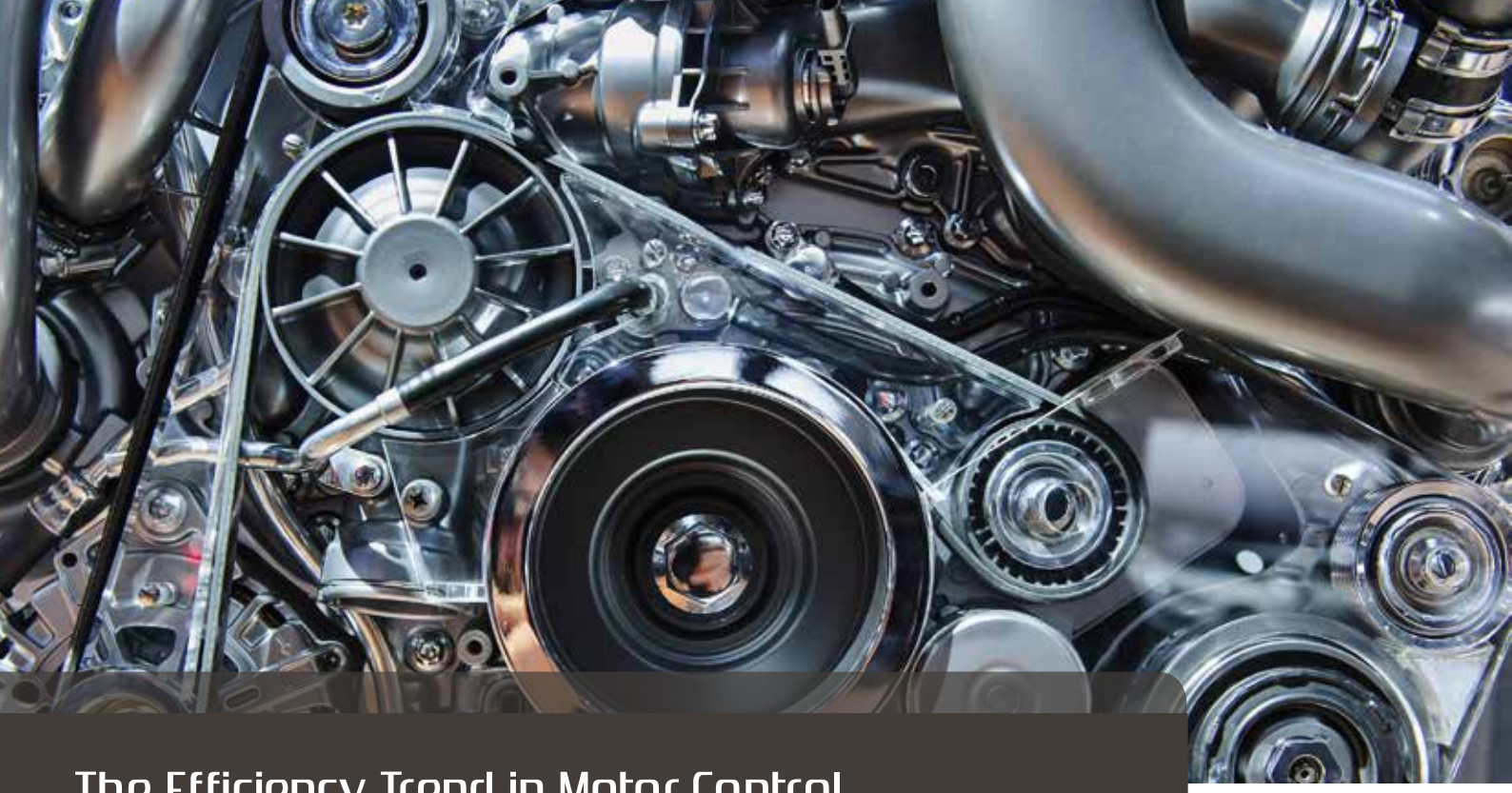
For power, the principle challenges are integrating the power coils and near-field antenna into a very small form factor that is relatively easy to manufacture. This requires knowledge of mechanical design and power electronics, as well as magnetics, RF circuit design and antennas.

With both the data and power transmission now integrated into a single connector head, the options and application dynamics change, dramatically. Flexibility jumps to a higher level, with 360° rotation without cable, connector, or harness wear and tear. This freedom of movement also allows for connector tilt, angle or misalignment, while the rotational freedom enables faster maintenance-free rotation as well as faster return to starting points, as the rotating heads don't have to rotate back through 180° offset, but instead can keep going to 360°.

Contactless connectors are vibration resistant and are hermetically sealed against harsh environments and have unlimited mating cycles, despite wet & dusty environments. The magnetic coupling is particularly attractive in gaseous applications or where flammable liquids or material are present.

Other advantages include easy on-the-fly connection without the traditional mechanical limitations, design flexibility and cost savings by enabling the transfer of power and signal through fluids and walls, as well as improved reliability for reduced maintenance & lower total cost of ownership.

For more information about the ARSIO range of products from TE, visit the company's site.



The Efficiency Trend in Motor Control

› Erlendur Kristjansson, Microchip Technology Inc.

Introduction

Efficiency is the Holy Grail in all electric motor- based applications. If we look at the different applications that are using electric motors today, we can see the trend of continued improvement for higher efficiency and lower cost. For example, in cars, the original approach for driving pumps and fans under the hood was the serpentine belt. However, even though this is a convenient way to utilize the engine rotation to drive these actuators it is not very efficient. Taking these actuators, and driving them with motors adds flexibility and improved efficiency. Another example is washing machines, where the primary motor type has been AC induction. With the increased requirements for energy efficiency in home appliances and more control of the washing cycle to reduce water usage, the use of permanent magnet synchronous motors in new designs has become dominant.

Of course, this trend has been heavily dependent on the improvement of the semiconductor components needed for the inverter stage and control. In the past, the cost of the motor drive needed for electronic commutation has been a significant factor in limiting the use of synchronous motors in many applications. Today, costs have come down and these motors have become the norm in many applications.

Motor Options

The primary motor types that are being considered today, in most applications where efficiency and dynamic controls are important, are:

- AC Induction Motor (ACIM)
- Brushless DC (BLDC) Motor
- Surface Permanent Magnet Synchronous Motor (PMSM or SPM motor)
- Internal Permanent Magnet Synchronous Motor (IPMSM or IPM motor)
- Switched Reluctance Motor (SRM)
- Synchronous Reluctance Motor (SyncRM)

The efficiency of the various motor types can be ranked as follows, from most to least efficient: IPMSM, PMSM, BLDC, SynchRM, SRM, and ACIM, with same order for power/torque density.

The ACIM is the workhorse of industrial applications, and is the most common motor type in high-wattage applications (>1kW). But, with the increased demand for efficiency, many ACIM installations are being updated with electronic commutation drives for improved

efficiency. In applications where more dynamic control is needed, the use of PMSM makes more sense. Then in some applications, where the cost is critical and factors such as weight-to-torque ratio and robustness are needed, the use of SRMs has been seen. Another classic industrial ACIM application is large HP (>15 HP) compressors. Here SyncRM motors have started to appear, as they have a very similar structure to ACIMs, including the same stator design with a different rotor. However, for the same frame size, you can increase the torque and efficiency, or reduce the frame size.

Then there are the applications where there haven't been any motors, such as under the hood of a car. Here, the electrical motor is being used to replace the mechanical serpentine belt, increasing efficiency, as the load can come and go with motors, while with the belt it is always there even though it isn't needed. These days, everything counts when it comes to efficiency and fuel economy. Here the trend has been to move from belt to BLDC motor to PMSM. Another application in cars that is utilizing electric motors is drive by wire. Here, for example, SRMs are being used to drive the hydraulic pumps in the brakes. The high-speed capability of the SRM can build up pressure quickly, to allow for fast break response.

Another very different application space where the use of electrically commutated motors has had a big impact is battery-operated tools and appliances. With the improvements in battery technologies, such as lithium-ion, we can now have vacuum cleaners and power tools utilizing the efficiency of BLDC motors. Initially, these applications primarily used brushed DC motors, but there was a limitation on speed and torque. The higher power/torque density of BLDC motors allows for reasonable weight, longevity and performance that is close to matching the wired version.

Figure 1: Electric Motors for Improved Fuel Efficiency

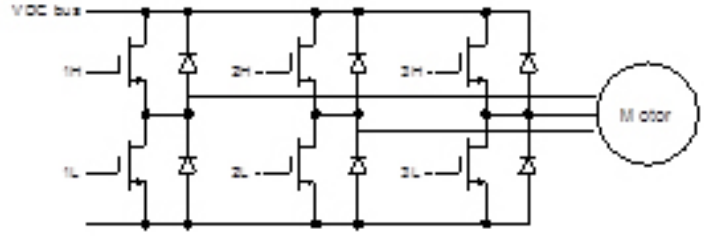


Figure 2a: Synchronous motor drive circuit

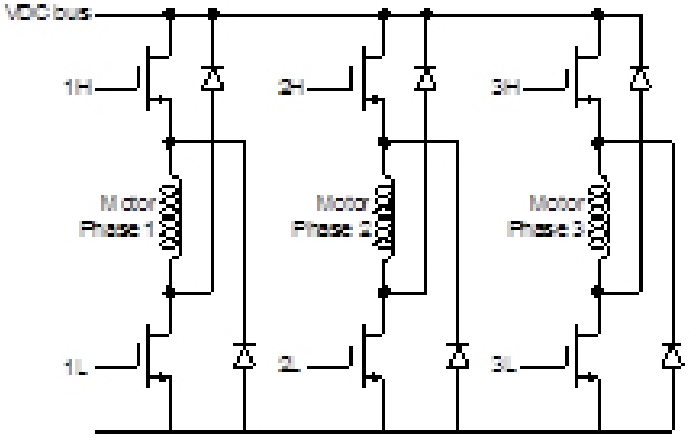


Figure 2b: SRM Drive Circuit

In home appliances, such as washing machines, refrigerators, dishwashers, air conditioners, etc., the primary workhorse, just as in the industrial space, has been the

ACIM. Since the new millennium, the brushless synchronous motors, primarily BLDC motors and PMSMs, have become more and more important. The primary reason has to do with governmental efficiency requirements. The problem with this transition away from ACIMs in the consumer product space has always been the cost, both for the motor and the drive circuit. Fortunately, the cost for both has come down significantly to allow the majority of new appliances to utilize the more efficient technology.

Drive Technology

As mentioned earlier, the drive circuit is an important part when using electronically commutated motors, and is actually mandatory. Without it, nothing happens. For nearly all the motors that we are talking about, the drive circuit has a very similar structure (Figure 2a). The odd man out is SRM (Figure 2b). The biggest difference between these motor types is in the controls; i.e., how the drive signal is created for the circuits in Figure 2. This has to do with how each motor is constructed, resulting in different electromagnetic behaviors. This has to be considered when generating the voltage/current waveforms for the motor, so it operates optimally/efficiently.

During the early days of the transition over to electronically commutated motors, many of the targeted applications were very cost sensitive and, as a result, the BLDC motor was selected because it could be controlled with an 8-bit microcontroller using trapezoidal commutation. Even so, the cost in some cases was still too high. Fast forward 15 years, and the costs of high-performance digital signal controllers and microcontrollers have come down enough to allow cost-sensitive applications to use more advanced control algorithms, such as sensorless Field Oriented Control (FOC). For example, this is emphasized in circulation pumps for home heating systems or cooling fans for automobiles (Figure 3).

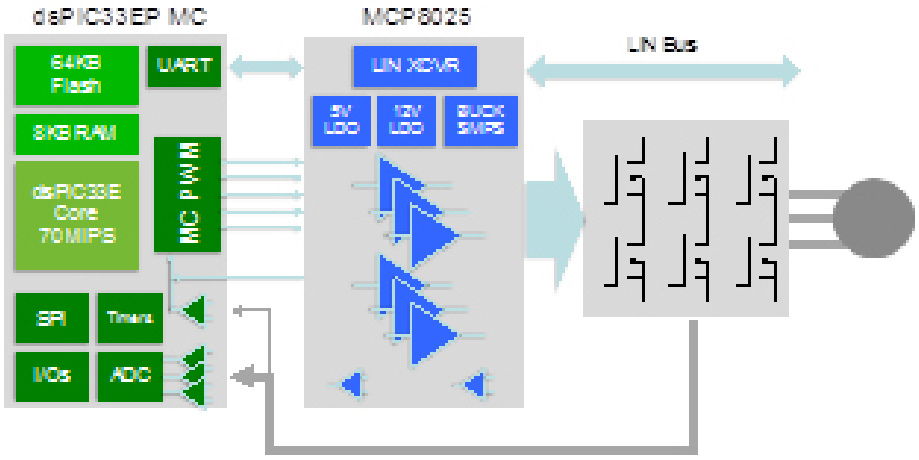


Figure 3: Automotive Cooling Fan Implementation

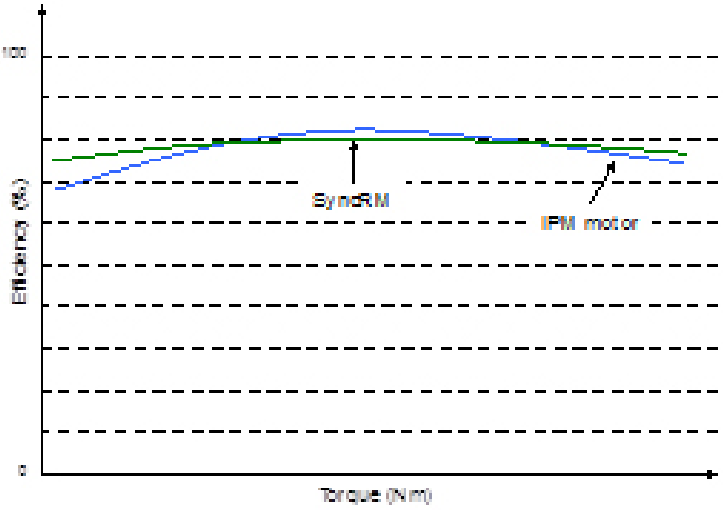


Figure 4: Load/Efficiency Curves (Motor & Drive)

So what do all these fancy new control algorithms provide anyway? Why isn't the trapezoidal-controlled BLDC motor good enough?

Efficiency

There is a lot of talk about more efficient motors and drives, but in the end it is the whole system efficiency that matters. For example, we talked about the serpentine belt in car engines. Belt transmissions are very efficient above 90%, but don't stop when something isn't needed. Instead, they start idling, which has significant losses. So, if we look at electro-mechanical systems, there are additional losses, such as vibration, which can be caused by

torque ripple, which in turn are side effects of the way BLDC motors and SRMs work. Based on the needs of the application, efficiency can be maximized further if the motor would run smoothly. This can be achieved by using an FOC algorithm or equivalent vector control.

Another factor is the load at which the motor is running. All motors have a load efficiency curve that looks something like the one in Figure 4 (this includes the drive). As can be seen, there is a peak, which is at the rated torque of the motor, but most applications don't have a fixed single operating load. Some even have to work the full width of the operating range. An example of that is the air-conditioner compressor. Here, the load changes based on how much the system has to cool or heat, and also during each piston cycle. Because compressors are nearly running all the time, the use of IPM motors has become common, as they have the highest efficiency. But, if we look at the efficiency curve of an IPM motor and compare it to an equivalent SyncRM (Figure 4), we see that even though the IPM motor has higher efficiency at the rated load, the SyncRM's curve is flatter. In other words, the SyncRM maintains higher efficiency at lighter load, making the over all efficiency for the application very similar to the IPM motor.

Conclusion

The trend toward higher efficiency for electrical motors started to accelerate since the new millennium, with advent of brushless permanent magnet motors and improved semiconductor cost and performance. This trend expanded into consumer products with the BLDC motor. Since then, it has evolved to include the electronic commutation of ACIMs, revival of the SRM, and even removal of the magnets again with the SyncRM.

What is important to remember in all of this is that the efficiency of a system is the sum of all the pieces, and how much you maximize it has to make financial sense. Therefore, depending on the application, there are different motor types and algorithms to choose from. There is no one motor technology that trumps all, and therefore, whoever is designing an electric motor-based system has to understand the pros and cons of the available technologies and select the best option for their needs.

Solving signal integrity problems at very high data rates

› Lee Ritchey, Scott McMorrow & Kella Knack, Samtec

The good news about the Internet of Things (IoT) is that it demonstrates just how pervasive high-speed communication technology has become. Addressing software issues within the IoT is pretty straight forward-create some code that people can readily download to their hardware devices to maintain the operating integrity of their various communication devices.

Addressing hardware issues is not so simple. Even experienced hardware developers are challenged in addressing these issues. Part of the problem is attributable to the nature of hardware technology itself. Printed circuit boards (PCBs) and the various other pieces of hardware associated with them have essentially "run out of gas". Moreover, wringing the last ounce of performance capability out of these devices often requires unprecedented and very creative engineering efforts.

Of course, the question arises as to why not just move to the next iteration of hardware technology? The answer to that question is very complicated. The next iteration of hardware technology is silicon photonics. It is not an easy process and making the move to it will require massive changes to the entire infrastructure including equipment, materials, and manufacturing processes. So, for the time being, we are stuck with tried and true PCB technology. And, for the next several years, we have to figure out how to make this technology work for us as long as possible. Or, more importantly, we need to figure out how we are going to get from here to there—how many ways and in which manner can existing hardware be "tweaked" to meet the escalating performance requirements of today's end products.

The state of technology

At the start of 21st century, providers of equipment for the Internet struggled to design large routers and switches containing backplanes and plug-in line cards that had long internal connections running at 3.125 Gb/s. The primary concern was how to manage loss in those long paths.

Fast forward to 2016 and the picture has changed radically. Manufacturers of the semiconductors used in route processors and switch ICs have managed to engineer them so they operate at speeds as high as 32 Gb/s with a very high tolerance for loss along the signal paths. The ICs of 2001 could tolerate as little as 10 dB of loss in the signal path at 3.125 Gb/s. The ICs of 2016 can tolerate as much as 38 dB of loss at 32 Gb/s.

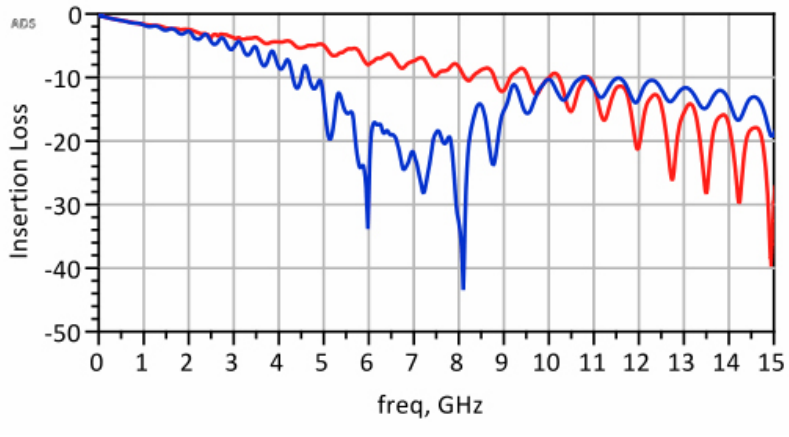


Figure 1. Block diagram of hybrid beamforming transmitter.

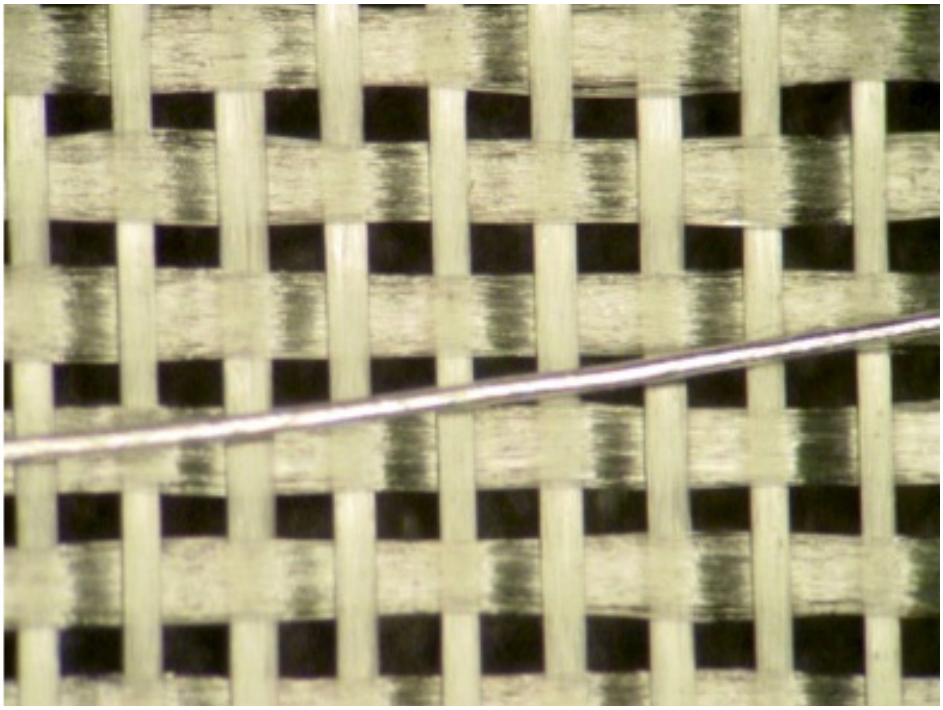


Figure 2. 1080 glass weave and a 3.5 mil wire

These changes have exposed a number of microdefects in the signal path that were of little consequence in previous products running at lower data rates. These microdefects include:

1. The parasitic capacitance of the plated through holes required to mount the connectors can introduce substantial bandwidth degradation.
2. Crosstalk between transmit and receive signals can be severe because those signals that tolerate 38 dB of loss at the receivers are far more susceptible to interference from a signal leaving a transmitter at full amplitude.
3. The difference in travel time of the two sides of a differential pair (skew) induced by the irregularities in the weave of the glass cloth required to provide mechanical strength in the PCB can cause a signal path to fail.
4. Signal loss along the data paths is still an issue but, in most cases, can be handled with the materials currently available used to fabricate PCBs and backplanes. However, as the shift is made to 56 Gb/s and higher, loss in the data path comes back into the equation as a major issue.

Solving the first three problems has met with varied success.

The first problem (excess capacitance in the plated through holes) has been dealt with by using a technique called back-drilling to remove the excess capacitance of the connector plated through holes that extend below the layer in which the signal traces are routed. In thick backplanes this has resulted in very complex manufacturing procedures to ensure enough of the plated through hole copper has been removed to achieve proper performance while at the same avoiding drilling so deep that the connection is severed.

Figure 1 is a loss vs. frequency plot of two 8" (20 cm) traces. The red trace is routed near the bottom of the PCB so that the signal travels nearly the full length of the vias used to connect to the trace. The blue trace is routed near the top of the PCB so that the signal travels only part of the way along the vias leaving small parasitic capacitors attached to each end of the trace. Clearly, the bandwidth of the blue trace has been severely affected by these parasitic capacitors. Back drilling removes this unwanted parasitic with the risks noted earlier.

The second problem (excess crosstalk) has been dealt with by routing the signals farther and farther apart from each other so this problem is

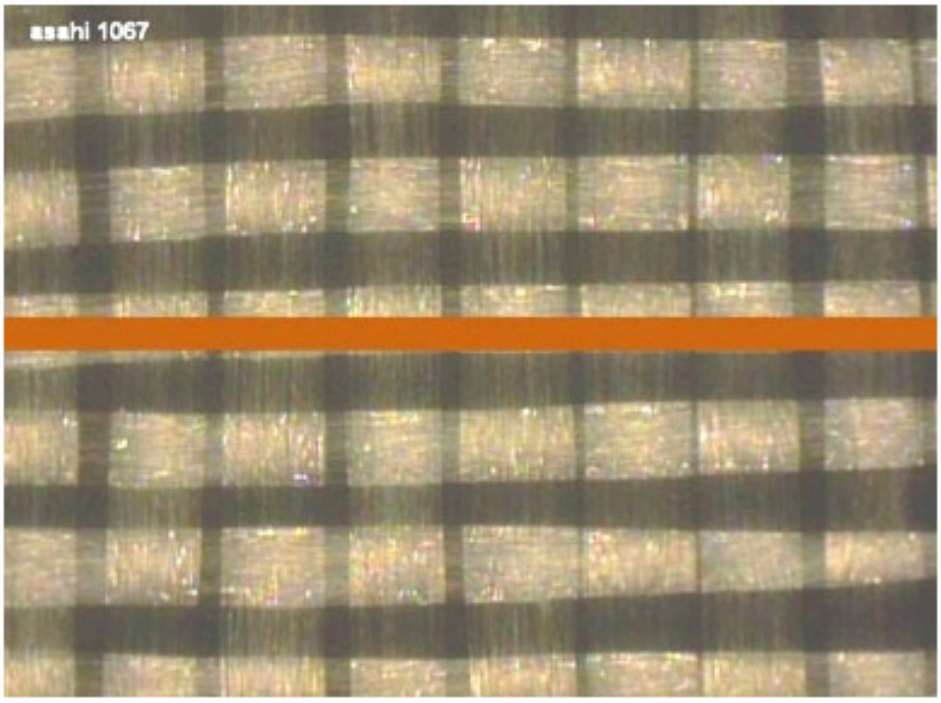


Figure 3. 1067 glass weave and a 4 mil trace

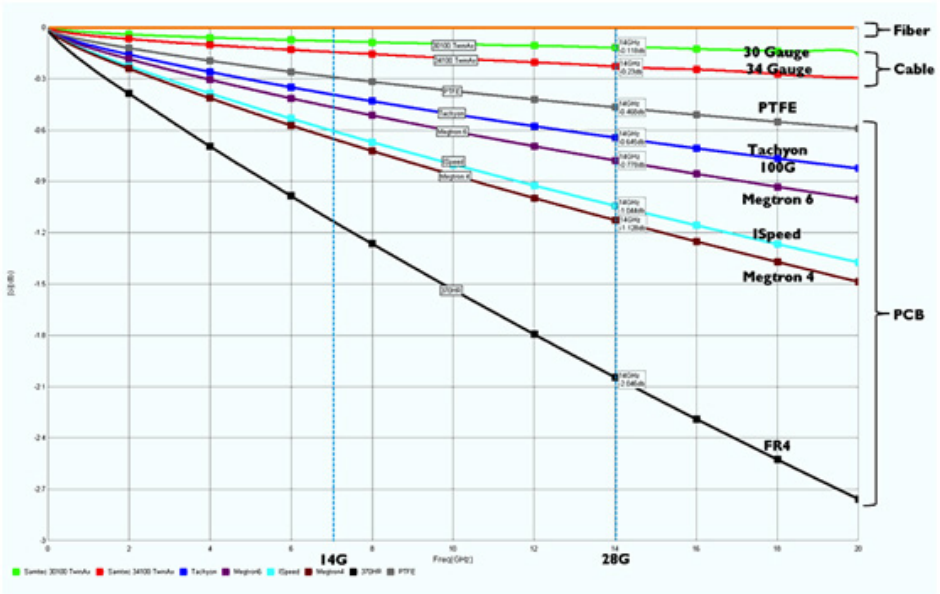


Figure 4. Loss vs. Frequency of materials available for high speed

minimized. However, when receive signals can be only 2 or 3% the amplitude of transmit signals this becomes mechanically very difficult to accomplish when routing signals on the same layer in the vicinity of the connectors.

The third of these (skew or difference in travel time in the two sides of a differential pair), is a result of the uneven distribution of the glass in the woven cloth and the resin used to bind the composite together. This unevenness is due to the fact that the glass bundles used to weave the cloth are much larger than the width of the traces. Figure 2 is a photo of a common glass weave cloth (1080) with a 3.5 mil (89 micron) wire superimposed on it to show the difference in scale of traces and glass weaves. Notice that for part of the time the wire is on top of a glass bundle with a dielectric constant of about 6 and part of the time it is in between glass bundles in pure resin that has a dielectric constant of about 3. Signals will travel faster when they are in pure resin than when they are traveling over glass. This variation in velocity is what causes differences in travel time between the two sides of a differential pair. We have seen differences in travel time over 14 inch (35 cm) differential pairs on 1080 glass as high as 62 ps. That is 60% of a bit period at 10 Gb/s and two bit periods at 32 Gb/s.

Many techniques have been proposed to minimize the effect of skew. The two most common methods in use are:

- Routing the signals at an angle to the glass weave hoping that the irregularities are evened out between the two sides of the pair.
- Using a glass weave style that has the glass evenly spread out to minimize variation in the glass weave over which signals travel.

The first of these two methods has taken two forms. One is to route the signals in the PCB at an angle so that when the PCB is fabricated the traces run at an angle to the glass cloth weave. This has proved impractical in most products because the large number of connector and component pins impose an X-Y grid on routing.

Alternatively, the PCB or backplane is routed on an X-Y orientation and the artwork is placed at an angle on the fabrication panel resulting in the traces running at an angle to the glass weave. This method wastes substantial amounts of board material

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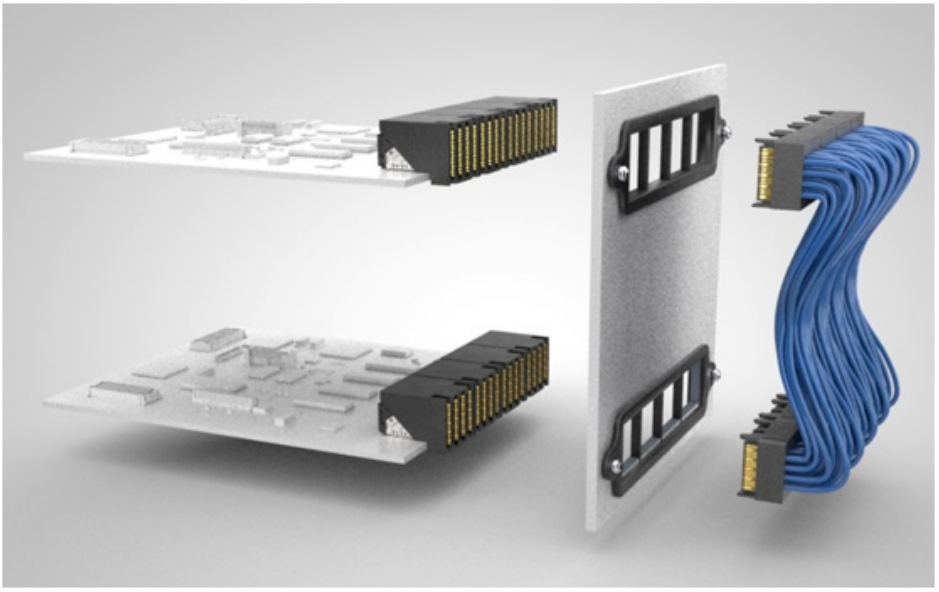

Figure 5. Backplane using twinax cabling in place of PCB traces

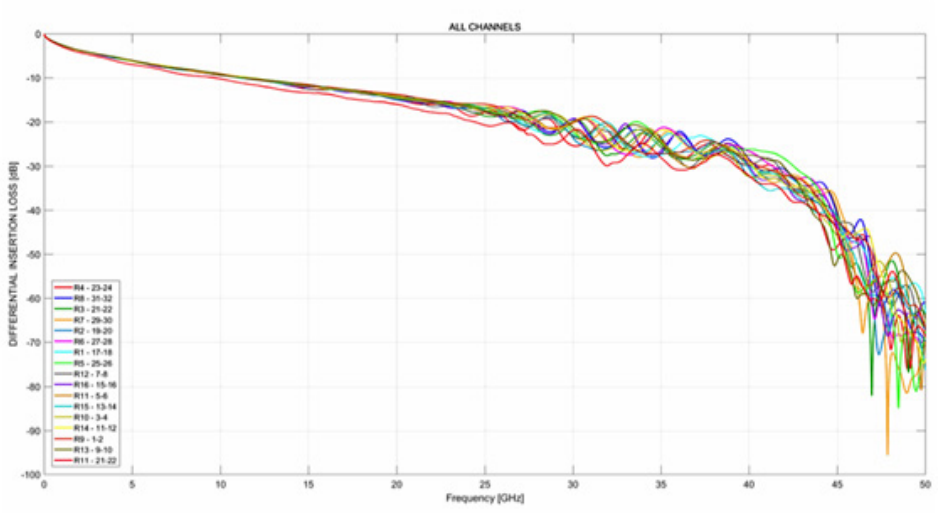

Figure 6. Differential cable insertion loss, 2.6-3m

on the fabrication panels which are rectangles and thus increases overall board cost.

Neither of these methods are satisfactory for most products which must compete in a price-sensitive market.

The second method employs a glass weave style that has the glass uniformly spread across the surface. Figure 3 is a photo of 1067 glass weave cloth with a 4 mil (102 micron) trace running across it. As can be seen, there are no resin filled voids in the example. Because of this, the difference in travel time of the two sides of the differential pair is minimized. In fact, we have been able to build quite large systems where the skew over 30 inches (76 cm) is less than 2 ps.

This sounds like the perfect answer to the skew problem. It would be if the methods by which the glass is spread were uniform between glass weavers. Unfortunately, this has proven not to be true. The driver for spreading the glass weave is the cell phone manufacturers. Their reason for spreading the glass is to make laser drilling of blind vias more uniform, not to preserve signal integrity. At present, there is no sure way to guarantee uniform spreading of the glass, so controlling skew by manipulating PCB laminates is problematic.

Dealing with signal-path loss

As mentioned at the start of this article, advances in semiconductor technology have resulted in transceivers that can tolerate as much as 38 dB of loss in the signal path at 32 Gb/s. This has made it possible to design systems with large backplanes with plug in modules. When the move to 56 Gb/s is made the materials that are available as laminates no longer have loss values that allow the design of the very large routers required in server farms and large IT centers. Figure 4 is the loss vs. frequency for a variety of materials that might be used to create next generation high performance Internet products.

Notice that the two curves labeled "cable" have far lower loss than any of the laminate systems used to manufacture current products. This loss is representative of what twinax cable can achieve. This solves the problem of how to achieve 56 Gb/s in large systems without the need to resort to optical interconnects.

More reliable & economical than PCB laminates

Since the signal integrity problem at high data rates in large systems

is directly traced to microdefects in the PCBs and connectors used to manufacture very large, high performance systems, removing these signals from those PCBs and backplanes can solve the problem. This is not a new idea. If one looks back to several of the high performance computers designed by Cray Research and other companies in that market, all of the very high speed signals were moved from PCB to PCB over shielded twisted pairs or, in some cases, unshielded twisted pairs. This latter technique is how the Ethernet has been able to operate over long distances using ordinary phone wiring at data rates as high as 1 Gb/s.

The first advantage of the cable method is the opportunity for crosstalk between signals to be eliminated.

A second advantage the cable method has is the backplane can now be manufactured from standard PCB laminate material as its only task is to carry power to the modules plugged into it and to hold all of the connectors in a rigid structure.

What about the problem caused by those plated through holes that are necessary to hold the connector pins in place as well as the plated through holes required to connect component pins to traces in the daughter cards? What has been demonstrated by simulations as well as by laboratory measurement is that when a signal travels the length of the plated through hole or via, the parasitic capacitance of the hole is distributed along the length of the hole, rendering it virtually invisible.

This leaves the task of tackling skew. When the differential pairs are connected with shielded pairs, such as twinax, the two sides of the differential pair travel in a very uniform dielectric that is common to both sides of the pair. The result is that skew or difference in travel time between the two sides of a pair can be made virtually zero.

Figure 5 is an example of a design that uses this twinax method to implement a very complex high performance switch/router. Using this method, performance as high as 56 Gb/s can be achieved using ordinary PCB materials. This avoids the problem of designing very complex PCBs and then managing the supply chain process to insure that all of the complex manufacturing problems are kept under control.

Figure 6 shows the loss vs. frequency of several 2.6m - 3m differential paths. The measured paths include two daughter cards connected through twinax cable as shown in Figure 5. The insertion loss is near ideal up to about 25 GHz. This demonstrates that this assembly is potentially capable of 50 Gb/s.

A further advantage of implementing all of the high performance signals in twinax cable is that it is possible to make wiring changes at the backplane level by reconfiguring the twinax cables to implement a new function not available when the original backplane design is done. This helps eliminate the "fork lift" upgrades often required with hard wired backplanes.

Conclusion

Advances in semiconductor technology are making it possible to connect components in products such as switches and routers at rates as high as 56 Gb/s. As these higher speeds are achieved, micro-scale variations in the materials used to fabricate PCBs and backplanes can significantly degrade signals. Among the problems encountered are loss, skew, crosstalk, and degradation due to the parasitic capacitance of the plated-though holes required to mount the connectors to the backplanes and daughter cards.

By using twinax cables to make these connections instead of implementing them in PCBs and backplanes with traditional traces, skew, crosstalk, and degradation from the plated-though holes can be virtually eliminated. Due to the ultra-low loss of the twinax cables, path lengths can be longer, or the frequency of operation can extend much higher than is possible with the laminate systems currently available.

Authors Ritchey & Knack are with Speeding Edge, McMorrow with Samtec division Teraspeed Consulting.

Optimizing Virtual Reality: Understanding Multiview

› Thomas Poulet, ARM

Introduction

As you may have seen, Virtual Reality (VR) is getting increasingly popular. From its modern origins on desktop, it has quickly spread to other platforms, mobile being the most popular. Every time a new mobile VR demo comes out I am stunned by its quality; each time it is a giant leap forward for content quality. As of today, mobile VR is leading the way; based on our everyday phone it makes it the most accessible and because you are not bound to a particular location and wrapped in cables, you can use it wherever you want, whenever you want.

As we all know, smooth framerate is critical in VR, where just a slight swing in framerate can cause nausea. The problem we are therefore facing is simple, yet hard to address. How can we keep reasonable performance while increasing the visual quality as much as possible?

As everybody in the industry is starting to talk about multiview, let us pause and take a bit of time to understand multiview, what kind of improvements one can expect and why you should definitely consider adding it to your pipeline.

Stereoscopic rendering

What is stereoscopic rendering? The scope of this post doesn't cover the theoretical details behind this question, but the important point is that we need to trick your brain into thinking that the object is real 3D - not screen flat. To do this you need to give the viewer two points of view on the object, or in other words, emulate the way eyes work. In order to do so we generate two cameras with a slight padding, one on the left, the other on the right. If they share the same projection matrix, obviously their view matrices are not the same. That way, we have two different viewpoints on the same scene.

Now, let us have a look at an abstract of a regular pipeline for rendering stereo images:

1. Compute and upload left MVP matrix
2. Upload Geometry
3. Emit the left eye draw call
4. Compute and upload right MVP matrix
5. Upload Geometry
6. Emit the right eye draw call
7. Combine the left and right images onto the backbuffer

We can obviously see a bit of a pattern here as we are emitting two draw calls, and sending the same geometries twice. If Vertex Buffer Objects can mitigate the latter, doubling the draw calls is still a major issue as it is adding an important overhead on your CPU. That is where multiview kicks in, as it allows you in that case, to render the same scene with multiple points of view with one draw call.

Multiview Double Action Extension

Before going into the details of the expected improvements, I would like to have a quick look at the code needed to get multiview up and running. Multiview currently exists in two major flavors: OVR_multiview and OVR_multiview2. If they share the same underlying construction, OVR_multiview restricts the usage of the gl_ViewID_OVR variable to the computation of gl_Position. This means you can only use the view ID inside the vertex shader position computation step, if you want to use it inside your fragment shader or in other parts of your shader you will need to use multiview2.

As antialiasing is one of the key requirements of VR, multiview also comes in a version with multisampling called OVR_multiview_multisampled_render_to_texture. This extension is built against the specification of OVR_multiview2 and EXT_multisampled_render_to_texture.

Some devices might only support some of the multiview extensions, so remember to always query your OpenGL ES driver before using one of them. This is the code snippet you may want to use to test if OVR_multiview is available in your driver:

```
const GLubyte* extensions = GL_CHECK( glGetString( GL_EXTENSIONS ) );
char * found_extension = strstr( (const char*)extensions, "GL_OVR_multiview" );
if (NULL == found_extension)
{
    exit( EXIT_FAILURE );
}
```

In your code multiview manifests itself on two fronts; during the creation of your frame buffer and inside your shaders, and you will be amazed how simple it is to use it.

```
glFramebufferTextureMultisampledMultiviewOVR = PFNGLFRAMEBUFFERTEXTUREMULTISAMPLEDMULTIVIEWOVR(eglGetProcAddress("g
glFramebufferTextureMultisampledMultiviewOVR (GL_DRAW_FRAMEBUFFER, GL_COLOR_ATTACHMENT0, textureID, 0, 0, 2);
```

That is more or less all you need to change in your engine code. More or less, because instead of sending a single view matrix uniform to your shader you need to send an array filled with the different view matrices.

Now for the shader part:

```
#version 300 es

#extension GL_OVR_multiview : enable

layout(num_views = 2) in;

in vec3 vertexPosition;

uniform mat4 MVP[2];

void main(){
    gl_Position = MVP[gl_ViewID_OVR] * vec4(vertexPosition, 1.0f);
}
```

Simple isn't it?

Multiview will automatically run the shader multiple times, and increment gl_ViewID_OVR to make it correspond to the view currently being processed.

For more in depth information on how to implement multiview, see the sample code and article "Using Multiview Rendering".

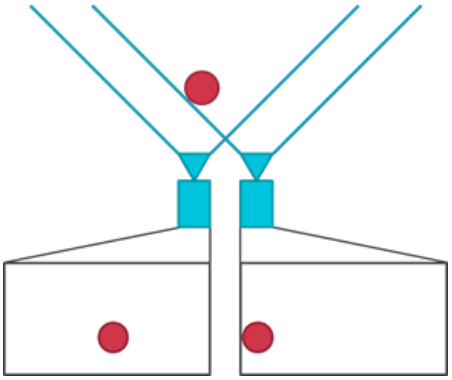

Fig. 1: Stereo camera setup

Why using Multiview?

Now that you know how to implement multiview, I will try to give you some insights as to what kind of performance improvements you can expect.

The Multiview Timeline

Before diving into the numbers, let's discuss the theory.

In this timeline, we can see how our CPU-GPU system is interacting in order to render a frame using regular stereo. For more in depth information on how GPU scheduling works on Mali, please see Peter Harris' blogs.

First the CPU is working to get all the information ready, then the vertex jobs are executed and finally the fragment jobs. On this timeline the light blue are all the jobs related to the left eye, the dark blue to the right eye and the orange to the composition (rendering our two eyes side by side on a buffer).

In comparison, this is the same

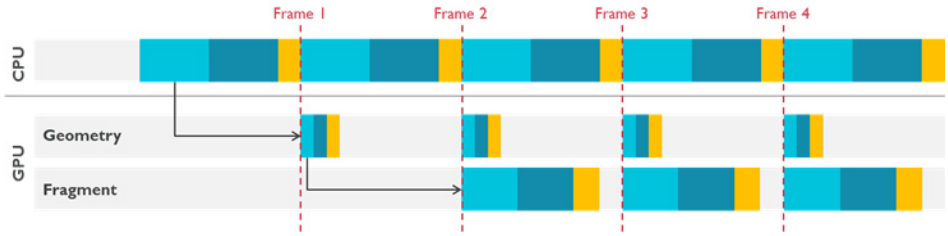

Fig. 2: Regular Stereo job scheduling timeline

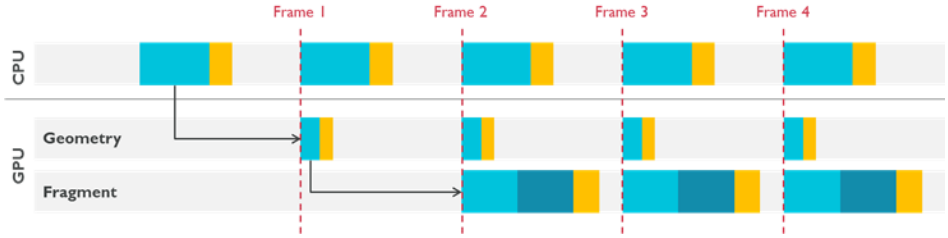

Fig. 3: Multiview job scheduling timeline.

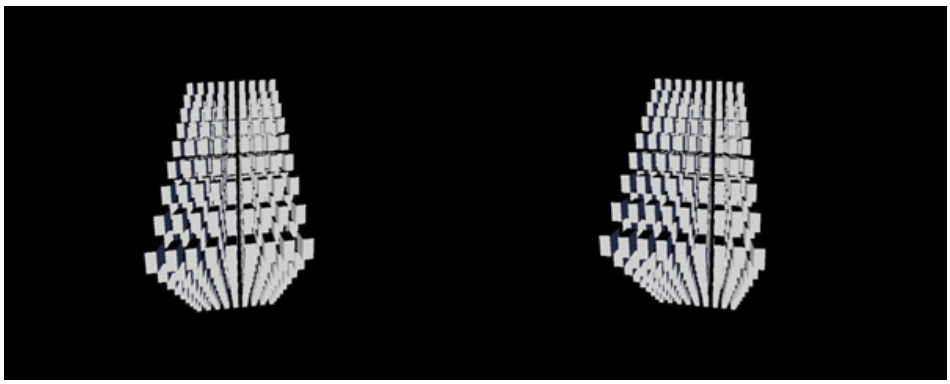

Fig. 4: Scene used to measure performances

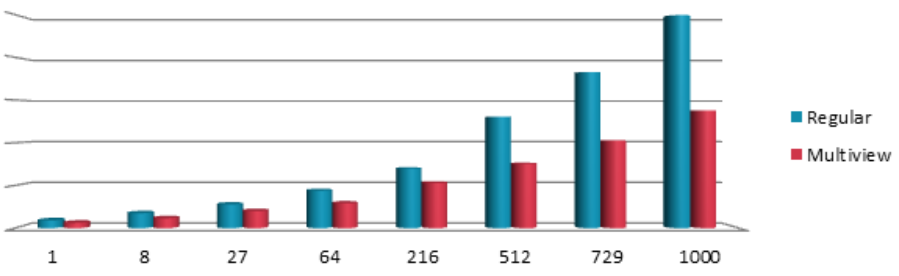

Fig. 5: Relative CPU time between multiview and regular stereo. The smaller the better, with the number of cubes on the x-axis and the relative time on the y-axis. Multiview in red, and regular stereo in blue

frame rendered using multiview. As expected since our CPU is only sending one draw call, we are only processing once on the CPU. Also, on the GPU the vertex job is smaller since we are not running the non-multiview part of the shader twice. The fragment job, however, remains the same as we still need to evaluate each pixel of the screen one by one.

Relative CPU Time

As we have seen, multiview is mainly working on the CPU by reducing the number of draw calls you need to issue in order to draw your scene. Let us consider an application where our CPU is lagging behind our GPU, or in other words is CPU bound.

In this application the number of cubes is changing over time, starting from one and going up to one thousand. Each of them is drawn using a different draw call - obviously we could use batching, but that's not the scope here. As expected, the more cubes we add, the longer the frame will take to render. On the graph below, where smaller is better we have measured the relative CPU time between regular stereo (Blue) and multiview (Red). If you remember the timeline, this result was expected as multiview is halving our number of draw calls and therefore our CPU time.

Relative GPU Time

On the GPU we are running vertex and fragment jobs. As we have seen in the timeline (Fig. 3), they are not equally affected by multiview, in fact only vertex jobs are. On Midgard and Bifrost based Mali GPUs only multiview related parts in the vertex shaders are executed for each view. In our previous example we looked

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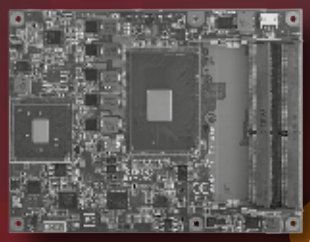

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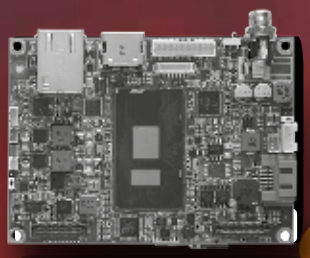

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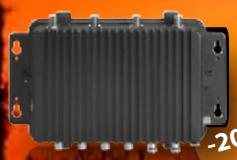

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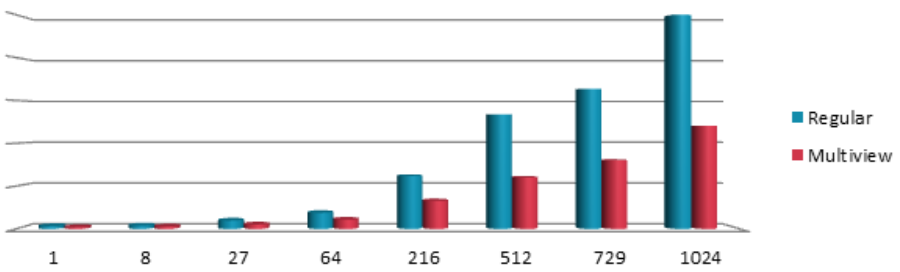


Fig. 6: Relative GPU time between multiview and regular stereo. The smaller the better, with the number of cubes on the x-axis and the relative time on the y-axis. Multiview in red, and regular stereo in blue

Fig. 7: Example of an application using foveated rendering

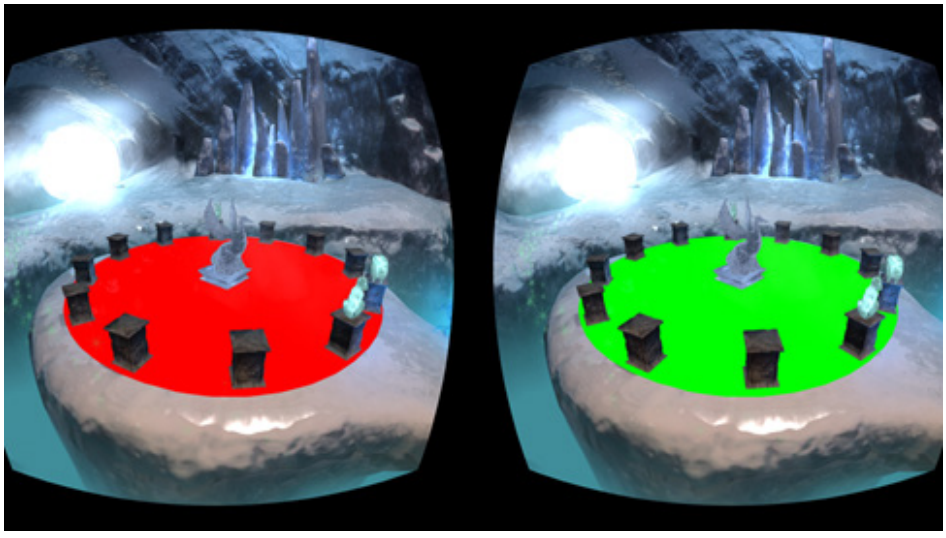


Fig. 8: A different reflection for each eye, demonstrated here in Ice Cave VR

at relative CPU time, this time we have recorded the relative GPU Vertex jobs time. Again, the smaller the better, regular stereo in blue and multiview in red.
The savings are immediately visible on this chart as we are no longer computing most of the shader twice.

Wrap it up

From our measurements multiview is the perfect extension for CPU bound applications, in which you can expect between 40% and 50% improvements. If your application is not yet CPU bound multiview should not be overlooked as it can also somewhat improve your vertex processing time at a very limited cost.
It is noteworthy that multiview is rendering to an array of textures inside a framebuffer, thus the result is not directly ready for the front buffer. You will first need to render the two views side by side, this composition step is mandatory, but in most cases the time needed to do so is small compared to the rendering time, and can thus be neglected. Moreover, this step can be integrated directly in the lens deformation or timewarp process.

Multiview Applications

The obvious way, and the one already discussed in this article, is to use multiview in your VR rendering pipeline. Both of your views are then rendered using the same draw calls onto a shared framebuffer. If we try to think outside the box though, it opens up a whole new field in which we can innovate.

Foveated Rendering

Each year sees our device screen

getting bigger and bigger, our content becoming increasingly more complicated and our rendering time staying the same. We have already seen what we could save on the CPU side but sometimes fragment shaders are the real bottleneck. Foveated rendering is based on the physical properties of the human eye where only 1% of our eye (called the fovea), is mapped to 50% of our visual cortex.

Foveated rendering uses this property to only render high resolution images in the center of your view, allowing us to render a low resolution version on the edges.

For more information on foveated rendering and eye tracking applications, you can have a look at Freddi Jeffries' blog Eye Heart VR. Stay tuned for a follow-up of this blog on foveated rendering theory.

We then need to render four versions of the same scene, two per eye, one high, one low resolution. Multiview makes this possible by sending only one draw call for all four views.

Stereo Reflections

Reflections are a key factor for achieving true immersion in VR, however, as for everything in VR it has to be in stereo. I won't discuss the details of real time stereo reflections here, please see Roberto Lopez Mendez's article Combined Reflections: Stereo Reflections in VR for that. In short, this method is based on the use of a secondary camera rendering a mirrored version of the scene. Multiview can help us achieve the stereo reflection at little more than the cost of a regular reflection, thus making real time reflections viable in mobile VR.

Conclusions

As we have seen throughout this article, multiview is a game changer for mobile VR as it allows us to unload our applications and finally consider the two similar views as one. Each draw call we save is a new opportunity for artists and content creators to add more life to the scenes and improve the overall VR experience.

If you are using your custom engine and OpenGL ES 3.0 for your project, you can already start working with multiview on some ARM Mali based devices, like the Samsung S6 and S7. Multiview is also drawing increased attention from industry leaders. Oculus, starting from Mobile SDK 1.0.3, is now directly supporting multiview on Samsung Gear VR and if you are using a commercial engine such as Unreal, plans are in progress to support multiview inside the rendering pipeline.

Fast Track: How Next-Gen Interconnects Enable High-Speed Data

› Jairo Guerrero, Molex, LLC

The continuous growth in IP services and access speeds has led to exponential growth in bandwidth demand, driving the need for higher speed interfaces in routers and switches. That, in turn, has led to the development of new interconnect technology and new standards for 40 Gbps and 100 Gbps interfaces. And plans for 400 Gbps speeds are now materializing, so there will be no rest for connector designers!

The need to transmit more data at higher speeds is changing system design. New strategies include developing connectors with features and capabilities specifically for high-speed operations, maintaining signal integrity at high speeds and using new protocols.

For example, it's becoming apparent that PAM4 will play a growing role in this transition. NRZ (non-return-to-zero) signaling, an industry standard, is giving way to PAM4 modulation in many applications due to PAM4's ability to process data rates of 56 Gbps, 100 Gbps and higher.

While PAM4 does offer important speed improvements over NRZ, its downside is that data must be encoded prior to transmission, then de-encoded when received. This requires additional processing capability, making PAM4 more challenging to implement. Still, where high speeds are critical, the additional capability of PAM4 balances out the higher processing costs.

At the same time, it's important to keep in mind that NRZ is still appropriate for certain high-speed applications. Indeed, new backplane connectors can provide data rates above 50 Gbps in both PAM4 and NRZ systems. Compared to in-line beams, these backplanes optimize signal integrity performance and improve insertion loss, enabling interface resonance frequency that exceeds 30 GHz. They also deliver an enhanced signal integrity by optimizing geometries and differential shielding that minimize impedance discontinuities and reduce crosstalk.

Meeting New Challenges

When speeds increase, traditional connector challenges are magnified. For example, higher data speed channels typically involve increased electromagnetic interference, higher crosstalk and impedance discontinuities, so protection against these issues must be designed in. Also, the connectors described above typically have to work with existing headers (ensuring backwards compatibility), enabling integration into existing designs. For example, if

only the daughtercard is enhanced, the same headers can be used.

Another issue with increased system speeds is maintaining appropriate signal integrity. One way to accomplish this is to remove high-speed signals from the PCB by applying high-speed copper cable. This alternative can be used with both 50 Gbps NRZ and 50 Gbps PAM4 live, encoded serial traffic using QSFP cable assemblies and connector interfaces.

Tools that Expedite Design

With new designs required for high-speed connectors, tools that can reduce the time required to simulate system design are welcome. In traditional manual system simulation, each component is simulated independently. That means it can take a week or more to simulate individual system designs. When multiple design iterations are required, this can slow the design process down to a crawl.

Using a different approach, new software-based design tools employ libraries of pre-simulated models based on typical designs, materials, traces and vias. Designers select the models they want, push the enter key on their computer, and get results almost immediately. The software allows first-order system approximation, giving designers new insight into critical parameters for developing a new system. Designers are being tasked with getting their systems to market more rapidly and they are using more high-speed interconnects. As a result, automated design tools will gain in importance and value.

New Approach for Mezzanines

High-speed mezzanine systems offer another route to drive increasing data speeds. With tunable differential pairs, enabling matched impedance configurations, single ended lines and power, combined with a range of stack heights and compliant-pin terminations, the high-speed mezzanine connectors are enabling data rates up to 56 Gbps. These are appropriate for high-speed infotech and telecom applications, among others.

The typical attachment for mezzanine connectors is either press fit or SMT (while there are some compression versions), with both options presenting advantages and disadvantages, such as the process easiness of a press fit mezzanine connector, while SMT connectors typically drive enhanced performance by allowing footprint optimization and removing stub effect from the compliant pin. The downside is mainly centered on the rework aspect as it becomes more challenging than a press fit attachment.

In recent times, new technologies allow to reduce the performance gap between SMT and press fit, to the point that the difference is null in a real channel, so when matching the signal integrity then it becomes more of a preference option to design either attachment method, which will be mainly driven by layout, routing and board thickness (among other variables). In addition, compliant-pin technology allows system designers to rework the board and maximize system utility while achieving the necessary signal integrity.

Finally, employing a triad wafer design, the high-speed mezzanine connector offers the following options: high-speed differential pairs that can be tuned to 85- to-100-Ohm impedances, single-ended triads for low-speed options, and power triads. As a result, designers need only one connector for different signal speeds, freeing up space on the PCB and true reflection of the designer's preferred pinout.

Thermal Management Strategies

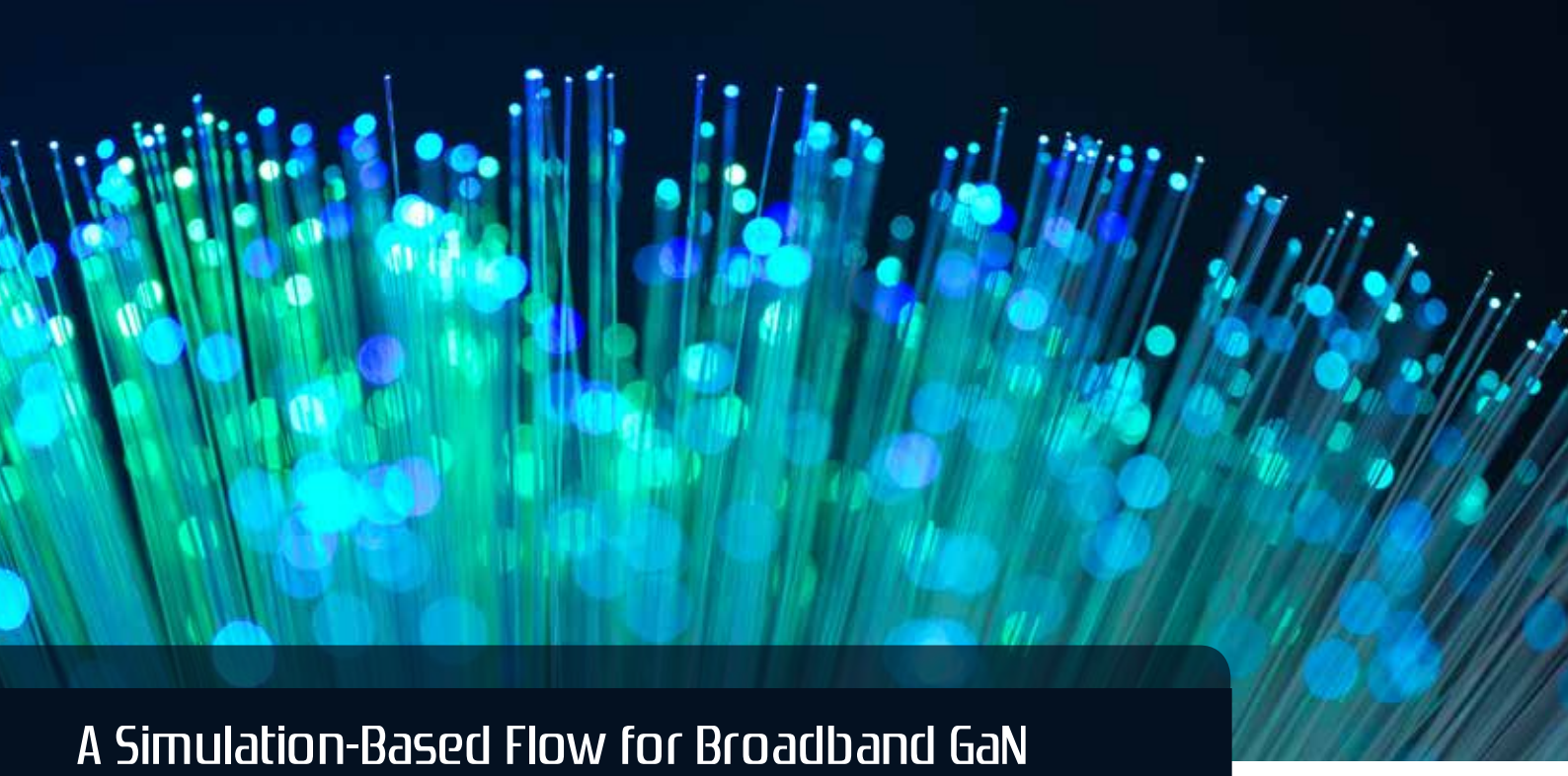
As speeds increase and new modules enter the market, enhanced thermal management solutions are becoming a key element for next generation systems.

For example, stacked connectors deliver higher speed but use about 4.5 to 5 W more power — and produce more heat — in 100 Gbps QSFP modules than standard interconnects.

For the most part, temperatures in enterprise systems must be controlled to below 70°C in the module and below a 45°C ambient temperature in the enclosure. Otherwise, the result can be degradation in reliability and overall performance decline.

One successful new heat management approach is to design in internal riding heat sinks and high-flow cages that can optimize air movement. Utilizing these technologies reduced overall temperature in an emulated 5 W optical QSFP module by 9°C. Thermal management strategies like this one will be vital for next-generation modules that are required to support at least 7 W (or more).

As we move into the fast-data future, new interconnect solutions must enable both advanced technology and increased network bandwidth. Successful products will need the capability to support a wide range of data rates using multiple connector shapes and sizes. New designs must meet demanding high-speed performance requirements while providing next-generation efficiency and reliability.



A Simulation-Based Flow for Broadband GaN Power Amplifier Design

› Ivan Boshnakov, ETL Systems Ltd. & Malcolm Edwards, AWR Group, NI, & Larry Dunleavy & Isabella Delgado, Modelithics Inc.

Overview

This application note demonstrates a simulation-based methodology for broadband power amplifier (PA) design using load-line, load-pull, and real-frequency synthesis techniques. The design highlighted in this application note is a Class F amplifier created using the Qorvo 30 W gallium nitride (GaN) high electron mobility transistor (HEMT) T2G6003028-FL. Goals for this design included a minimum output power of 25 W, bandwidth of 1.8 - 2.2 GHz, and maximum power-added efficiency (PAE). The design procedure was performed using the Modelithics GaN HEMT nonlinear model for the Qorvo transistor in conjunction with NI AWR Design Environment™, inclusive of Microwave Office circuit design software, Modelithics Microwave Global Models, and the AMPSA Amplifier Design Wizard (ADW).

Design Overview

The design for this PA began with measurements of the voltage and current at the drain-source intrinsic current generator within Microwave Office. The near optimum load line, terminating impedances at the fundamental frequency, and impedances at harmonic frequencies for a single-drive frequency were located for the required mode of operation. The impedance regions were then extracted using load-pull simulations. Using ADW with Microwave Office software, the real-frequency synthesis of the matching networks was quickly realized simultaneously for the fundamental and harmonic impedances across a wide bandwidth. These fully laid-out matching networks were then exported to Microwave Office software for the remainder of the design optimization, nonlinear analysis, and electromagnetic (EM) simulation.

Design Process

To begin the design process, a schematic was created to bias and stabilize the transistor. Once the conditions required for stability and biasing were established, the initial load-line analysis and harmonic-impedance tuning could be performed, as shown in Figure 1.

Initial Load-Line and Harmonic Impedance Tuning

First, a line was drawn on top of the IV curves to approximate the near-optimum load line for the fundamental frequency (the maximum swing of the RF voltage and current before hard clipping occurs). A dynamic load line was defined using meters located within the model to monitor the intrinsic drain voltage and current and superimposed on the IV curves by the IV dynamic load line (DLL) measurement. It was then tuned to be a straight line and parallel to the drawn line. The tuning at a chosen frequency was performed by

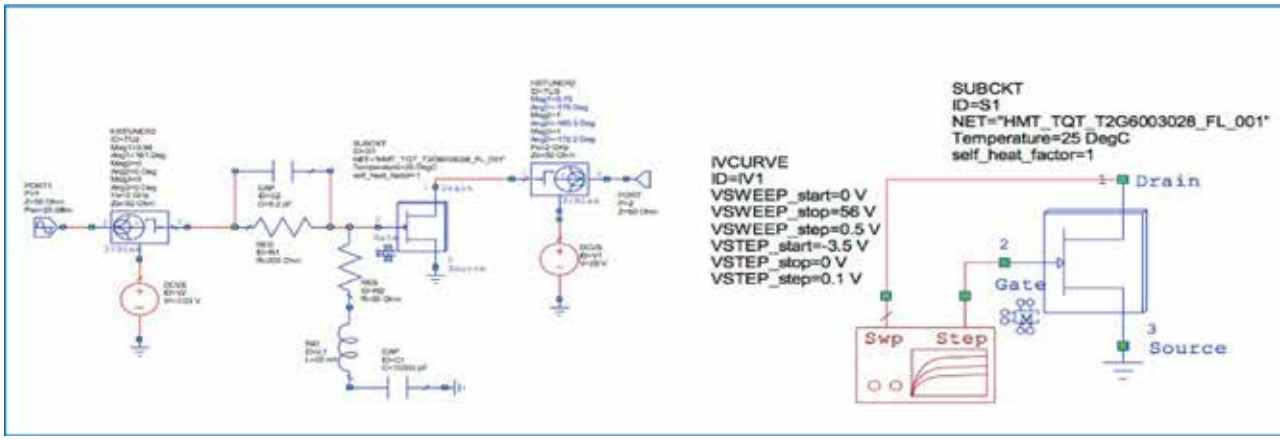


Figure 1: Initial load-line analysis and harmonic impedance tuning. Left side is the schematic to bias and stabilize transistor and right is the IV curve simulation schematic

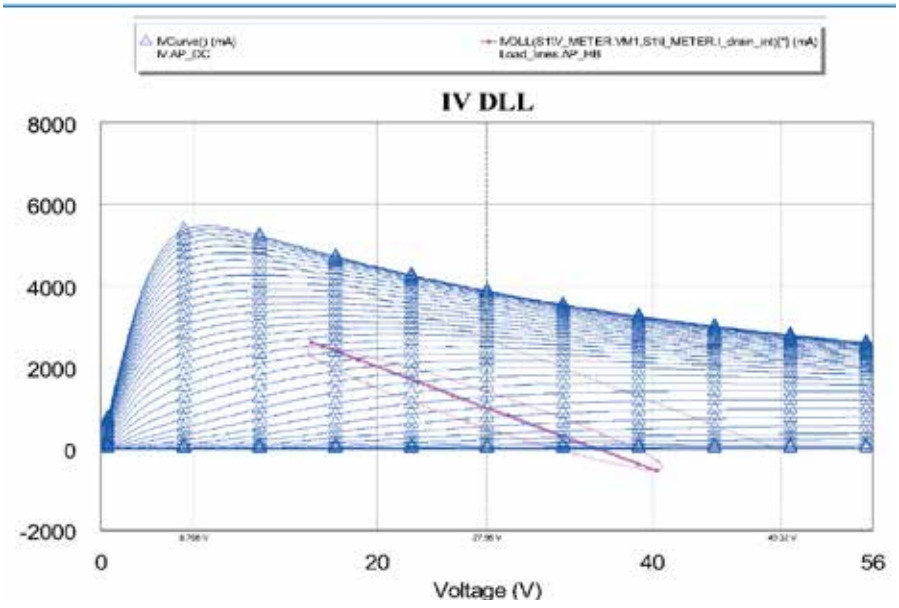


Figure 2: Final results of tuning with IV curves with dynamic load line superimposed

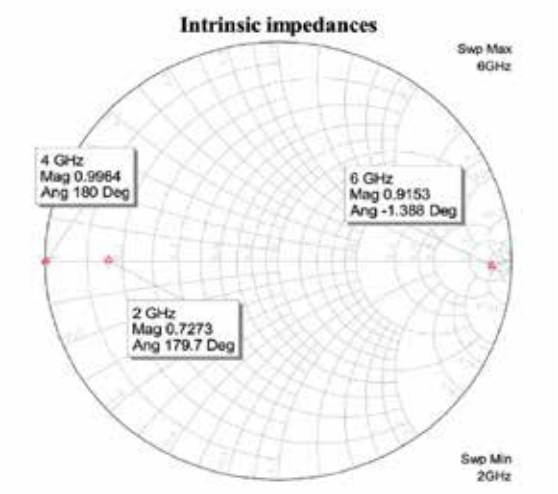


Figure 3: Smith chart view of the fundamental and harmonic impedances of the output tuner

tuning the magnitude and phase of the output tuner impedances. At this stage, the harmonic balance (HB) simulation was limited to just a single harmonic – the fundamental frequency. Additionally, the harmonic impedances of the output tuner and all the impedances of the input tuner were set to 50 ohms. The final results of this load-line tuning can be seen in Figure 2.

Once the impedance of the fundamental frequency was determined, the second and the third harmonic impedances presented to the intrinsic drain were tuned according to the desired mode of operation. In the case of this application note, Class-F operation was desired, meaning that the second harmonic impedance was tuned to a short circuit and the third harmonic impedance was tuned to an open circuit, as shown in Figure 3.

The fundamental impedance of the input tuner was then set to be a conjugate match to the S11 of the transistor and stability / bias network. This would provide the best match, and, therefore, maximum gain. The harmonic impedances of the input tuner were set to 50 ohms.

Once all of the impedances were tuned, a final harmonic balance simulation (using three harmonics) was performed to confirm the design was in the desired mode of operation. Figures 4 and 5

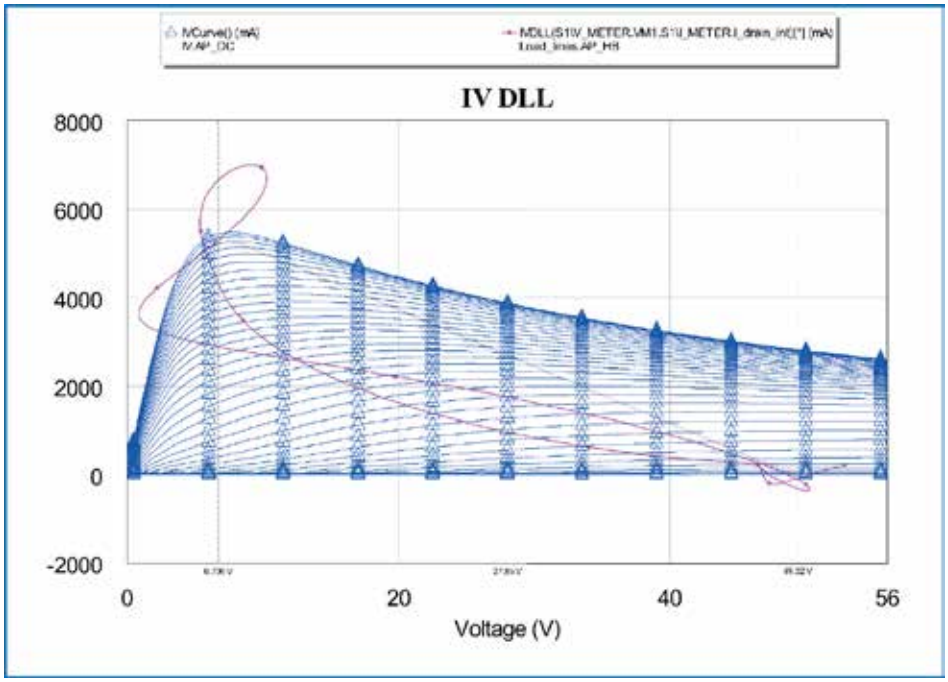


Figure 4: Final dynamic load-line after harmonic impedance tuning

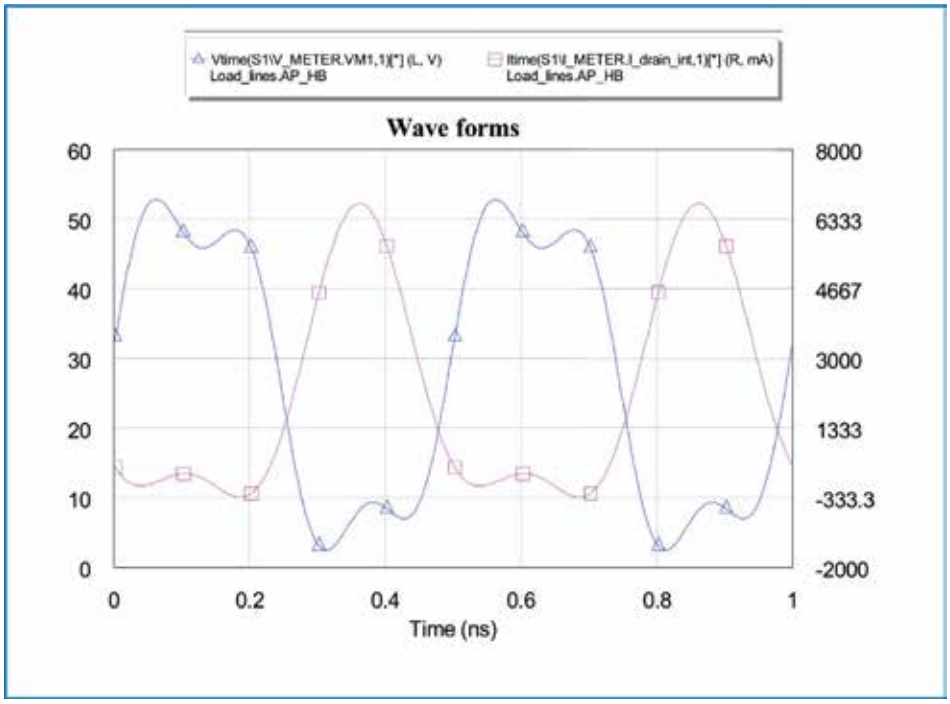


Figure 5: Intrinsic voltage and current waveforms after harmonic impedance tuning

show the classic shapes of a Class-F mode design.

Load-Pull Impedance Extraction

With the previously defined input and output impedances, load-pull simulations were performed to produce contours, first for maximum power (Pmax) and then for maximum drain efficiency (DCRF). The same schematic was used for the load-pull simulations as for the initial tuning, except for the addition of an XDB control element (Figure 6). This provided contours that were not only at a constant power and efficiency, but also at a constant gain compression.

Notice that the schematic is identical to that of Figure 1, however, the input and output impedances have been updated and the XDB component has been added.

In Figure 7 the contours at the fundamental frequency for both maximum power and efficiency have been superimposed in order to define a region of compromise for mutually acceptable power and efficiency. In this case, an output power 1 dB below the maximum and an efficiency five percent below the maximum was chosen. In the plot shown in Figure 7, a circle defining this region was placed by using an equation to define the acceptable area of the fundamental frequency impedance for the synthesis of the relatively broadband output network.

In the next step, load-pull simulations for second and third harmonic frequencies were performed at the two impedances that provided the maximum power and maximum efficiency in the load-pull simulation of the fundamental frequency. The results for both load-pull simulations at the second and third harmonic can be seen in Figure 8. For the simulation at the second harmonic frequency, the optimum maximum efficiency in both cases was the same and the contours were essentially the same. A line was drawn to bound the area with acceptable performance. In this case, the acceptable region was below the line. For the simulation at the third harmonic frequency, the optimum maximum efficiency was again the same in both cases, however, the contours differed somewhat. Fortunately, the effect of varying the third harmonic impedance was small and an acceptable region was easily defined above the drawn line.

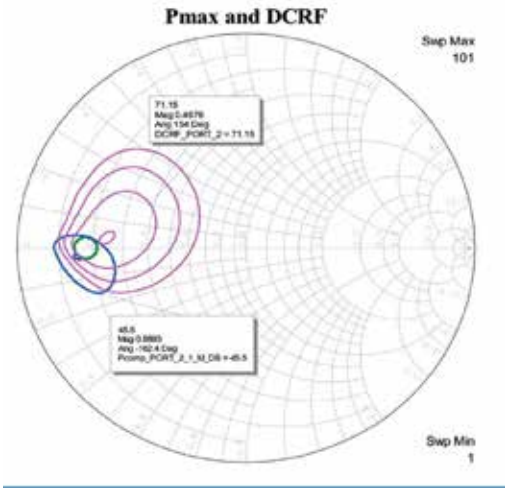


Figure 6: Load-pull simulation schematic

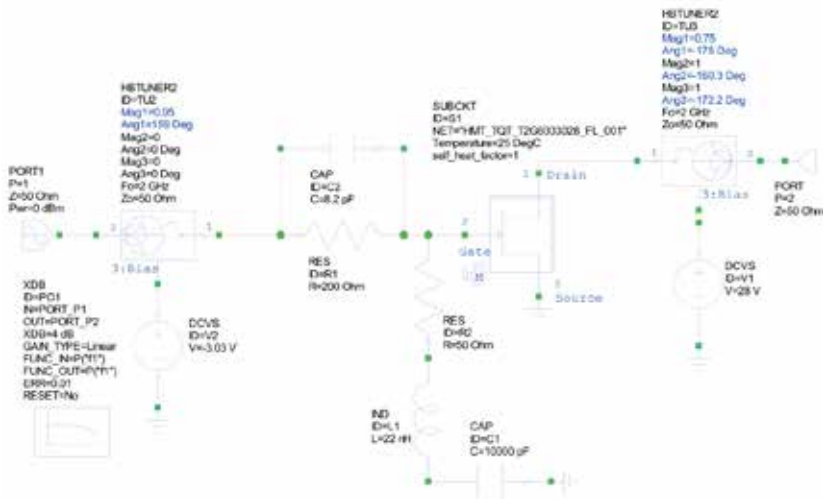


Figure 7: The load-pull contours of the fundamental frequency for maximum power (blue) and drain efficiency (magenta) have been plotted in the same Smith chart. The green circle defines the region of mutually acceptable power and efficiency

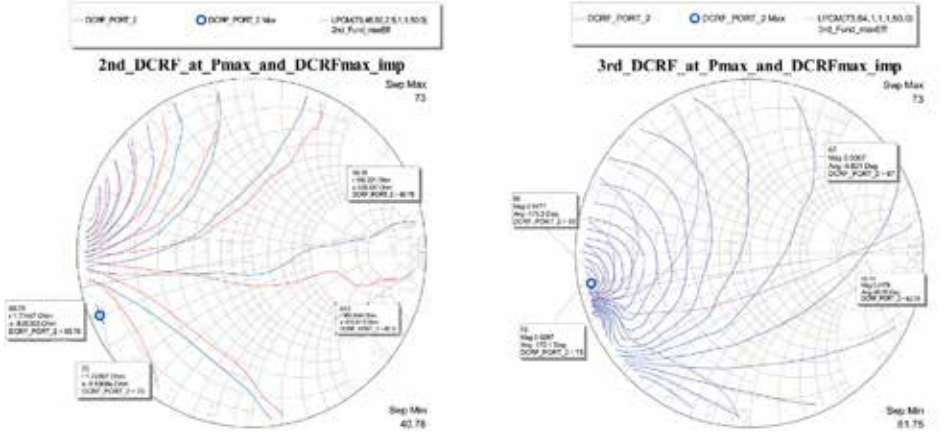


Figure 8: Left – Plot of load-pull contours for the second harmonic frequency at the fundamental impedances for maximum power and drain efficiency. The acceptable region is below the drawn line. Right – Plot of load-pull contours for the third harmonic frequency at the fundamental impedances for maximum power and drain efficiency. The acceptable region is above the drawn line

The described impedance extraction process was performed for a few frequencies across the desired bandwidth. In the case of this application note, simulations for 1.8 GHz, 2 GHz, and 2.2 GHz were sufficient. It is important to note that this was a streamlined method of extracting the fundamental and harmonic impedances that relied on access to the voltage and current across the intrinsic generator. Access to the intrinsic device nodes enabled a near optimum tuning of the fundamental load line (impedance) and allowed for fixing the harmonics impedances for a particular mode of operation at the outset of the design flow. This capability, along with model availability, greatly sped up the design process by reducing iterative tuning between fundamental and harmonic load impedances.

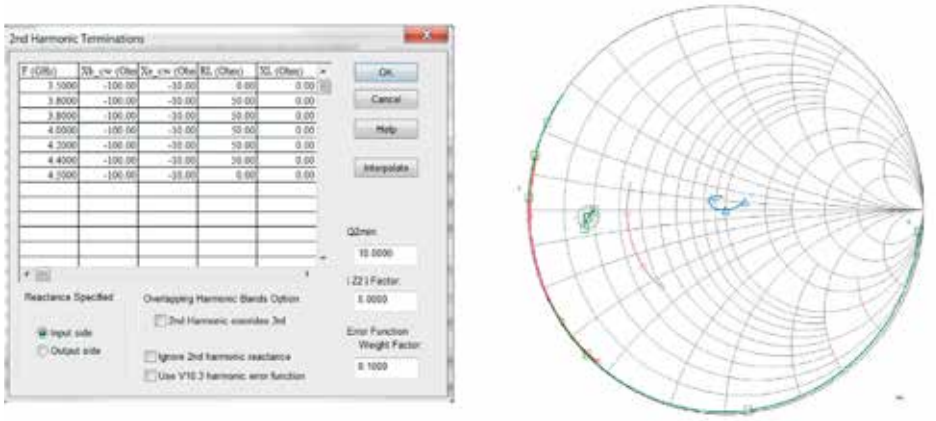
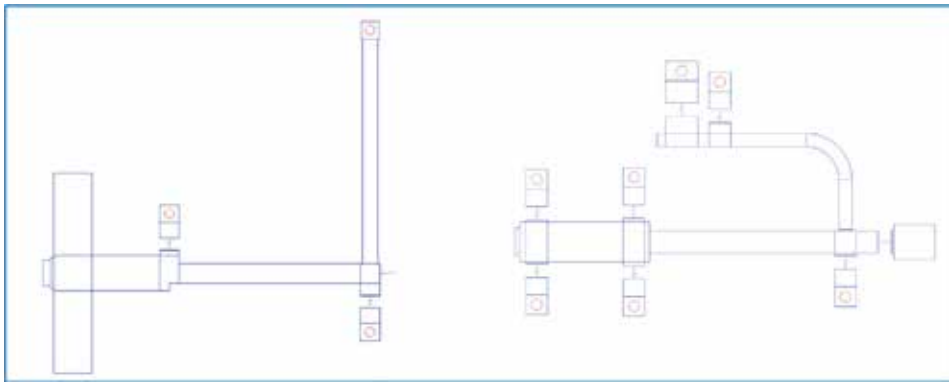


Figure 9: Left - Examples of the termination definition facilities in ADW. Right – Smith chart view of desired termination impedances (red, grey, pink, and blue) versus achieved impedances (green)

If the transistor model was a black box or the intrinsic access was not used, the load-pull impedance extractions would need to be performed for far more iterations. First, load pull for the fundamental frequency would have to be performed with the harmonics set to 50 ohms. Then, the load pull would have to be performed for harmonic loads and then with the newly found harmonic impedances. For the highest performance, load-pull analysis/optimization at the fundamental frequency would again need to be repeated. More iteration would be needed for the harmonics, and at that point one might want to stop the iterations. The issue with this approach, other than the number of iterations required, is the uncertainty that optimum loads have actually been defined, and nothing would be known of mode of operation.



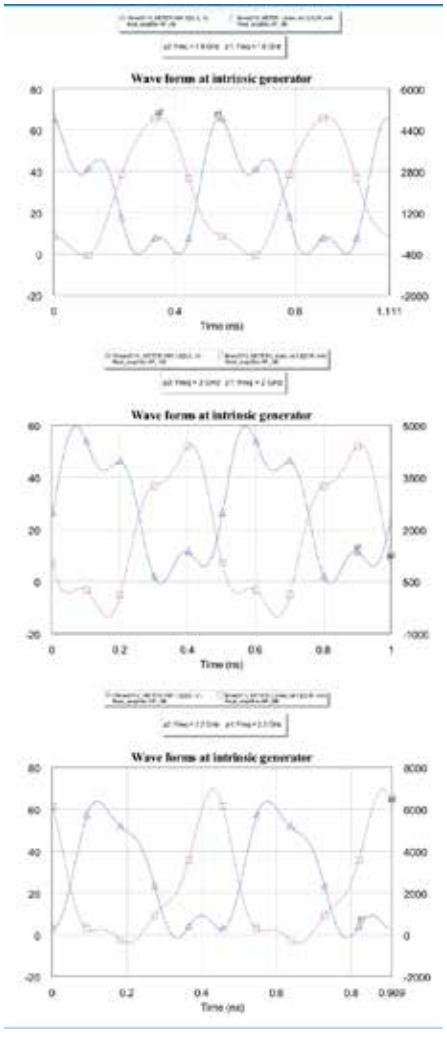


Figure 10: Left – Initial hybrid microstrip / lumped-element output-matching network created in ADW. Right – Final output matching network after decoupling elements, optimization, and layout manipulation is complete

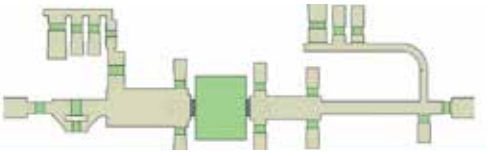


Figure 11: Final layout for the Class-F amplifier design

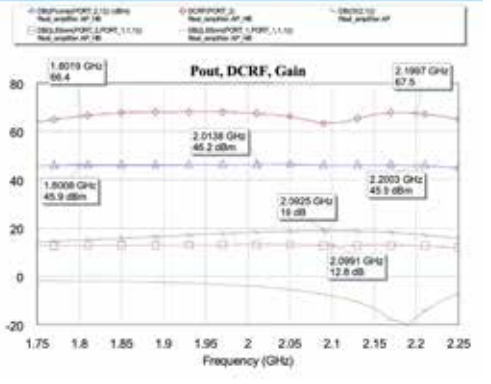


Figure 12: Final simulated performance for the Class-F amplifier design

Figure 13: Simulated intrinsic device channel voltage and current wave forms at 1.8 GHz (top), 2 GHz (center), and 2.2 GHz (bottom).

Matching Network Synthesis

Once all impedances were determined, ADW was used to synthesize the broadband matching networks. The required fundamental and harmonics impedance areas across the desired bandwidth were defined in the corresponding facilities of ADW, shown in Figure 9. The fundamental impedance areas for each frequency are circles on the Smith chart. The harmonic impedance areas are sections of the Smith chart.

Based on the impedances input into ADW, an initial hybrid microstrip / lumped-component output-matching network was synthesized (left image in Figure 10). The initial design was then exported into ADW's analysis facility for the addition of all decoupling components, optimization, and layout manipulation. The final output-matching network design can be seen on the right in Figure 10. The same process was performed for the input matching network and both designs were exported to Microwave Office software to finalize the design.

Finalizing the Design

Once the matching networks were in Microwave Office, Modelithics models were substituted for the surface-mount lumped-element models used in ADW. Final linear, HB, EM, and DC simulations were then performed in Microwave Office to fine tune the design. The

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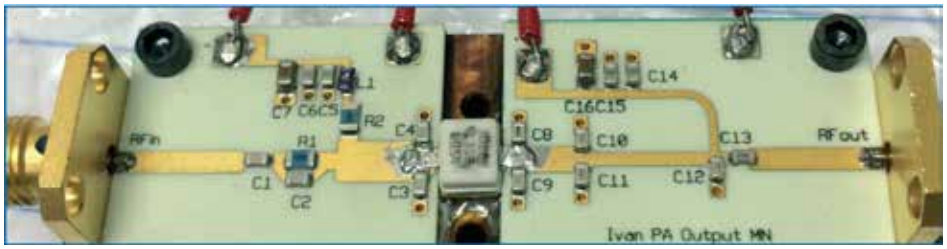

Figure 14: Assembled Class-F amplifier design

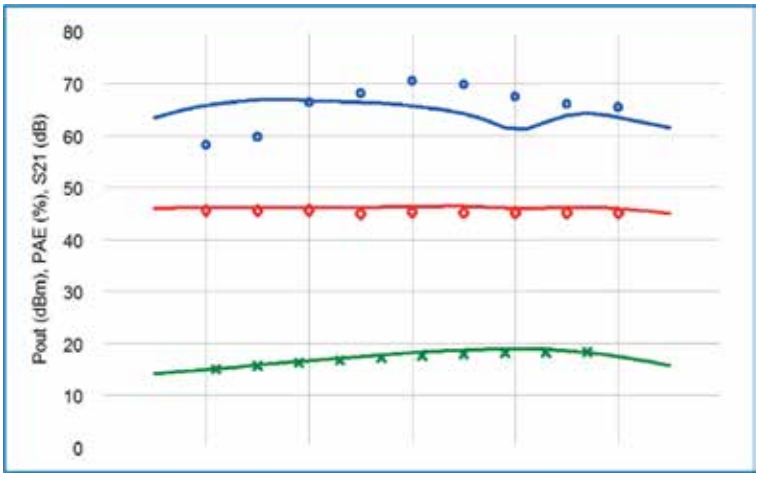

Figure 15: Simulated versus measured output power (red), PAE (blue), and S21 (green). Lines show simulated performance; symbols show measured data

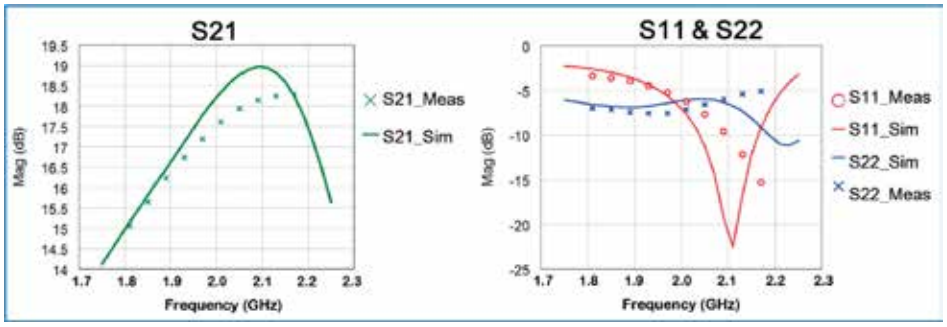

Figure 16: Simulated versus measured small signal S-Parameters

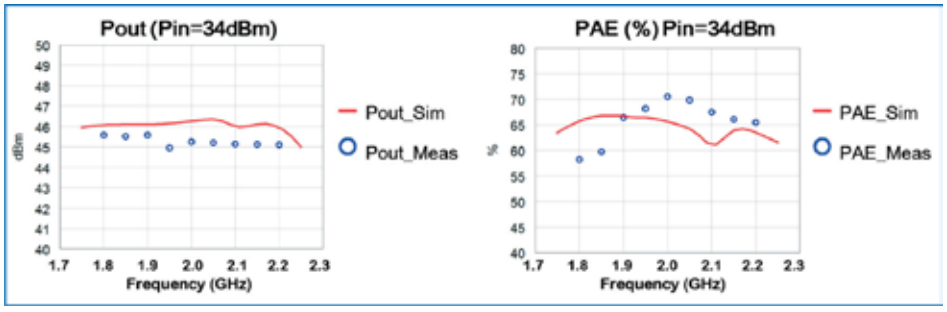

Figure 17: Simulated versus measured output power (left) and PAE (right)

described design process typically eliminates the need for optimization.

The final layout and design performance can be seen in Figures 11 and 12, respectively. Figure 13 shows the simulated intrinsic device channel voltage and current waveforms at 1.8 GHz, 2 GHz, and 2.2 GHz. It can be seen that the mode of operation of the final design is very close to Class-F across the required bandwidth. It could be claimed that the described method of design achieves an extended continuous Class-F mode of operation [1].

Measurement Results

The Class-F power amplifier design presented in the design flow above was built and tested. An image of the assembled amplifier can be seen in Figure 14. The measured results in Figures 15 – 18 are presented without any tuning. As evidenced by these figures, excellent measurement to simulation agreement was achieved without any on-the-bench tuning.

Although there was a small difference in simulated versus measured output power, this was to be expected, as in reality there would be slightly more losses in each element, the transistor would heat up, and the models of the transistor and any other component could not be perfect.

However, the difference in PAE was somewhat more substantial. In an attempt to resolve this discrepancy, a preliminary yield analysis was performed on capacitor part values in the output matching network (Figure 18). All capacitors were assigned a five percent tolerance. It was perceived from the yield analysis that some initial tuning could reduce, if not eliminate, the discrepancy in PAE.

Conclusion

This application note presented a streamlined practical design method for broadband high-efficiency RF power

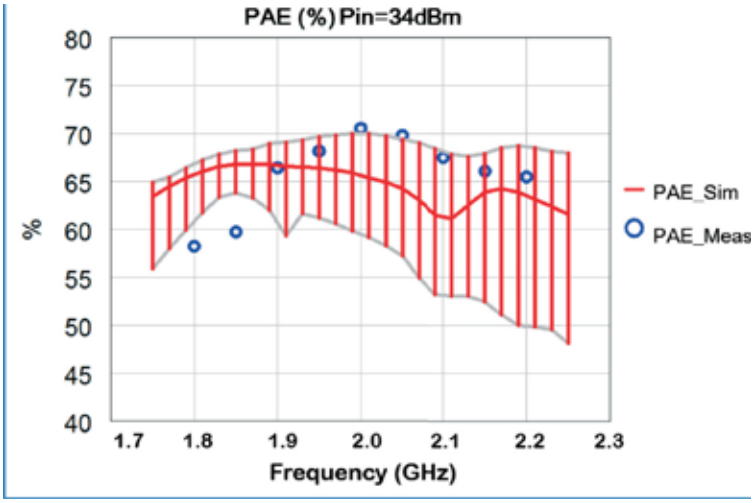

Figure 18: Results of a preliminary yield analysis showing the effect of part value tolerances on PAE. Performed with five per-cent tolerance on all capacitors in the output matching network

amplifiers. Using Microwave Office circuit design software and Modelithics transistor models with access to the reference planes at the intrinsic generator enabled a new approach in which the fundamental and harmonics impedances presented to the intrinsic current generator were pre-tuned before performing load-pull simulations. This shortened the process of extracting the fundamental and harmonic impedances to obtain the desired performance.

The efficiency and creativity of the design process was also improved by using the ADW tool available in Microwave Office, which provided many levels of automation to reduce the amount of time required to create and manipulate the schematics and layouts.

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The xPaaS Revolution and the Rise of BizDevOps

› Mike Piech, Red Hat

Platform-as-a-service, or PaaS, is an increasingly popular cloud offering that enables developers and IT operations professionals to build and maintain applications while avoiding many infrastructure-related challenges and expenses. According to a 2014 IDC report, the global PaaS market is expected to reach $20.3 billion in 2018 as enterprises continue to adopt this new technology.

Playing on "PaaS," Gartner coined the term xPaaS in 2013 to describe the broad spectrum of specialized middleware products that IT vendors offer as services, like integration Platform-as-a-service (iPaaS) or business process management Platform-as-a-service (bpmPaaS). xPaaS seizes the opportunity cloud computing provides to reimagine application development and operations, making these processes faster, easier, less risky, and more flexible.

Middleware meeting the cloud has facilitated the DevOps movement and predictably transformed how developers create applications and IT operations professionals manage them. But enterprise IT is only starting to experience the xPaaS revolution's most surprising and exciting consequence as line of business managers become more closely involved in the software development process than ever before. The rise of "BizDevOps" is leading not only to tighter collaboration between IT departments and business managers, but also to heightened expectations, with businesses increasingly relying on technology to carve out unique competitive advantages.

Accelerating time to market

One major benefit of xPaaS is accelerating applications' time to market. Innovation demands the ability to experiment, fail fast, and deliver before the competition. Developers must be free to focus on their applications, unhampered by the need to provision, configure, and secure their application infrastructure. IT operations can't take on even more maintenance responsibilities, especially when many stacks deployed for the sake of rapid innovation may be extremely short lived. Architects need to provide an environment that maximizes productivity, minimizes cost and risk, and scales rapidly and securely.

The last generation of application platforms, integration buses, and process automation suites, while an improvement over earlier home-grown solutions, fell short of delivering critical functionality on-demand without the need to acquire, provision, and maintain application infrastructure. xPaaS automates tedious tasks like setup, configuration, and integration. Traditionally, developers performed each of these functions for each middleware product manually—a time-consuming, error-prone process. To communicate with the database, for example, developers needed to obtain a connection string in one place and input it into a configuration file somewhere else. With xPaaS, intuitive menus help developers select their database and get their systems up and running quickly.

xPaaS also speeds time to market by accelerating trial and error. Engineers and architects can often approach development problems in multiple ways, several of which may appear equally viable, leaving teams uncertain of which to choose. Instead of having to sit and envision every scenario before writing a single line of code, developers working in an xPaaS environment can simply try different solutions and find out which works best.

Reducing risk

The same xPaaS features that accelerate time to market also reduce development and deployment risk. An intuitive GUI presents the simple logic of the situation and automates the complex, underlying processes, shielding applications from a major source of risk: human error. xPaaS takes advantage of the fact that computers are better at repeatedly executing tedious tasks, which frees up humans to focus on what they're better at: higher-level logic, thinking, and creativity.

xPaaS also de-risks the delicate transition from development to production. In the past, developers would cobble together an intricate and fragile environment on their workstations, miraculously get their application running, and the moment they needed to recreate that environment on the way to production, forget how they built it—which versions of which modules they used, for example. But for developers working in an xPaaS environment, replication is much easier, partly because the platform built the environment automatically, and partly because the platform consistently documents and audits the steps that go into creating the application. Once developers build an application using xPaaS, the underlying machinery can produce however many instances are needed.

Improving flexibility

Microservices and containers are the latest in a long line of technology that has catalyzed the xPaaS revolution and improved IT organizations' flexibility.

Containers allow developers to decompose applications into a greater number of smaller modules, or microservices. Before containers, a cloud-based module had to run on a full virtual server, a heavyweight operating system, and all the virtual hardware underneath. In those days, it didn't make sense for developers to place only a few lines of code on a virtual server. Now, using lighter weight containers, developers can run microservices on commensurately small infrastructures. At the same time, xPaaS has made deploying and maintaining a proliferation of microservices tractable.

By breaking down applications into loosely-coupled microservices, developers and IT operations professionals gain the ability to create, modify, restart, and scale each microservice independently. If a particular microservice becomes a performance bottleneck, for example, operations can scale it without scaling the whole application along with it. In the xPaaS world, IT organizations can improve their flexibility by thoughtfully employing containers and microservices.

BizDevOps: the new relationship between development, operations, and business

The xPaaS revolution is fueling the rise of DevOps, the increasingly popular software development methodology that emphasizes collaboration between developers ("Dev") and IT operations ("Ops"). Developers used to create applications independently in their own environment. After a certain point, they threw applications over the wall to operations, who had to figure out how to install them, configure them, and make them work in a real production environment. The DevOps movement is making developers and IT operations professionals work more closely together. As a result, developers are more aware of applications' operational attributes, which reduces the risk of operational errors. The developer's role has shifted. In exchange for the speed gains associated with working in an xPaaS environment, developers now have to complete many infrastructure-related tasks previously performed by operations. Of course, operations still has a role running and managing applications.

But the most surprising and exciting aspect of the xPaaS revolution is that business people are starting to collaborate more closely with their IT organizations in creating new applications. With the waterfall model, business people used to imagine a new application, write a detailed spec, throw it over the wall to development, wait a year or more, and then receive an application that might or might not turn out to be what they needed. In the world of xPaaS, business people can conceive of new applications in a more iterative, trial-and-error fashion. Developers can quickly create draft applications to show business people, who can give immediate feedback or launch the applications and see how customers respond. Enabling more trial and error on the business front is perhaps the greatest value of xPaaS. In the beginning, there were three siloed groups: development, operations, and business. Then came DevOps, which improved cooperation between development and operations. Now the prevailing development model won't be DevOps, but BizDevOps, and all three groups—development, operations, and business—can collaborate and iterate more tightly, creating better outcomes for all.

BizDevOps is a new term, but in practice, it's already here. The sooner enterprises take advantage of the tighter collaboration between developers, IT operations professionals, and business people that the xPaaS revolution has facilitated, the greater their competitive rewards will be.

Driverless-vehicle options now include scooters

Self-driving scooter demonstrated at MIT complements autonomous golf carts and city cars.

At MIT's 2016 Open House last spring, more than 100 visitors took rides on an autonomous mobility scooter in a trial of software designed by researchers from MIT's Computer Science and Artificial Intelligence Laboratory (CSAIL), the National University of Singapore, and the Singapore-MIT Alliance for Research and Technology (SMART).

The researchers had previously used the same sensor configuration and software in trials of autonomous cars and golf carts, so the new trial completes the demonstration of a comprehensive autonomous mobility system. A mobility-impaired user could, in principle, use a scooter to get down the hall and through the lobby of an apartment building, take a golf cart across the building's parking lot, and pick up an autonomous car on the public roads.

The new trial establishes that the researchers' control algorithms work indoors as well as out. "We were testing them in tighter spaces," says Scott Pendleton, a graduate student in mechanical engineering at the National University of Singapore (NUS) and a research fellow at SMART. "One of the spaces that we tested in was the Infinite Corridor of MIT, which is a very difficult localization problem, being a long corridor without very many distinctive features. You can lose your place along the corridor. But our algorithms proved to work very well in this new environment."

The researchers' system includes several layers of software: low-level control algorithms that enable a vehicle to respond immediately to changes in its environment, such as a pedestrian darting across its path; route-planning algorithms; localization algorithms that the vehicle uses to determine its location on a map; map-building algorithms that it uses to construct the map in the first place; a scheduling algorithm that allocates fleet resources; and an online booking system that allows users to schedule rides.

Uniformity

Using the same control algorithms for all types of vehicles — scooters, golf carts, and city cars — has several advantages. One is that it becomes much more practical to perform reliable analyses of the system's overall performance.

"If you have a uniform system where all the algorithms

are the same, the complexity is much lower than if you have a heterogeneous system where each vehicle does something different," says Daniela Rus, the Andrew and Erna Viterbi Professor of Electrical Engineering and Computer Science at MIT and one of the project's leaders. "That's useful for verifying that this multilayer complexity is correct."

Furthermore, with software uniformity, information that one vehicle acquires can easily be transferred to another. Before the scooter was shipped to MIT, for instance, it was tested in Singapore, where it used maps that had been created by the autonomous golf cart.

Similarly, says Marcelo Ang, an associate professor of mechanical engineering at NUS who co-leads the project with Rus, in ongoing work the researchers are equipping their vehicles with machine-learning systems, so that interactions with the environment will improve the performance of their navigation and control algorithms. "Once you have a better driver, you can easily transplant that to another vehicle," says Ang. "That's the same across different platforms."

Finally, software uniformity means that the scheduling algorithm has more flexibility in its allocation of system resources. If an autonomous golf cart isn't available to take a user across a public park, a scooter could fill in; if a city car isn't available for a short trip on back roads, a golf cart might be.

"I can see its usefulness in large indoor shopping malls and amusement parks to take [mobility-impaired] people from one spot to another," says Dan Ding, an associate professor of rehabilitation science and technology at the University of Pittsburgh, about the system.

Changing perceptions

The scooter trial at MIT also demonstrated the ease with which the researchers could deploy their modular hardware and software system in a new context. "It's extraordinary to me, because it's a project that the team conducted in about two months," Rus says. MIT's Open House was at the end of April, and "the scooter didn't exist on February 1st," Rus says.

The researchers described the design of the scooter system and the results of the trial in a paper they presented last week at the IEEE International Conference on Intelligent Transportation Systems. Joining Rus, Pendleton, and Ang on the paper are You Hong Eng, who leads the SMART autonomous-vehicle project, and four other researchers from both NUS and SMART.

The paper also reports the results of a short user survey that the researchers conducted during the trial. Before riding the scooter, users were asked how safe they considered autonomous vehicles to be, on a scale from one to five; after their rides, they were asked the same question again. Experience with the scooter brought the average safety score up, from 3.5 to 4.6.

NI Demonstrates Autonomous Vehicle Test Solutions

NI (Nasdaq: NATI), the provider of platform-based systems that enable engineers and scientists to solve the world's greatest engineering challenges, announced today new technology demonstrations of test solutions for the rapidly expanding autonomous vehicles market. These test solutions include all facets of vehicle design, verification and production, and will be on display at the Automotive Testing Expo (ATE) USA 2016 in Novi, Michigan, October 25–27.

Automotive companies today face increased testing challenges, exacerbated by the emergence of the connected car and semi- and fully-autonomous vehicles. Both OEMs and suppliers need flexible test systems that can quickly adapt to changing technologies and standards while also delivering a high-level starting point to speed up system implementation and deployment.

At ATE, NI will showcase the Advanced Driver Assistance Systems (ADAS) Radar Test Solution for performing RF measurements and target simulation for radar sensors; the HIL Simulator based on the new SLSC open architecture for switches, loads and signal conditioning; and the Direct Injector Control Module (DCM) for driving and controlling any type of injector.

- The ADAS Radar Test Solution combines NI's recently released PXIe-5840 second-generation vector signal transceiver (VST) with banded, frequency-specific upconverters and downconverters designed to test the 76–81 GHz radar band with 1 GHz of real-time bandwidth. Engineers can program the VST's FPGA with LabVIEW to use the ADAS Test Solution for radar target emulation, in the range from 1 m to 250 m with a resolution of 10 cm.
- NI's HIL Simulators are built on open standards like PXI and SLSC, giving customers complete test coverage by taking advantage of a massive breadth of native I/O and signal conditioning that includes cameras and RF for testing automotive radar.
- The DCM is an integrated, turnkey test and measurement device. Built for injector research, validation and test, it gives customers the flexibility to control any engine and drive a large variety of injectors with complex control solutions and advanced injection profiles.

NI has also extended its platform with an ecosystem of industry-leading partners in the connected car and advanced vehicle technology space. Showcased in the NI booth this year will be Averna for infotainment test, Bloomy for battery management system test, Danlaw for V2X communication, IPG for ADAS simulation and test and Signal.X for in-vehicle noise and vibration analysis.

"From concept to production, NI smarter test solutions can help customers reduce cost across all stages of vehicle development and future proof their test systems against rapidly expanding test requirements," said Chad Chesney, vice president of data acquisition and embedded systems at NI. "Built on the modular platforms of LabVIEW, VeriStand and PXI, customers gain the cost benefits of commercial off-the-shelf tools and the breadth of measurement and control capabilities to help them maximize test coverage."

To see these demonstrations in person, visit NI's booth (#1000) at ATE USA 2016, or visit http://www.ni.com/en-us/innovations/automotive/ to learn more about NI HIL systems.

OptiMOS™ 5 150 V delivers a breakthrough reduction in on-state resistance and reverse recovery charge

Aiming at high efficiency designs and applications, Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) introduces the OptiMOS™ 5 150 V portfolio. This product family further expands the industry leading OptiMOS 5 generation of power MOSFETs. The new 150 V product family is especially optimized for high performance applications which require low charges, high power density and yet high ruggedness. It is an important contributor to Infineon's system solutions for low voltage drives, synchronous rectification in telecom rectifiers and brick converters as well as solar power optimizers.

Greener technologies

Infineon is constantly developing products which help to reduce the global CO 2 emissions by enabling high efficiency designs. OptiMOS 5 150 V contributes to this goal by decreasing the power consumption of telecommunication equipment or increasing the power and range of electric vehicles.

Compared to the next best alternative, OptiMOS 5 150 V offers a breakthrough reduction in on-state resistance R DS(on) of 25 percent in a SuperSO8 package and the FOM g is improved by up to 29 percent over the previous generation. Increased commutation ruggedness is provided by the ultra-low Q rr, which is 72 percent lower than the next best alternative in SuperSO8. An additional outstanding feature of this product family is an improved EMI behaviour.

TT Electronics' zero ohm link is perfect for compact designs

Electrically 'invisible' link for optional connection points on PCBs

Woking, UK, 13 October 2016 – TT Electronics, a global provider of engineered electronics for performance critical applications, today launched a zero ohm link designed for making optional connections on printed circuit board assemblies. The LRZ0603 offers the most compact 6A zero ohm link available in a surface mount ceramic chip format.

With target markets in the automotive, industrial and instrumentation sectors the link is aimed at designers of a wide range of products including power supplies, small motor or actuator drive systems and power management. The zero ohm link is used for making optional connecting points in a PCB, allowing a common PCB to be used for multiple product variants, saving on design time and inventory. The LRZ0603 can also be used as a crossover to simplify – and reduce the cost of – PCB design by reducing the number of layers needed.

The LRZ0603 features a high current rating of 6A in SMD 0603 size (1.6mm × 0.8mm) thus reducing the PCB area required for a high current link, enabling product miniaturisation. It is AEC-Q200 qualified, providing the assured reliability of an automotive grade component. The link's ultra-low residual resistance value is closer to the ideal zero ohm characteristic with negligible voltage drop and its low internal thermal impedance minimises heating in the assembly, improving reliability and reducing field failures.

TT Electronics' LRZ0603 is unique among thick film on ceramic zero ohm chips in using a copper material to achieve low residual resistance coupled with low internal thermal impedance. A thick film copper conductive element is screen printed on a 96% alumina substrate resulting in far higher current ratings for a given footprint. This new 0603 size has a similar rating to the leading competing 2512 size i.e. with approximately 16 times larger area, and a much higher current rating than competing parts of the same 0603 size. The LRZ0603 adds to and complements TT Electronics' existing LRZ product series that contains larger sizes – see http://www.ttelectronicsresistors.com/datasheets/LRZ.pdf.

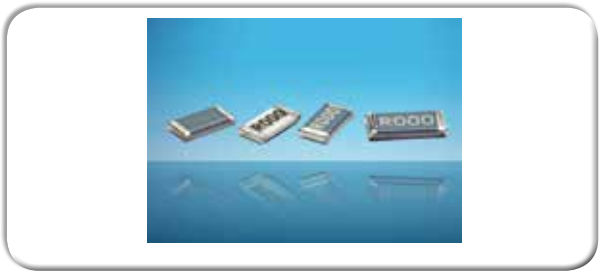
The LRZ0603's wrap-around copper terminations have an electroplated nickel barrier and solderable coating, which ensures excellent 'leach' resistance properties and solderability. Chips can withstand immersion in solder at 260°C for 30 seconds and are suitable for reflow or wave soldering processes.

Factors driving the demand for this type of product are the growth of electrical drives and actuators in industrial and automotive markets, and the increasing offer of multiple option product variants.

The LRZ0603 zero ohm link is available from the following distributors: Mouser, Newark, and Farnell. For other franchised distributors, please see http://www.ttelectronicsresistors.com/sales.php.

For sales or technical information, contact stephen.oxley@ttelectronics.com or visit http://www.ttelectronicsresistors.com.

For further information about TT Electronics visit http://www.ttelectronics.com



First dual-port CSI-2 quad deserializer hub enables faster, more flexible ADAS applications

TI deserializer hub aggregates and replicates data from multiple high-resolution sensors in automotive camera and radar applications

Texas Instruments (TI) (NASDAQ: TXN) today introduced the industry's first dual-port quad deserializer hub that is compliant with the MIPI Camera Serial Interface 2 (CSI-2) specification. The new automotive-qualified hub simultaneously aggregates and replicates high-resolution data from up to four cameras. High data throughput and precision are essential in autonomous driving and sensor fusion-based advanced driver assistance systems (ADAS), including surround-view systems, rearview cameras, driver-monitor cameras, camera-monitor systems, front camera systems and satellite radar equipment. For more information, see www.ti.com/DS90UB964q1-pr-eu.

The new device's higher bandwidth enables processing of more video data at faster speeds in equipment designed to recognize pedestrians, bicyclists and other obstacles in a vehicle's path or periphery. The DS90UB964-Q1 FPD-Link III device's dual CSI-2 outputs with virtual channel ID mapping and port replication save processor resources to speed processing of data from up to four cameras at 100 MHz per sensor and 12-bit resolution. In addition, TI's adaptive equalization (EQ) provides diagnostics that enable the system to monitor cable health and take action before cable failure occurs.

Key features and benefits of the new DS90UB964-Q1 quad deserializer hub

Faster video processing: Dual-port CSI-2 outputs support video transmission at up to 1.6 Gbps per lane for higher bandwidth and faster obstacle recognition by supporting the following:

- The second CSI-2 port enables simultaneous video replication for data logging, or separate viewing and machine-vision flows.
- The new hub, unlike competitive devices, supports virtual channel ID mapping which helps processors differentiate cameras and high-dynamic-range exposures, enabling more efficient processing.
- The ultra-low-latency control channel enables integration of the image signal processing (ISP) function into the electronic control unit (ECU), and out of the camera, improving image quality and reducing system costs.

Robust system operation and diagnostics: Like other devices in TI's growing FPD-Link III serializers-deserializer (SerDes) family, the DS90UB964-Q1 features adaptive receiver EQ rather than transmitter pre-emphasis. Adaptive EQ automatically compensates for cable aging and bending effects to ensure optimal signal quality, and helps reduce electromagnetic interference (EMI).

Cost-optimized, flexible system design: TI's broad portfolio of interoperable, upward- and downward-compatible FPD-Link III SerDes devices support automotive manufacturers and tier-1 suppliers' high-, mid- and entry-level performance configurations. This scalability makes it easy for designers to select and design in the best SerDes to optimize system performance and cost.

The DS90UB964-Q1 deserializer hub can work with many processors on the market today, including the TDA3x SoC processor for ADAS. The power-over-coax support in both devices enables engineers to significantly reduce the wiring needed in their systems.

In addition to the DS90UB964-Q1 1-megapixel (MP) deserializer hub, TI is now sampling SerDes devices for 2-MP cameras at 60 frames per second. These 2-MP devices feature synchronous clocking, and advanced data protection and diagnostic features.

Tools and support to speed design

Engineers can quickly and easily evaluate the new deserializer hub with the DS90UB964-Q1 evaluation module (DS90UB964-Q1EVM), available today for US$499 from the TI store and authorized distributors. Designers can also jump-start their system design using the new device with a TI Designs reference design. Check out the Automotive ADAS 4 Camera Hub Reference Design with Integrated ISP and DVP Outputs or Automotive 1MP Camera Module Reference Design with YUV422 Output, FPD-Link III and Power-over-Coax.

Package, availability and pricing

The DS90UB964-Q1 deserializer hub is now available in the TI store and with authorized distributors in a 64-pin very thin quad flat no-lead (VQFN) package. Pricing starts at US$15 in 1,000-unit quantities. Contact your TI field sales representative to sample TI's other new 1-MP and 2-MP SerDes devices.

Timing-Architects and Vector join Forces for Multi-core Development

Stuttgart and Regensburg, Germany, 2016-10-18 – Vector Informatik GmbH (Vector) of Stuttgart invests in Timing-Architects Embedded Systems GmbH (TA) of Regensburg. Together they now offer a complete tool chain for developing distributed multi-core real-time systems for Electronic Control Units (ECU) in vehicles. Vector is also enabling global sales of TA products.

Through this partnership, ECU developers and automotive OEMs will benefit from a universal tool solution. The multi-core capable AUTOSAR basic software MICROSAR and the Vector tools PREEvision, DaVinci Developer and DaVinci Configurator Pro are complemented by the TA Tool Suite from Timing-Architects. By this means, engineers get an innovative and comprehensive solution which lets them cover all phases of software development for real-time multi-core processors. Software integration into the ECU is simplified by architectural design, simulation, optimization and the evaluation of real-time data.

To intensify the already successful collaboration, Vector Informatik GmbH has acquired 49% of Timing-Architects Embedded Systems GmbH shares. Vector also supports worldwide sales of the TA Tool Suite and provides local technical expertise as well. This sales partnership, which has already been launched in the USA and Japan, will soon be extended to other countries. TA and Vector will still remain autonomous and independent companies.

Dr. Michael Deubzer, CEO of Timing-Architects, sees many advantages how software and functional developers will benefit from the partnership: "Due to their complexity, it is nearly impossible to develop networked multi-core systems without tool support. The real-time behavior of such systems can be validated by a combination of Vector and TA tools. Now, our partnership with Vector ensures easy and competent access to our tools for customers worldwide."

Dr. Thomas Beck, CEO of Vector Informatik GmbH, adds: "Today, our customers are already benefiting from a jointly developed interface for our tools, which can be used to analyze and optimize an AUTOSAR-conformant system configuration. Our two companies can now network this special knowledge even better to optimally tune our products to one another."

In the framework of the partnership, Vector and TA are already planning additional steps towards realizing efficient and productive automotive engineering.

In using the joint solution during development, first the AUTOSAR tools from Vector are used to describe the software components (SWCs) and create a preliminary draft of the ECU configuration. Engineers use PREEvision, DaVinci Developer and DaVinci Configurator Pro for this purpose. Then, the TA tools are used to analyze this configuration and make comparisons to time requirements. The best distribution of the SWCs to the cores and OS partitions is determined by simulation and optimization, and the configuration is then updated. The interplay of different ECUs is considered by simulating the network communication. Data is exchanged between the tools over an AUTOSAR-conformant file interface.

Due to their higher computing power, multi-core processors offer ideal conditions for innovative software applications in vehicles, such as for ADAS systems. However, when applications are running on multiple cores, runtime losses are incurred due to data communication between the cores. For time-critical applications, the challenge is to find an optimal distribution of the application software. With the joint solution from TA and Vector, the network of multi-core ECUs can now be analyzed and optimized consistently,

resulting in a reliable and efficient system. Completely in the sense of the vision of AUTOSAR, now developers will have new degrees of freedom in distributing software functions in real-time multi-core processors.
More information at: www.timing-architects.com and www.vector.com/autosar

Intersil Unveils 14-Channel Programmable Gamma Buffer for Infotainment and ADAS Displays

Automotive-grade ISL76534 delivers lowest power and highest accuracy gamma calibration to enable bright, high-contrast LCD displays

Intersil Corporation (NASDAQ: ISIL), a leading provider of innovative power management and precision analog solutions, today announced the industry's lowest power 14-channel programmable gamma buffer for automotive TFT-LCD displays. The automotive-grade ISL76534 delivers the highest accuracy gamma calibration to ensure consistent brightness and color matching of every LCD panel inside a vehicle. The ISL76534 is ideal for next generation LCDs designed for infotainment displays, advanced driver assistance system (ADAS) smart mirrors and instrument cluster displays.

The robust ISL76534 provides engineers with one Vcom and 14 gamma channels with 10-bit resolution for fine-tuning the gamma curve. LCD panels that are not properly gamma corrected often appear bleached out or too dark. Engineers employ the ISL76534 to calibrate and store the gamma curve, guaranteeing that each LCD powers up and displays eye-pleasing images. The ISL76534's internal EEPROM stores the factory-calibrated gamma and Vcom reference values, and enables significantly higher reliability than competitive devices by offering 10,000 write cycles and 20 years of data retention at 105°C.

The ISL76534 circuit architecture makes it easier to use than competitive solutions. No power-supply sequencing is required–either analog or digital power supplies can startup first. At initialization, all gamma buffer and Vcom output channels monotonically start up together in a controlled fashion preventing any possibility of an LCD panel lock-up. This adds another layer of reliability for ADAS and safety systems, such as backup cameras that rely on LCD panels to startup immediately and work flawlessly. In addition, the ISL76534's high 75 dB PSRR prevents power supply noise from reaching the gamma buffer outputs and becoming visible in the LCD panel.

The ISL76534 also provides the industry's lowest power consumption at 56.6mW, which is 5x lower than the closest competitor. Its low maximum output current for analog, digital, and Vcom supplies simplifies power supply and thermal design. The device's low power dissipation also eliminates the need for heatsinks, prevents junction temperature overheating, and allows engineers to use lower cost LDOs instead of switching regulators.

"Carmakers are continuing to leverage a variety of displays to enable new features in next generation vehicles," said Philip Chesley, senior vice president of Precision Products at Intersil. "Our 14-channel programmable gamma buffer ensures every vehicle's LCD panels offer consistent rich color and a uniform, visually appealing appearance drivers have come to expect from their electronics."

Key Features and Specifications of ISL76534

- I2C programmable, 15-channel reference voltage outputs

☐ 14-channel gamma references, 10-bit resolution, buffered outputs with 60mA Iout and 5V/µs slew rate

☐ 1-channel Vcom calibrator, 10-bit resolution, 100mA (max) Iout and 5V/µs slew rate

- Analog supply operating range from 6.3V to 19V
- Digital supply operating range from 2.25V to 3.6V
- Ultra-low power consumption of 56.6mW simplifies power supply and thermal design

☐ Analog AVDD max current of 2.5mA, amp AVDD max current of 1.2mA, and digital DVDD max current of 0.33mA

- Typical quiescent current power of 12mW at 8V
- High PSRR of 75dB typical at DC
- EEPROM data retention of 20 years at +105°C for

extreme robustness and reliability

- EEPROM endurance of 10,000 write cycles
- Over-temperature protection against excessive die temperature
- AEC-Q100 Grade-2 qualified for operation from -40°C to +105°C

System designers can create a complete TFT-LCD power supply by combining the ISL76534 with the ISL78419 TFT-LCD PMIC, ISL78206 40V 2.5A synchronous buck controller, and ISL78307 40V low Iq linear regulator. The ISL78171 6-channel, 50mA, LED backlight driver can be added to drive all infotainment and ADAS TFT-LCDs.

Pricing and Availability

The 14-channel ISL76534 programmable gamma buffer is available now in a compact 4.5mm x 5mm, 28-lead TQFN package and is priced at $1.99 USD in 1k quantities. An ISL76534EVAL1Z evaluation board can be purchased for $116.00 USD. For more information, please visit: http://www.intersil.com/products/isl76534.

e2v reveals the world's first K-band capable Digital-to-Analog Converter

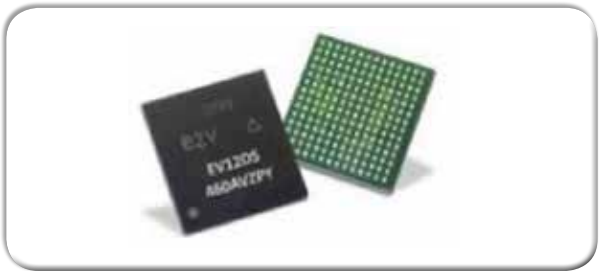
e2v announces the launch of the EV12DS460, a 6GSps Digital-to-Analog Converter (DAC) which can achieve clean signal generation up to 26.5GHz.

The new EV12DS460 from e2v is the world's first DAC to perform signal generation directly in the K-band frequency (18GHz-27GHz), removing the need for signal up-conversion and the costly mixers that perform this task. Radio Frequency (RF) applications operating at higher bands will benefit from system simplification through Size, Weight and Power (SWaP) savings, meeting growing demands to reduce the cost of system ownership.

With an ability to operate in the previously up-converted K-band frequency, the EV12DS460 contains the largest choice of DAC settings to optimize performance up to 26.5GHz. It is also equipped with four output operating modes and includes an option for program pulse shaping, making it proficient at handling the most specific of RF applications.

Laurent Monge, Vice President of Semiconductors at e2v, commented, "Removing up-conversion stages in our customers' systems operating up to K-band will help them to significantly simplify system design. We've always pushed the limits of signal conversion technology since developing the world's first microwave frequency capable data converter, and the EV12DS460 is evidence of this."

Each packaging option for the EV12DS460 guarantees dynamic performance across different temperature ranges, including military grade at -55°C to 125°C, offering a powerful and versatile data conversion solution.



Analog Devices' RS-485 Transceivers First to Meet Stringent IEC Surge Standards

Analog Devices, Inc. today announced the industry's first RS-485 transceivers fully certified for Level 4 EMC surge protection, thus eliminating the need for external transient-voltage surge-suppression devices. The galvanically isolated ADM2795E, using Analog Devices iCoupler® magnetic-isolation technology, and non-isolated ADM3095E save space and component count, speed time to market, and greatly minimize regulatory compliance issues. The integrated fault protection offered by the devices prevents potentially destructive voltages from damaging the communication interface, which can result from failures, surges, electrostatic discharge (ESD), and wiring errors.

View product pages, download data sheets, order samples and evaluation boards: http://www.analog.com/ADM2795E or http://www.analog.com/ADM3095E

Learn more about Analog Devices' iCoupler technology:

http://www.analog.com/icoupler

Connect with engineers and ADI product experts on EngineerZone®, an online technical support community: https://ez.analog.com/community/interface-isolation

Designers using the new RS-485 transceivers no longer need to individually design, test, verify, and formally obtain regulatory certification of their implementation, as these components have the required approval. Also, no external protective components are needed, which eliminates the need to match these discrete devices to the specific RS-485 transceivers users have selected. This also yields a simplified BOM and smaller-board space footprint for a higher density of RS-485 ports.

The ADM2795E and ADM3095E RS-485 transceivers meet IEC61000-4-5 Level 4 surge protection requirements, as well as industrial IEC immunity standards (radiated, conducted, and magnetic immunity) and EMC protection against ESD, electrical fast transient (EFT), and surge. Both devices are TIA/EIA RS-485/RS-422 compliant over their full supply range of 3 V to 5.5 V. In addition, the available evaluation boards, IBIS models, safety and regulatory compliance certificates, and videos and application notes available for the RS-485 transceivers greatly simplify the design-in process.

Critical specifications include:

5kV rms isolated RS-485/RS-422 transceiver (ADM2795E)

Certified IEC 61000-4-x immunity across isolation barrier (ADM2795E)

High common-mode transient immunity: >75 kV/µs (ADM2795E)

Certified Level 4 EMC Protection on RS-485 A, B Bus Pins

IEC61000-4-5 Surge Protection (±4 kV)

IEC61000-4-4 EFT Protection (±2 kV)

IEC61000-4-2 ESD protection

±8 kV Contact Discharge

±15 kV Air-Gap Discharge

IEC61000-4-6 conducted RF immunity (10 V/m rms)

RS-485 A, B pins human body model HBM ESD >±30 kV

±42V ac/dc peak Fault Protection on RS-485 bus pins

Extended common-mode input range of −25 V to +25 V

TIA/EIA RS-485/RS-422 compliant over full supply range and up to 125°C

TI unveils the industry's first single-chip 60-V eFuse with reverse polarity protection

Texas Instruments (TI) (NASDAQ: TXN) today introduced the first single-chip eFuse with back-to-back FETs, providing the industry's highest rating of protection at up to 60 V. Offering on-chip advanced features including reverse polarity protection and reverse current blocking, the TPS2660 is the most integrated eFuse on the power management market for 24-V and 48-V rail applications in industrial, automotive and communication infrastructure designs. For more details, see http://www.ti.com/TPS2660-pr-eu.tps2660_chip-shot_31oct16

Key features and benefits of the TPS2660 eFuse

• Integrated back-to-back FETs: The device's unique architecture equips the TPS2660 with the following:

o Enables reverse polarity protection to help guard the system load from miswiring, which can occur in industrial equipment that use screw terminals.

o Reverse current blocking prevents current from flowing backward from the output side to the input side.

o Advanced protection and integration reduce board space up to 40 percent by eliminating the need for external components.

• Adjustable overvoltage protection up to 60 V: Helps designers pass industry-standard surge-compliance tests more quickly and reliably, including the electrical fast transient (EFT) test.

Start designing now with the Input Protection and Backup Supply Design for 25W PLC Controller Unit, in which the LM5002 and LM5160 DC/DC converters provide backup power supply to meet International Electrotechnical Commission (IEC) 61000-4

specifications.

The TPS2660 is the newest addition to TI's portfolio of eFuses, providing protection against overvoltage, overcurrent and short-circuit events for applications. The portfolio encompasses protection devices for industrial, personal electronics, automotive and enterprise systems.

Pricing and availability

The eFuse is available now in the TI store and through the company's authorized distribution network. The TPS2660 comes in a 4.4-mm-by-5-mm thin shrink small outline package (TSSOP) and is priced at US$2.20 in 1,000-unit quantities.

SMD resistors from TT Electronics withstand high surge conditions New smaller footprint size saves space on PCBs and assemblies

– TT Electronics, a global provider of engineered electronics for performance critical applications, today launched two new ranges of SMD thick film chip resistors designed to optimise performance under pulse and surge conditions. With a value range of 1R0 to 1M0, the resistors provide surge protection in compact circuits where a small footprint size is critical to the design.

TT Electronics' PWC0603 and DSC0603 series are designed specifically to provide reliable operation under pulsed load conditions. For both the PWC and DSC ranges the 0603 size is a new smaller version that is being added to both series. DSC resistors are double sided while the PWC are single, otherwise most parameters and features are common to both ranges.

Aimed at designers of power supplies, circuit breakers, remote sensor interfaces, defibrillators, and indeed any circuit types where pulses or surges are possible, the resistors are particularly suited to applications in the industrial, medical and instrumentation sectors. They provide enhanced product reliability by protecting circuits against occasional surges that may be generated by load switching or lightning strikes close to power lines.

For a 100-microsecond pulse, PWC0603 will take 10W, and the double sided DSC version withstands 20W peak power, while for both types the surge withstanding is 1.2/50 microseconds up to 500V. These figures result in enhanced reliability and reduced field failures. In fact, TT Electronics' PWC0603 and DSC0603 offer a surge withstand performance exceeding that of competing parts. Further enhancing reliability, the resistors feature optional anti-sulphur terminations.

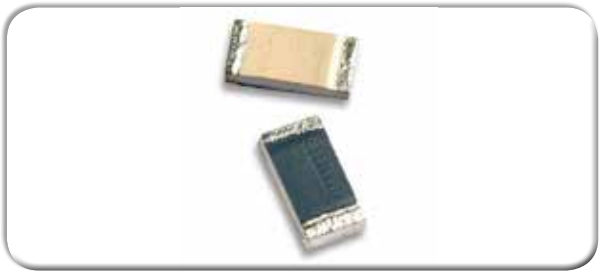
In developing and manufacturing the resistors, TT Electronics uses proprietary laser trimming techniques that help to spread the generated heat evenly over the surface of the component. In the case of the double sided DSC0603, the addition of a second resistor film on the underside ensures that heat is spread evenly on both sides of the component.

Factors driving the demand for this type of product include the increased sensitivity of modern electrical systems to damage from high-energy surges, and the demand for more compact components to allow miniaturisation of host equipments.

PWC0603 and DSC0603 series resistors are available from the following distributors: Mouser, Newark, and Farnell. For other franchised distributors, please see the 'Sales' tab at www.ttelectronics.com/resistors.

For sales or technical information, contact stephen.oxley@ttelectronics.com or visit www.ttelectronics.com/resistors.

For further information about TT Electronics visit www.ttelectronics.com.



Core Independent Peripherals Now Available on PIC18 Family

The PIC18F “K40” family of microcontrollers (MCUs) is now available from Microchip Technology Inc. (NASDAQ: MCHP), a leading provider of microcontroller, mixed-signal, analog and Flash-IP solutions. The family consists of 10 new devices ranging from 16-128 KB of Flash memory with package options covering 28-64 pins. These cost-optimized 8-bit MCUs are the first PIC18 product family to offer Microchip’s popular Core Independent Peripherals (CIPs).

CIPs provide developers with the ability to accomplish tasks in hardware while freeing up the CPU to do other tasks or go to sleep. This results in reduced power consumption, allows for deterministic response time, and decreases firmware development and validation time. The PIC18F “K40” features the ADC with Computation (ADC2) — an intelligent Analog-to-Digital Converter which, independent of the core, can control data acquisition and signal analysis functions required in sensor interface applications, such as capacitive touch sensing.

The addition of CIPs to the PIC18F “K40” builds upon the legacy of the successful PIC18F “K20” family. These new devices are cost effective and offer up to 128 KB of Flash, 5V operation, EEPROM and extensive peripheral integration. The devices include a full complement of Core Independent Peripherals for safety-critical applications (CRC/Memory Scan, Windowed Watchdog Timer, and Hardware Limit Timer), up to seven hardware PWMs and multiple communications interfaces. Additionally, the PIC18 “K40” family offers Intelligent Analog peripherals including Zero Cross Detect (ZCD), on-chip comparator and ADC2. The ADC2 handles the signal analysis functions of averaging, filtering, oversampling and automatic threshold comparison independent of the CPU. These devices are well suited for a broad range of applications and market segments including touch sensing, industrial control, consumer, automotive and Internet of Things (IoT).

“Microchip continues to expand our 8-bit portfolio with new on-chip peripherals for both the PIC® and AVR® architectures,” said Steve Drehobl, vice president of Microchip’s 8-bit MCU division. “The PIC18F ‘K40’ family combines large memories with the Core Independent Peripherals and Microchip’s MPLAB® Code Configurator (MCC) to significantly reduce product development time and improve system performance.”

For more information about the PIC18F “K40” family, visit http://www.microchip.com/K40

Development Support

The new PIC18F “K40” family is supported by the Curiosity High Pin Count (HPC) board and Microchip’s established software development platforms including MPLAB Code Configurator (MCC), MPLAB X IDE, XC8 Complier, and Microchip’s new cloud-based MPLAB Xpress IDE.

Pricing and Availability

The family is available in volume production and consists of 10 new devices ranging from 16-128 KB of Flash memory. Package options range from 28-64 pins and include UQFN (4 x 4 x 0.5 mm), QFN, SOIC, SSOP, TQFP, and DIP packages. Pricing begins at $0.83 in 10K unit quantities.

Highly Integrated AFE for Power Quality Monitoring Saves Significant Design Time and Cost Versus Custom Development

Analog Devices, Inc. (ADI) today introduced a highly integrated polyphase analog front end (AFE) with power quality analysis designed to help extend the health and life of industrial equipment while saving developers significant time and cost over custom solutions. Achieving extremely accurate, high-performance power quality monitoring typically requires customized development, which can be expensive and time-consuming. The ADE9000 AFE is an off-the-shelf solution with embedded power quality algorithms and integrated with high-performance analog-to-digital converters (ADCs) in one single device. This integration simplifies additional complex algorithm programming, reduces cost and component count, and increases speed to market while still achieving high accuracy and enabling EN61000-4-30 Class S for power quality. Equipment in factories, hospitals, commercial buildings, and other settings is often susceptible to service interruption, premature failure, and long-term damage caused by disturbances and variations in the power supply, known as pollution. In many cases, this pollution in the power supply

can go undetected before damaging expensive equipment. The ADE9000 AFE enables designers of power quality monitoring solutions to measure and analyze pollution in order to prevent these disruptions and long-term damage, primarily for three-phase power meters.

View product page, download data sheet, order samples and evaluation boards: http://www.analog.com/ADE9000

Learn about Analog Devices' energy measurement ICs portfolio: http://www.analog.com/en/products/analog-to-digital-converters/integrated-special-purpose-converters/energy-metering-ics.html

Read the product highlight to learn more about the ADE9000: http://www.analog.com/media/en/news-marketing-collateral/product-highlight/ADE9000-Product-Highlight.pdf

Connect with engineers and ADI product experts on EngineerZone®, an online technical support community: https://ez.analog.com/welcome

The ADE9000 AFE integrates seven high-performance ADCs, a high-end reference, a flexible digital signal processing (DSP) core, and proprietary algorithms into a single convenient device. High accuracy is driven by the ADCs and reference which provide low drift over temperature and the highest accuracy over the widest dynamic range. Pre-programmed proprietary power quality software provide real-time monitoring and harmonic analysis, including magnitude and phase information. This enables timely and cost-saving corrective action when necessary. For power system meter designers who do not require the advanced power quality features of the ADE9000, the ADE9078 energy metering AFE is available for polyphase utility grade meter applications.

Linear Technology Announces QML Class V Standard Microcircuit Drawings for Popular Radiation Hardened Components

Linear Technology Corporation today announced Qualified Manufacturer List (QML) Class V Standard Microcircuit Drawings (SMD) for some of the most widely used Radiation Hardened (RH) components. Part types now available to QML Class V are RH1013 and RH1014 op amps; RH1498 and RH1499 precision rail-to-rail op amps; and RH1009 and RH1021-10 voltage references. QML Class V components are intended for use in the most demanding space flight applications and must meet the performance, quality and reliability requirements defined in MIL-PRF-38535. By choosing QML Class V components, users are guaranteed that the component manufacturers' test methods and quality procedures meet the exacting standards of the U.S. Government Qualifying Activity program.

Consequently, the use of QML Class V components is preferred by spacecraft prime contractors. This can lower program costs by simplifying the procurement process, reducing component documentation, and may no longer require performance of destructive physical analysis using flight grade components. Compliance to Radiation Hardness Assurance (RHA) ensures that Linear Technology has performed Radiation Lot Acceptance Tests on each manufacturing lot, so manufacturers no longer need to commission their own Total Ionizing Dose testing, providing further cost and time savings.

Additional Linear Technology RH products are planned for release to QML Class V. For more information, pricing and availability for Linear's complete line of SMD, Rad Hard, Space and Military components, please contact your local sales office or ltcspace@linear.com.

e2v's new CMOS sensors feature the world's smallest true global shutter

ARM® e2v has launched its ground breaking new Emerald family of

Complementary Metal Oxide Semiconductor (CMOS) image sensors. This new product family features the world's smallest true global shutter pixel available on the market today (2.8µm). With a smaller optical format and higher resolutions, the new sensors lead to improved performance and reduced system costs for customers.

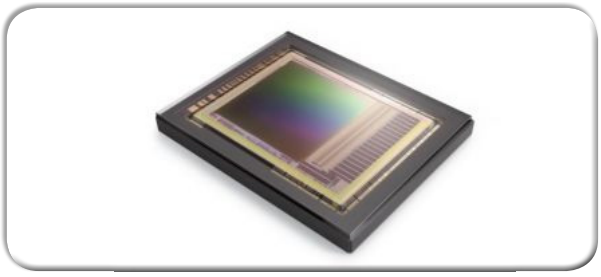
This new generation of image sensors marks a significant improvement of Dark Signal Non Uniformity (DSNU), that is 10 times improved when compared to other CMOS products. This allows cameras to perform better in high temperatures and enables long exposures to be used in low-light applications such as microscopes or outdoor cameras for surveillance, speed and traffic applications.

e2v's Emerald family comprises a 16MP (4096 x 4096 pixels), which is the first to be released, a 12MP (4096 x 3072 pixels) and a 8MP (4096 x 2160 pixels). These high resolution formats are a world first and include a one inch optical format, which can be interfaced with a compact C Mount lens. This innovation makes the new sensors ideal for a wide range of industrial applications.

The whole Emerald family features the same pixel, processing, readout structures and ceramic Land Grid Array (LGA) package to simplify integration, helping to lower development costs for camera makers. The new products have dedicated embedded features including High Dynamic Range (HDR) modes, 8/10/12 bit Analog to Digital Converters (ADCs), modulable high speed outputs (60fps at 10 bits, full 16MP resolution), and a number of convenient power saving modes. These impressive features are the result of e2v working closely with customers to anticipate their future needs and to address the growing trends of the machine vision market.

Gareth Powell, Marketing Manager for Professional Imaging at e2v, said, "Our new Emerald sensors use advanced CMOS image process technology and pixel design to offer a low noise global shutter pixel, with an electro-optical performance tuned to meet the demanding requirements of the machine vision industry. The sensors deliver Quantum Efficiency of more than 65%, a full well capacity of over 7ke, a typical temporal noise of 4e- and a new low-noise mode to offer typically around 2e-."

The new sensors will be showcased for the first time at Vision, Stuttgart 2016. New and existing customers should contact e2v prior to the show to reserve an exclusive technology demonstration.



AURIX™ microcontroller TC3xx family of Infineon fuels automated driving and electromobility

Serving the requirements of automated cars and electric vehicles Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) today launched the next generation of its AURIX™ microcontroller family. The TC3xx microcontrollers offer the highest level of integration on the market and real-time performance that is three times higher than that available today.

With its high-performing hexa-core architecture and its advanced features for connectivity, security and embedded safety, the AURIX family TC3xx is ideally suited for a wide field of automotive applications. In addition to engine management and transmission control, powertrain applications include new systems in electrical and hybrid drives. Specifically hybrid domain control, inverter control, battery management, and DC-DC converters will benefit from the new architecture. The AURIX TC3xx microcontrollers are well-suited to safety-critical applications ranging from airbag, braking and power steering to sensor-based systems using radar or camera technologies. The combination of performance and a powerful safety architecture makes the TC3xx family ideal for domain control and data fusion applications supporting the next levels towards automated driving.

"The AURIX TC3xx family will advance the automated and electrical car," said Peter Schaefer, Vice President and General Manager, Microcontrollers at Infineon. "We are proud to introduce our next generation of high-performing TriCore-based microcontrollers that set new performance standards and offer the right mix in performance, security and safety to meet ISO 26262 ASIL-D system requirements."

AURIX™ TC3xx for a plus in performance, connectivity and security

The AURIX TC3xx family will be highly scalable and offer Flash memory sizes of up to 16 MByte and more than 6 MByte of integrated RAM. Compared to today's AURIX TC2xx microcontrollers with up to three TriCore™ cores, the TC3xx multicore architecture provides up to six TriCore cores, each with a full clock frequency of 300 MHz. Four of the six cores feature an additional lockstep core enabling a new level of ISO 26262 functional safe computational power on a single integrated device: Up to 2400 DMIPS performance supporting applications classified ASIL-D, compared to up to 740 DMIPS with the previous AURIX architecture.

The performance increase and the reuse of existing safety concepts allow automotive system suppliers to reduce development costs by 20 percent and improve time-to-market. Also, more functions can now be implemented on a single microcontroller, such as powertrain and chassis domain control and next generation radar and fusion algorithms.

Automotive radar systems ranging from blindspot monitoring to advanced front radar specifically benefit from the capabilities of the AURIX TC3xx family. TC3xx microcontrollers will feature a radar processing sub-system with up to two dedicated Signal Processing Units running at 300 MHz enabling computation of next-generation radar algorithms on a single chip. In addition, radar chips can be seamlessly connected to AURIX via a high-speed digital radar interface.

AURIX TC3xx does not compromise on security. A new version of the programmable Hardware Security Module (HSM) is available across the family: it supports to better secure on-board communications and to prevent hardware manipulation, such as motor tuning. New asymmetric cryptography accelerators are integrated into the HSM hardware that helps to achieve full EVITA support. The AURIX TC3xx facilitates fast software-over-the-air updates to protect against software hijacking.

As a host controller in gateway and telematics applications, AURIX TC3xx microcontrollers support the latest communications interfaces. They feature a Gigabit Ethernet interface, up to 12 CAN-FD channels compliant to ISO11898-1 and up to 24 LIN channels. An additional eMMC interface for external Flash interfacing enables local data storage supporting software-over-the-air update concepts.

Availability

The second generation AURIX TC3xx family is compatible with the previous AURIX TC2xx generation. Engineering samples of the 300 MHz lead device, the TC39xx, with 16 Mbyte of embedded Flash will be available in BGA-516 package and BGA-292. General sampling is scheduled to start in the first quarter of 2017. Qualification of the first product is planned in the first quarter of 2019.

Industry First Intelligent Charge Controller from ON Semiconductor Meets the Exacting Demands of Next Generation Power Banks

ON Semiconductor (Nasdaq: ON), driving energy efficient innovations, has introduced a highly integrated single chip power bank solution for the development of next generation Li-Ion powered products. The LC709501F total Li-Ion battery solution offers broad power and voltage/current output range of 5 volt (V), 9 V and 12 V operation, with a maximum charge/discharge capability of up to 30 watts (W) through simple FET selection.

The LC709501F determines what type of device is connected and automatically selects the fastest available method for charging. Advanced users can even reprogram the LC709501F to support custom charge/discharge profiles, as well as USB Type-C and PD Policy Engine functions. This single-chip solution includes integrated fuel gauge function, configurable I/O, LED drivers, I2C interface, and pre-drivers for external power MOSFETs, providing system flexibility. A design reference kit is available to realize fast time to market. The LC709501F supports various output power levels up to 30 W, by changing external MOSFETs. In addition, there is an integrated USB 2.0 Full Speed host controller.

The LC709501F's USB host controller supports

connectivity with iOS and Android apps that enable the device to communicate with the connected smartphone and subsequently make use of its display to show information concerning the battery health and the charging process (charging time, battery life, number of charging cycles completed, etc.). The device works with the proprietary charging protocols (such as Fast Charge and Qualcomm® Quick Charge™) now being utilized by smartphone manufacturers to accelerate the charging period. To ensure operational longevity, over-current, over-voltage, and redundant battery protection mechanisms are all included, as well as a thermistor for monitoring of temperature levels. The LC709501F supports an operational temperature range of -40 °C to +85 °C.

"With a growing need for on-the-go recharging of portable electronics, power banks are certain to become more prevalent over the coming years," states Matthew Tyler, Director Strategy and Product Roadmap Definition of the Digital and DC/DC Division at ON Semiconductor. "Accurate and reliable charge capacity indication and the ability to support the latest quick charging standards are becoming more critical, especially as power bank capacities have grown over time. The level of sophistication that power banks possess is destined to increase, so that batteries can be replenished as quickly as possible and inconvenience is minimized. The new, best-in-class LC709501F charger will enable the creation of compact, highly efficient, feature-rich power banks that will simplify and accelerate time-to-market of next generation power bank solutions. Its breadth of functionality will enhance the user experience and mean that high degrees of safety are maintained."

Packaging and Pricing The LC709501F is offered in a QFN-52 (6 x 6 mm) package and priced at $2.80 per unit in 10,000 unit quantities.

New Line of USB 2.0 and 3.0 Connectors Expands CUI's Interconnect Portfolio

CUI's Components Group today announced an expansion to its existing portfolio of power, audio and signal connectors with the addition of a USB product line. The new connector family incorporates USB 2.0 and 3.0 connectors available in Type A, Type B, Micro AB, Micro B, Mini AB and Mini B USB versions. Able to support data rates up to 5 Gbps in USB 3.0 models, the new product family is ideal for a variety of I/O applications in consumer and portable electronic devices, including mobile computing equipment, digital audio devices and high volume storage products.

Offered in jack or plug connector types with horizontal or vertical orientations depending on the model, the new USB line boasts a number of mounting styles including surface mount, cable mount, mid mount SMT and through hole, allowing them to plug into virtually any design.

All models feature a voltage rating of 30 Vac, current ratings of 1 or 1.8 A and reliability as high as 10,000 mating cycles for specific models. Color insulator options of black, blue and white are also offered. The USB connectors also feature an operating temperature range of -25 to 85°C and RoHS compliance.

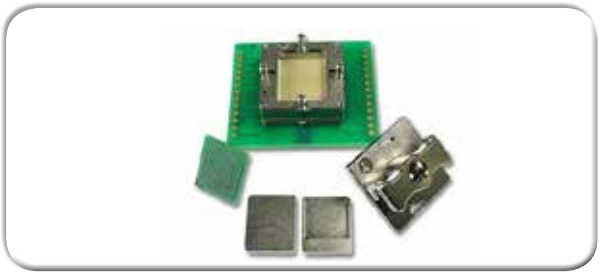
The entire product line of USB connectors are available immediately through distribution with prices starting at $0.23 per unit at 1500 pieces. Please contact CUI for OEM pricing. http://www.cui.com/contact

Stamped Spring Pin Socket for 0.65mm pitch NXP's RCPBGA

Ironwood Electronics recently introduced a new socket

addressing high performance requirements for Burn-in and Test applications – SBT-BGA-6538. The contactor is a stamped spring pin with 31 gram actuation force per ball and cycle life of 125,000 insertions. The self inductance of the contactor is 0.88 nH, insertion loss of < 1 dB at 15.7 GHz and capacitance 0.097pF. The current capacity of each contactor is 4 amps at 80C temperature rise. Socket temperature range is -55C to +180C. Socket features a floating guide for precise ball to pin alignment. Socket also includes additional floating compression plate that has a cavity to accommodate PoP devices. The specific configuration of the package to be tested in the SBT-BGA-6538 is BGA, 14x17mm body size, 0.65mm pitch and 20×25 ball array. To use, drop IC into the socket, place floating compression plate, swivel the lid, and apply down force using compression screw. This socket can be used for hand test and quick turn custom burn-in applications with the most stringent requirements.

Pricing for the SBT-BGA-6538 is $811 at qty 1 with reduced pricing available depending on quantity required.



TI's new USB Type-C™ and Power Delivery 3.0 devices improve power and data transfer, signal quality, and circuit protection

Expanding the industry's most comprehensive portfolio of USB-compliant integrated circuits (ICs), Texas Instruments (TI) (NASDAQ: TXN) today introduced five new USB Type-C and Power Delivery (PD) devices that enable engineers to design USB Type-C electronics with better signal quality and protection against system damage.

The TUSB1046 family of linear redrivers is the industry's first to support 10G USB data and DisplayPort™ 1.4 video transfer, enabling faster transmission without signal integrity degradation. To prevent hard field failure, the TPD8S300 family includes the industry's first single-chip solution to protect USB Type-C and PD systems from overvoltage damage. Additionally, the new TPS65983B USB PD 3.0 controller enables a complete system design and more reliable power and data transfer with integrated power path, fast role swap hardware, authentication support and standardized voltages. For more information, see www.ti.com/usbtypecpd2016-pr-eu.

Faster data and video transfer

The new TUSB1046 and TUSB1002 redrivers support twice the data bandwidth of current 5G USB solutions, enabling 10G data and video transfer with up to 8K resolution, while consuming only 335 mW of active power at 10G USB speeds. The redrivers compensate channel loss up to 14.4 dB when transmitted over long traces and cables. Additionally, 16 equalization levels optimize performance by compensating intersymbol interference jitter and signal attenuation, enabling better interoperability and connectivity with other devices. TI's 10G linear redriver family is pin-to-pin compatible with TI's family of 5G USB devices, enabling seamless speed upgrades in existing designs.

Overvoltage port protection

Using up to 75 percent less board space than a discrete implementation, the TPD8S300 and TPD6S300 devices protect against overvoltage damage caused by a DC short to the 20-V bus voltage (Vbus) on the configuration channel (CC) and sideband use (SBU) pins, while maintaining signal integrity. The port protectors integrate transient voltage suppression (TVS) diodes with low-clamping performance to provide International Electrotechnical Commission (IEC) 61000-4-2 electrostatic discharge protection (ESD) and protect the downstream PD controller.

Fully managed power path

The TPS65983B single-chip device is the only USB PD 3.0 controller that fully integrates the power path, while providing overcurrent, overvoltage, reverse current and thermal protection. The controller features fast role swap for sink or source implementations to give designers maximum flexibility.

Enabling compliance of the latest USB standards

These devices comply with the new USB Type-C, USB 3.1 Gen 2 and PD 3.0 standards, increasing reliability over previous specifications and enabling slim design, robust power delivery, and the use of universal connectors and cables. Additionally, these power, signal-chain and circuit-protection devices allow USB Type-C and PD systems to function seamlessly together, giving designers peace of mind.

Package, availability and pricing

TI's new USB Type-C and PD devices are available with package and pricing as listed in the table below. The TUSB1002, TUSB1046 and TPS65983B devices are available in production quantities from the TI store and authorized distributors. Prototype samples are available for the TPD8S300 and TPD6S300 protection devices through TI.com and authorized distributors. Additionally, evaluation modules (EVMs) are available to help engineers quickly and easily evaluate performance and speed time to market.

CUI Introduces High Performance Dc Fan Line to Bolster Thermal Management Portfolio

CUI's Components Group today announced the addition of a high performance dc fan line to its existing thermal management portfolio. The CFM series with frame sizes of 40, 50, 60, 70, 80, 92 and 120 mm delivers airflow ranging from 10 CFM in the 40 mm series to over 200 CFM in the 120 mm series.

Available with rated voltages of 5, 12, 24 and 48 Vdc, all dc fans feature dual ball bearing construction for maximum reliability and come as standard with auto restart protection. Static pressure values for the CFM series range from 2.79 up to 19.8 mm H2O with low rated currents from 0.1 to 1.4 A. Options for tachometer signal, rotation detector and PWM control signal are also available depending upon the model.

The CFM series also carries UL/cUL 507 and TUV (EN 60950-1) safety approvals while complying with EN55022 Class B limits for conducted and radiated emissions. All models are RoHS compliant.

Thanks to their variety of frame sizes and superior airflow, CUI's line of dc fans are the ideal cooling solution for IT and telecommunications equipment, medical devices and industrial applications.

The entire CFM series is available immediately through distribution with prices starting at $6.17 per unit at 100 pieces. Please contact CUI for OEM pricing.

Visit CUI's booth (Power Hall A2, Booth 613) at electronica 2016 where the company will be showcasing the new CFM series and the rest of their thermal management products as well as their power supply portfolio ranging from 1 W to 12,000 W. electronica is the world's leading trade fair for electronic components, systems and applications, and will be held at the Messe München in Munich, Germany from November 8-11, 2016.

Intersil Expands Single-Chip USB-C Buck-Boost Battery Charger Family

Intersil Corporation (NASDAQ: ISIL), a leading provider of innovative power management and precision analog solutions, today introduced two new USB-C™ buck-boost battery chargers that support bidirectional power delivery in ultrabooks, tablets, power banks and other mobile products. The single-chip ISL9238 and ISL9238A battery chargers replace competitive two-chip solutions to reduce customer bill of materials (BOM) costs by up to 40%. Both ICs employ Intersil's patented

R3™ modulation technology to extend battery life and deliver acoustic noise-free operation, superior light-load efficiency and ultra-fast transient response.

The ISL9238 and ISL9238A operate in forward buck, boost or buck-boost mode to fast charge mobile battery packs with up to 4-cell Li-ion batteries. They also support USB 3.1 On-The-Go (OTG) with 5V/20V reverse buck, boost or buck-boost mode to deliver power out of a USB-C port for charging external devices such as smartphones, headphones or virtual reality goggles. At maximum power, both ICs provide 20V at 5A to the USB-C port for delivery of power up to 100W over a reversible USB Type-C connector cable. The ISL9238A features the same capabilities as the ISL9238, but also includes a different SMBus address for OEMs that want to use both ICs to design systems with dual USB-C ports.

In charging mode, the ISL9238 and ISL9238A take input power from a wide range of DC power sources, including AC/DC charger adapters, USB power delivery (PD) ports and any travel adapter. Both chargers include SMBus and I2C programmable features such as depleted battery trickle charging, and a two-level adapter current limit for turbo-mode events where the charger takes advantage of the adapter's milliseconds of surge current capability to minimize power draw and extend battery run-time. The ISL9238 and ISL9238A also feature programmable autonomous charging and an end of charge safety timer to stop battery charging.

"The new ISL9238/A USB-C buck-boost battery chargers give our customers more features, including 5V/20V reverse buck, boost and buck-boost modes, and the ability to add dual ports for two USB-C battery chargers in one system," said Andrew Cowell, senior vice president of Mobile Power Products at Intersil. "Mobile computing OEMs rely on Intersil to consistently deliver power management innovations that help them differentiate their products with thinner form factors and exceptionally long battery life."

The ISL9238 and ISL9238A are pin-compatible with the ISL9237 USB-C battery charger and join Intersil's family of mobile computing power management solutions, including the ISL95852 Vcore PMIC, ISL95908 peripheral PMIC, and discrete PWM controllers (ISL95853/54/55/57). These ICs power IMVP8-compliant mobile systems using 6th and 7th Gen Intel® Core™ processors.

Key Features and Specifications of ISL9238 and ISL9238A

- Buck-boost NVDC charger for 1-, 2-, 3-, or 4-cell Li-ion batteries
- Input voltage range of 3.2V to 23.4V (no dead-zone)
- System output voltage of 2.4V to 18.304V
- Up to 1MHz operation allows use of smaller, lower cost inductors and automatically reduces switching frequency with no audible acoustic noise when charger is in DCM mode
- ASGATE FET control: actively controls inrush current to prevent FET damage
- Low-power and high-power LDO outputs tie to VDD pin to provide bias power and MOSFET gate drive power
- Compliant with Intel PROCHOT# and PSYS for protection against battery voltage drop, adapter over-current, battery over-current and overheat
- Allows trickle charging of depleted battery
- Autonomous charging option provides end of charge control using safety timer to stop battery charging
- SMBus/I2C programmable limit settings with adapter current monitor (AMON) and battery discharging current monitor (BMON)
- Battery learn mode calibrates the battery fuel gauge
- ISL9238A includes a different SMBus address to support charging a second battery

Pricing and Availability

The ISL9238 and ISL9238A buck-boost battery chargers are available now and priced at $3.50 USD in 1k quantities. Both battery chargers are supplied in 4mm x 4mm, 32-lead TQFN packages. For more information, please visit www.intersil.com/products/isl9238.

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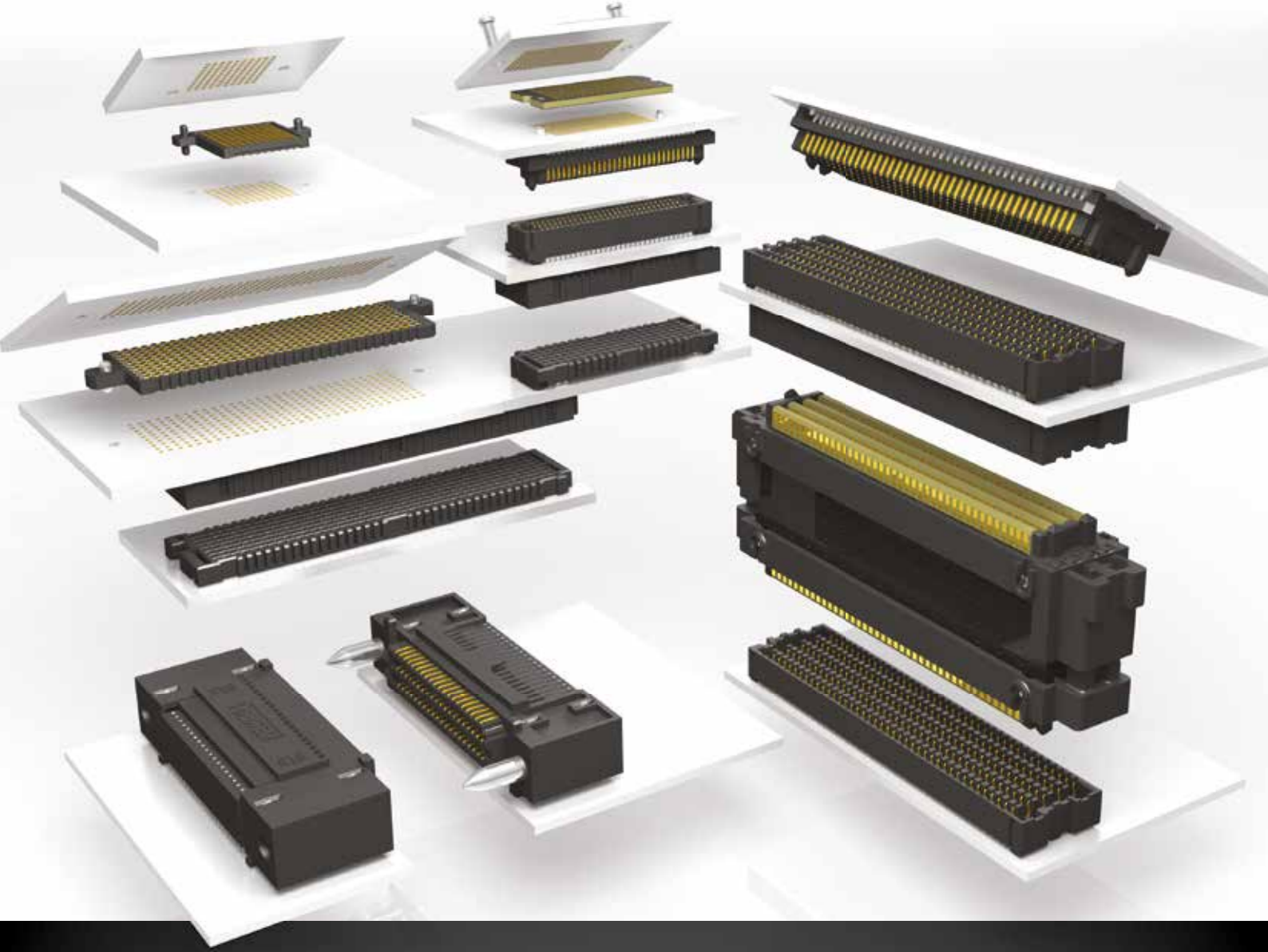

- (1,27 mm x 1,27 mm) .050" x .050" grid array for maximum grounding and routing flexibility
- Up to 500 single-ended I/Os or 125 differential pairs (using Samtec recommended pin assignments)
- Rugged Edge Rate® contact system less prone to damage when "zippered" to unmate
- 0,80 mm pitch system for up to 50% board space saving
- Right angle and low profile systems
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