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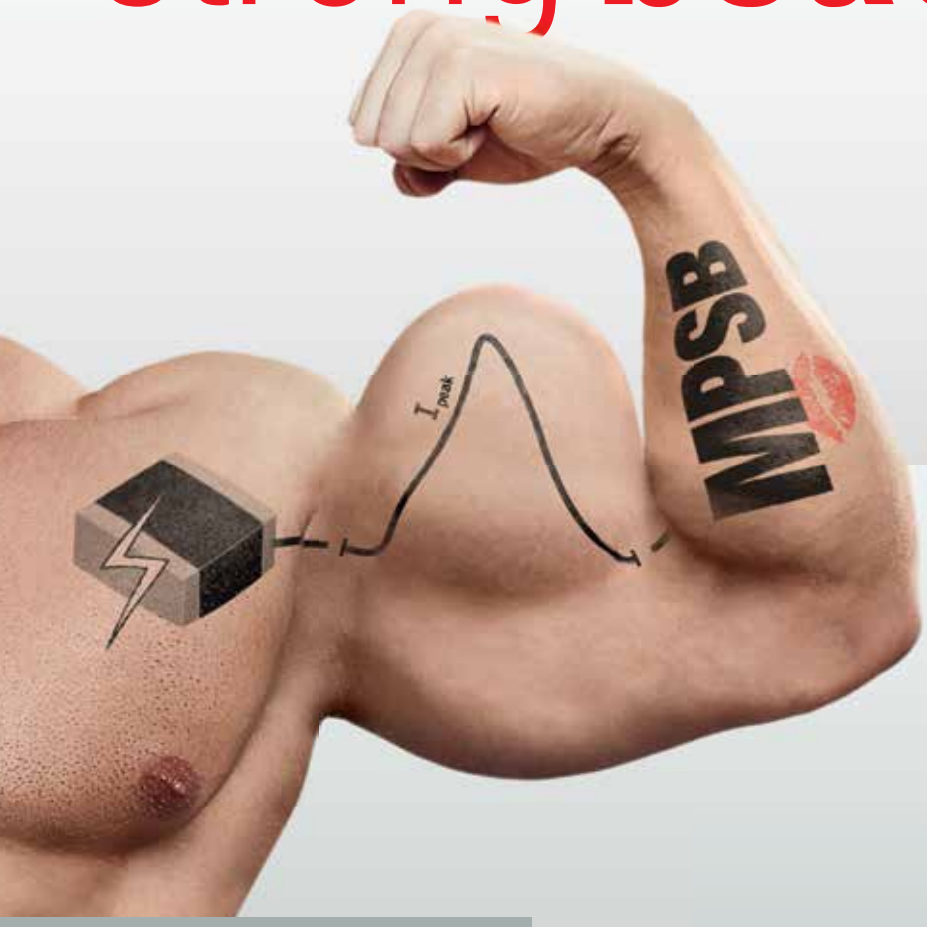

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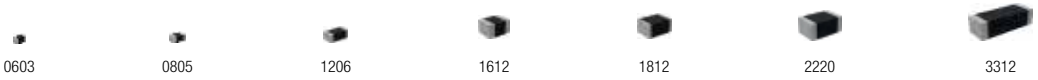

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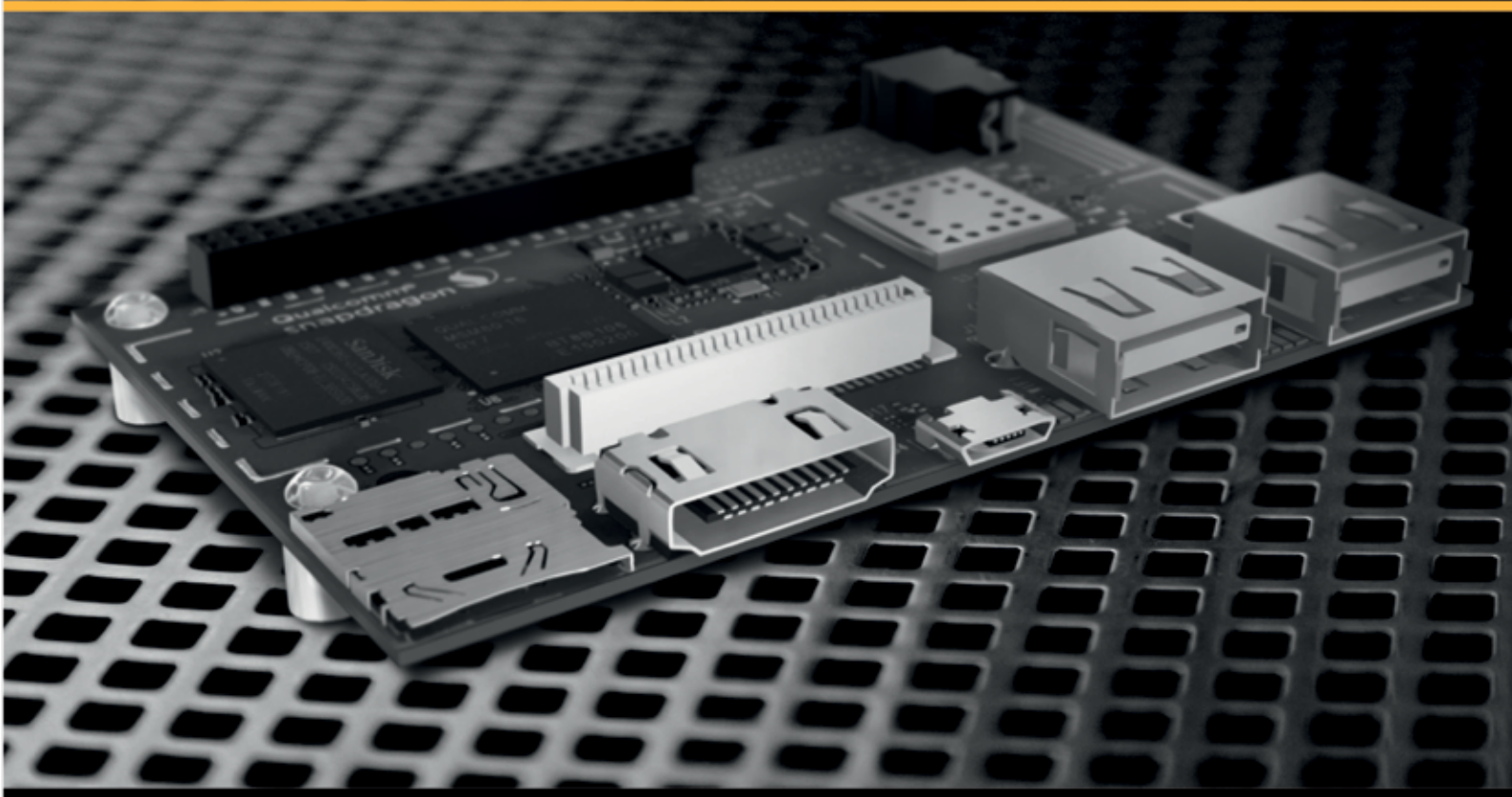
DragonBoard 410c supports Android 5.1 and Linux based on Ubuntu at launch and also support windows10 IoT and offers advanced processing power, WLAN, Bluetooth, and GPS, all packed into a board the size of a credit card. It is designed to support feature-rich functionality, including multimedia, with the Qualcomm® Adreno™ 306 GPU, integrated ISP with up to 13 MP camera support, and 1080p HD video playback and capture with H.264 (AVC).



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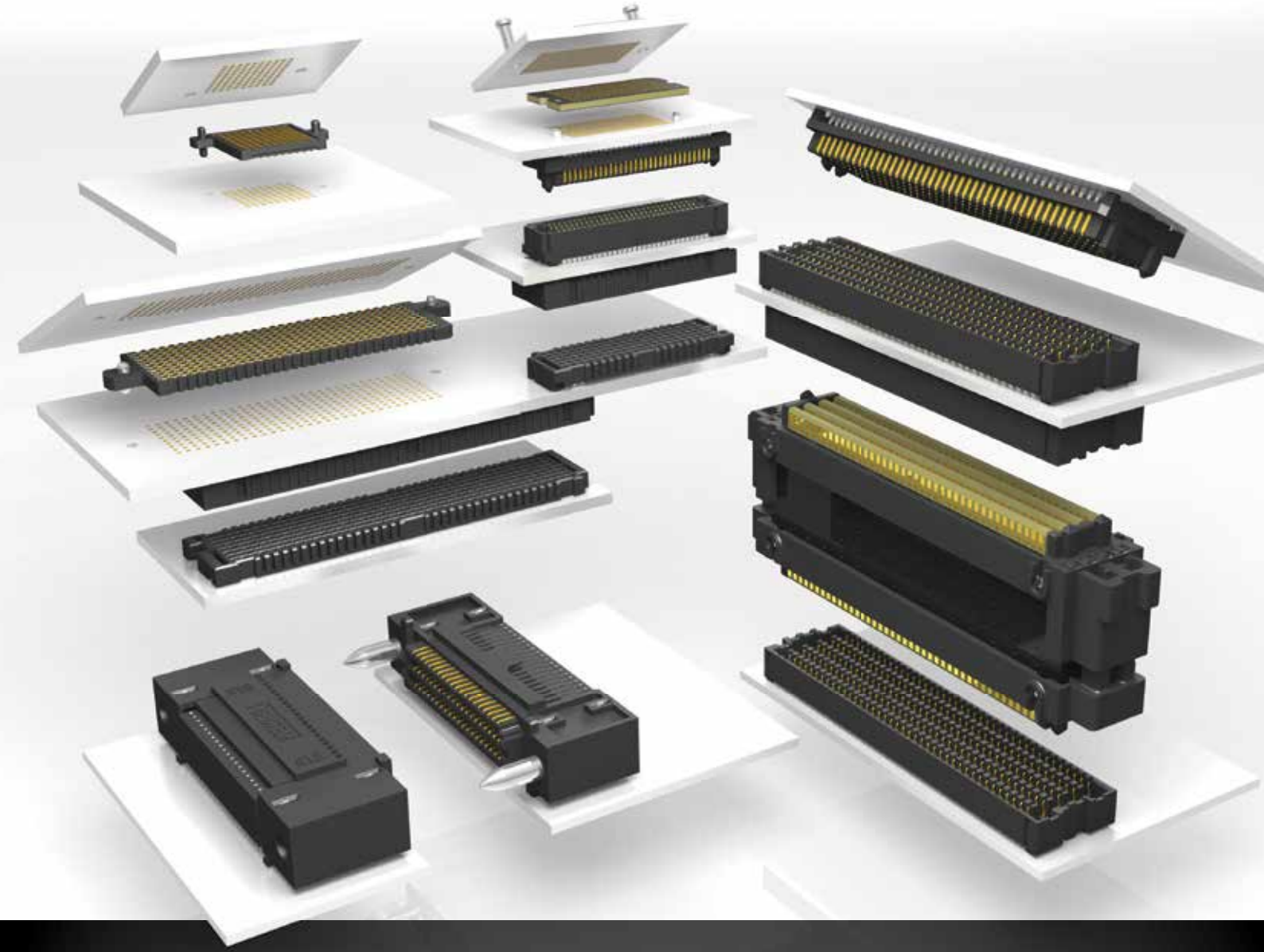

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About New-Tech Magazines Group

'New-Tech Magazines' A world leader in publishing high-tech and electronics, producing top quality publications read by tens of thousands professionals from all over the world especially from Europe, innovative electronics, IoT, microwave, homeland security, aerospace, automotive and technological industries.

Our specialized target audiences prefer New-Tech Europe because they know that our publications are a reliable source of the latest information in their respective fields. Our multidimensional editorials, news items, interviews and feature articles provide them with a full, well-rounded picture of the markets in which they operate - an essential asset for every technological leader striving to stay ahead, make the right decisions, and generate the next global innovation.

Moreover, as an attractive platform for advertisers from around the world, New-Tech Europe has become a hub for bustling international commercial activity. Here, through ads and other promotional materials, Israeli readers obtain crucial information about developers and manufacturers worldwide, finding the tools, instruments, systems and components they need to facilitate their innovative endeavors.

Targeting the needs of both the global and european industries and global advertisers, New-Tech Magazines Group constantly expands and upgrades its services. Over the years, the company has been able to formulate a remarkably effective, multi-medium mix of offerings, combining magazine publications with useful online activities, newsletters and special events and exhibitions.

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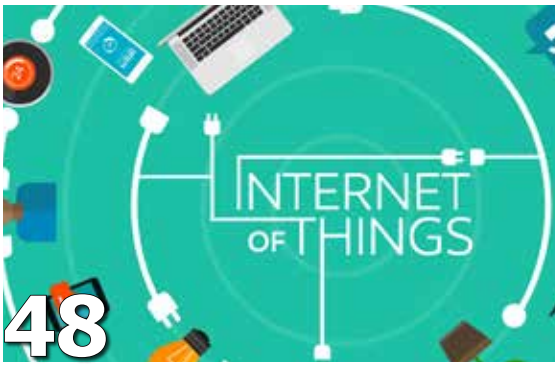

TactoTek awarded EUR 2.5 Million EU Horizon 2020 grant to mass produce injection molded electronics

TactoTek Solution and Capabilities Recognized As Key Enabling Technology That Enables and Drives Innovation and EU Competitiveness

TactoTek, a leading manufacturer of 3D injection molded structural electronics (IMSE) solutions today announced that it has been named a recipient of a €2.5 million EU Horizon 2020 award to mass produce injection molded electronics (IME) solutions.

Horizon 2020 is the financial instrument of Innovation Union, a Europe 2020 flagship initiative aimed at securing Europe's global competitiveness and whose charter includes supporting new, breakthrough enabling and industrial technologies that strengthen Europe's industrial capabilities.

"TactoTek is honored to be selected by the H2020 investment committee," said Jussi Harvela, CEO of TactoTek,

TactoTek's solutions integrate printed circuitry, printed touch controls and discrete electronic components, such as LEDs and ICs, into light, 3D injection molded plastics as thin as 2mm. By incorporating circuitry and electronics directly into plastic structures, TactoTek enables brands to design innovative form factors and consolidate electronics into a single 3D structure.

TactoTek maintains a staff of engineers to help customers adapt their traditional electronics designs into IMSE solutions. The company prototypes and manufactures products in its Kempele, Finland, factory that includes a complete, vertically-integrated production capability; mass production can be performed by TactoTek or TactoTek-licensed production partners.

Hallmark Envisions Real-Time Space Command and Control

First effort under new program aims to develop technologies to help commanders rapidly plan, assess, and execute the full spectrum of U.S. military operations in space

Military commanders responsible for situational awareness and command and control of assets in space know all too well the challenge that comes from the vast size of the space domain. The volume of Earth's operational space domain is hundreds of thousands times larger than the Earth's oceans. It contains thousands of objects hurtling at tens of thousands of miles per hour. The scales and speeds in this extreme environment are difficult enough to grasp conceptually, let alone operationally, as is required for commanders overseeing the nation's increasingly critical space assets.

Current space domain awareness tools and technologies were developed when there were many fewer objects in space. Only a few nations could even place satellites in orbit, and those orbits were easily predictable without advanced software tools. That situation has changed dramatically in the past decade with a developing space industry flooding once lonely orbits with volleys of satellite constellations. Despite this much more complex and chaotic environment, commanders with responsibility for space domain awareness often rely on outdated tools and processes - and thus incomplete information - as they plan, assess, and execute U.S. military operations in space.

To help address these technical and strategic challenges, DARPA is launching the first of two planned efforts under the Agency's new Hallmark program, which has the overarching goal to provide breakthrough capabilities in U.S. space command and control. This first effort, the Hallmark Software Testbed (Hallmark-ST), has as its primary goal the creation of an advanced enterprise software architecture for a testbed for tools that will integrate a full spectrum of real-time space-domain systems and capabilities. The testbed would be used to expedite the creation and assessment of a comprehensive set of new and improved tools and technologies that could be spun off into near-term operational use for the Defense Department's Joint Space Operations Center (JSpOC) and Joint Interagency Combined Space Operations Center

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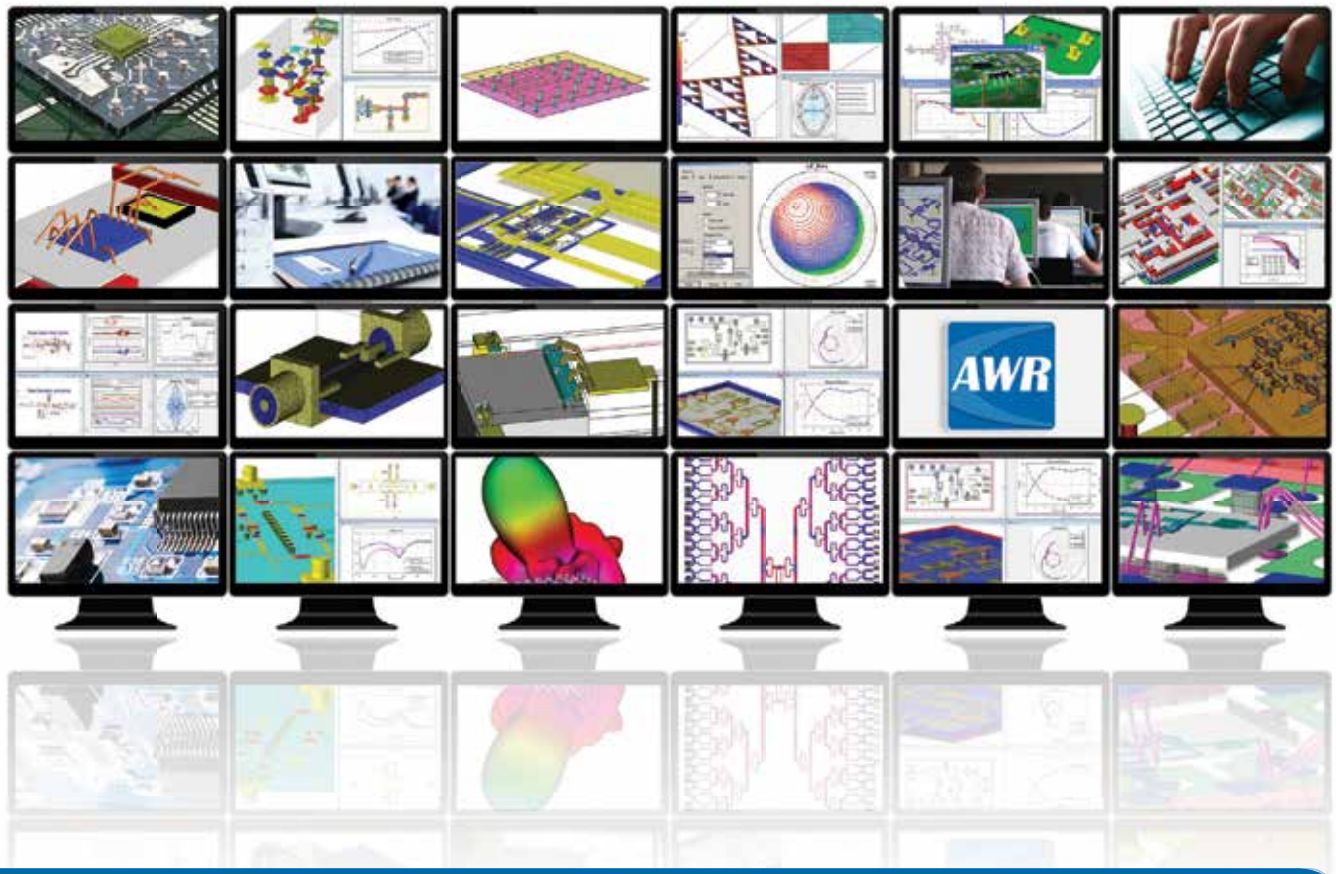

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A Broad Agency Announcement (BAA) providing technical details about Hallmark-ST is available at http://go.usa.gov/xqqHm, and will be followed in the near future by a second BAA encompassing additional Hallmark goals.

"We envision a system that would fuse information from diverse sources and vastly reduce the overall time required to make and execute decisions and observe results," said Brad Tousley, director of DARPA's Tactical Technology Office (TTO), which oversees Hallmark. "For example, an intuitive user interface incorporating 3-D visualization technology would present complex information in novel ways and provide commanders with unprecedented awareness and comprehension. An advanced testbed featuring playback and simulation capabilities would significantly facilitate research and development activities, experiments, and exercises to evaluate new technologies for their impact on space command and control capabilities."

Specifically, Hallmark-ST seeks to design, develop, and maintain a state-of-the-art enterprise software architecture that would be flexible, scalable, secure, and capable of supporting tools and data from diverse sources. The architecture would need to support the ability to model current and future space situational awareness and command and control tools, capabilities, subsystems, and systems, as well as external capabilities and interfaces to support air, cyber, land, and maritime environments.

The enterprise architecture would be the backbone of a long-term testbed, the Hallmark Space Evaluation and Analysis Capability (SEAC), anticipated to be located in Northern Virginia. SEAC would provide for the effective development, integration, modeling and simulation, and realistic testing of software and decision-support processes relevant to space command and control. It would also eventually contribute to the rapid integration of technology into future space enterprise command and control systems. Furthermore, Hallmark personnel at SEAC would be integral to the actual integration of external space command and control tools, capabilities, and data, as well as execution of a number of anticipated tests and scenario-based exercises.

Local Motors Debuts "Olli", the First Self-driving Vehicle to Tap the Power of IBM Watson

Local Motors, the leading vehicle technology integrator and creator of the world's first 3D-printed cars, today introduced the first self-driving vehicle to integrate the advanced cognitive computing capabilities of IBM (NYSE: IBM) Watson.

The vehicle, dubbed 'Olli,' was unveiled during the Grand Opening of a new Local Motors facility in National Harbor, MD this morning, and transported Local Motors CEO and co-founder John B. Rogers, Jr. along with vehicle designer Edgar Sarmiento from the Local Motors co-creation community into the new facility. The electric vehicle, which can carry up to 12 people, is equipped with some of the world's most advanced vehicle technology, including IBM Watson Internet of Things (IoT) for Automotive, to improve the passenger experience and allow natural interaction with the vehicle.

Local Motors CEO and co-founder John B. Rogers, Jr. Introduces Olli, on Thurs., June 16, 2016 in Fort Washington, MD. (Rich Riggins/Feature Photo Service for IBM)

Starting today, Olli will be used on public roads locally in DC, and late in 2016 in Miami-Dade County and Las Vegas.

"Olli offers a smart, safe and sustainable transportation solution that is long overdue," Rogers said. "Olli with Watson acts as our entry into the world of self-driving vehicles, something we've been quietly working on with our co-creative community for the past year. We are now ready to accelerate the adoption of this technology and apply it to nearly every vehicle in our current portfolio and those in the very near future. I'm thrilled to see what our open community will do with the latest in advanced vehicle technology."

Local Motors Debuts Olli, First Self-Driving Vehicle to Integrate IBM Watson Local Motors CEO and co-founder John B.

Rogers, Jr. introduces Olli, on Thurs., June 16, 2016 in Fort Washington, MD . Olli is the first self-driving vehicle to integrate the advanced cognitive computing capabilities of IBM Watson. The 12 passenger electric vehicle analyzes and learns from high volumes of transportation data and enables seamless interactions between the vehicle and passengers. (Rich Riggins/ Feature Photo Service for IBM)

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Olli is the first vehicle to utilize the cloud-based cognitive computing capability of IBM Watson IoT to analyze and learn from high volumes of transportation data, produced by more than 30 sensors embedded throughout the vehicle. Using the Local Motors open vehicle development process, sensors will be added and adjusted continuously as passenger needs and local preferences are identified. Furthermore, the platform leverages four Watson developer APIs - Speech to Text, Natural Language Classifier, Entity Extraction and Text to Speech - to enable seamless interactions between the vehicle and passengers.

Passengers will be able to interact conversationally with Olli while traveling from point A to point B, discussing topics about how the vehicle works, where they are going, and why Olli is making specific driving decisions. Watson empowers Olli to understand and respond to passengers' questions as they enter the vehicle, including about destinations ("Olli, can you take me downtown?") or specific vehicle functions ("how does this feature work?" or even "are we there yet?"). Passengers can also ask for recommendations on local destinations such as popular restaurants or historical sites based on analysis of personal preferences. These interactions with Olli are designed to create more pleasant, comfortable, intuitive and interactive experiences for riders as they journey in autonomous vehicles.

As part of Olli's debut, Local Motors officially opened its new National Harbor facility in Maryland today to serve as a public place where co-creation can flourish and vehicle technologies can rapidly advance. The company's 3D-printed cars are on display, along with a large-scale 3D printer and an interactive co-creative experience that showcases what the future of the nation's capital might look like. STEM-centered programming is also being developed for the facility so that the public can learn more about 3D printing, sustainability, autonomous technology and get involved with Local Motors engineers and the company's co-creation community.

The very first Olli will remain in National Harbor this summer, and the public will be able to interact with it during select times over the next several months. The development of the cognitive rider experience in Olli is a collaboration between Local Motors and IBM Watson IoT's AutoLAB, an industry-specific incubation engine for co-creation of cognitive mobility applications. Production of additional Ollies is taking place at Local Motors headquarters near Phoenix.

Leti Extends CMOS Platforms' Lifespan and Explores New Computing Paradigms

Leti, an institute of CEA Tech, said today its teams have demonstrated how Fully Depleted Silicon on Insulator (FDSOI) technology can be scaled downwards and how the experience in thin-film engineering built on FDSOI development can be harnessed for innovative architectures and computing paradigms.

At the recent 2016 Symposia on VLSI Technology and Circuits, Leti reported how performance boosters can be successfully implemented on a short time scale to increase performance of next-generation FDSOI devices using material engineering and design/technology co-optimization. With its current performance and flexibility, the FDSOI platform can be extended to the 10nm node. Looking further ahead, thin-film management expertise will be leveraged to design high-performance stacked nanowires.

Based on its expertise in CMOS technologies and thin-film integration, Leti also shared its latest results on CoolCubeTM high-density 3D integration. For the first time, 3D-via density above 10 million/mm² has been demonstrated and high CMOS FDSOI performance has been achieved within a low-temperature integration. CoolCubeTM, which powerfully leverages the benefits of the third dimension, provides designers with a wide range of design opportunities.

Through extreme device scaling, Leti and Inac, a fundamental research division of CEA, are exploring the emerging quantum computing era with an extended use of

FDSOI technology for chip design and fabrication.

"These results, which highlight the technology depth of the Grenoble ecosystem, stem from more than a decade of research on ways to use FDSOI-nanowire silicon technologies to design devices with an accurate control of single charge," said Maud Vinet, Leti's advanced CMOS manager. "We are currently leveraging this R&D activity, which relies primarily on extensive research in low-temperature physics of ultra-scaled MOS FET properties developed by Leti and Inac, to investigate the potential that silicon FDSOI technology has for quantum computing."

Leti and its long-time research partner Inac have been investigating a silicon-on-insulator technology for quantum computing applications that could rely on the scalability originally developed for CMOS VLSI circuits. Applying Inac's expertise in cryogenic electrical measurements and Leti's SOI nanowire FET technology, the teams also demonstrated the co-integration of quantum devices with conventional CMOS control electronics (ring oscillators) on 300 mm SOI substrates.

Cypress and MyScript® Announce Partnership for Automotive Industry

Cypress Semiconductor Corp. (NASDAQ: CY), a global leader in controllers for car infotainment systems, and MyScript, an industry pioneer in automotive HMI technologies, have joined forces to include MyScript's intuitive and precise handwriting recognition technology to automotive designers worldwide powered by Cypress's Traveo™ microcontroller (MCU) family. MyScript's automotive HMI input method technology enables a low-distraction user interface. Drivers can write characters or numerals, or simply gesture with their fingertips on a touchscreen or touchpad to quickly and discreetly accomplish important tasks, such as selecting a destination, making a telephone call or noting information. Cypress offers TrueTouch® capacitive touchscreen and touchpad solutions with industry-leading resistance to electrical noise, glove touch and water resistance, which combine with the Traveo MCU solutions to enable innovative and robust automotive HMI.

"We are excited to partner with Cypress to bring the benefits of handwriting input to the Traveo MCU family and significantly enhance the driver user experience," said Olivier Cros, Director of Global Automotive Sales at MyScript. "The joint integration development activity will bring MyScript's award winning automotive HMI solutions to the compact automotive segment, expanding the number of drivers that can now enjoy the benefits of a low-distraction input method within the vehicle."

Cypress and MyScript have been working together in the automotive market achieving several large successes and are now intensifying their activities together to bring a faster time-to-market solution to automotive developers for dashboards, navigation, head-up displays and HVAC systems in vehicles.

"Our partnership with MyScript marks another example of Cypress's commitment to bring innovative HMI automotive systems to the mass market," said Nils Bossemeyer, Systems Application Engineering Manager for Automotive Microcontrollers at Cypress. "This partnership adds to our ability to serve as a one-stop resource for our automotive customers, combining our Traveo MCU family and MyScript's handwriting input technology together with our broad line of memory products, PMICs, TrueTouch® touchscreen controllers and CapSense® touch-sensing HMI solutions."

Integration of the new Traveo family members with the award-winning MyScript handwriting input recognition technology will streamline design timelines and greatly enhance the driving experience. A unified effort will embed handwriting recognition together with the latest Traveo MCUs offerings, which represent another step forward in bringing the luxury car user experience to the mass market. By offering a high-performance and scalable platform, Cypress customers can affordably deliver a high-end and non-distractive input method in compact vehicles.

First test plant to produce fuel from solar power to be established in Finland

The production plant made up of container-sized units assembled on the LUT campus is to be completed in 2017. The purpose of this cooperation project is to convert solar power-produced electricity into gas or liquid fuels.

The research plant, which has been named SOLETAIR, will be made up of three components: VTT will design the equipment that will extract carbon dioxide from air and store it. LUT's task will be to build a device that will utilise electricity to produce hydrogen through the electrolysis of water. Another of the VTT's tasks will be to develop a synthesis device that will produce e.g. methane or liquid fuel from carbon dioxide or hydrogen.

The plant will be used to demonstrate how processes can be combined in a way that allows the utilisation of renewable electricity in the production of e.g. methane, fuels and chemicals. The demo plant could thus also function as a fuelling station for vehicles that run on hydrogen or natural gas.

"This research is the first of its kind in Finland in this type of combination of processes," states LUT Professor Jero Ahola, who is responsible for the research.

"The project will produce expertise for enterprises in various fields, and it will result in a multidisciplinary industrial integration that no one company can achieve on its own. Collaboration will strengthen the expertise of Finnish industry in this sector," states VTT's Principal Scientist Pekka Simell. He is responsible for coordinating the project as well as VTT's share of the research.

To help cut carbon dioxide emissions, in the future, all sectors of industry must be within the scope of carbon dioxide emission-free energy production. In practice, this means that the future's most important energy market will be the electricity market, where different sectors of industry will operate with electricity produced from carbon dioxide emission-free energy sources. Combining the electricity system and other energy systems will be successful with the researched methods.

The research will aim to build expertise that will facilitate the implementation of industrial-scale solutions. The project's second key aim will be to create new business opportunities for Finnish industry.

LUT and VTT have invested one million euros in the plant. Tekes and a group of Finnish companies including ABB, Gasum, GreenEnergy Finland, Hydrocell, Ineratec GmbH, Proventia Emission Control Oy and Trafi Finnish Transport Safety Agency, will fund the research.

Ficosa awarded multiple rear-view mirrors contract worth $510 M in North America

Ficosa, top-tier global provider devoted to the research, development, manufacturing and marketing of high-technology vision, safety, connectivity and efficiency systems for the automotive and mobility sectors, has been awarded four contracts from two American OEMs to produce 8,900,000 units of rear-view mirrors over a period of five years in North America. The total amount of these orders is 510 million dollars (approximately 449 million euros) and means a record number of contracts closed with OEMs in a single year in the North American region.

In the words of Joan Cañellas, Ficosa North America CEO: "These new projects for rear-view mirrors ensure high production volume and consolidate our business with strategic customers in the North America region, reaffirming our commitment and steady growth in this area".

The new facility in Cookeville wins three of the four contracts

Three orders will be produced in the new facility in Cookeville (Tennessee), which will be the group's most advanced worldwide. These will be the first new projects to go to the new factory, which will kick off its activity in October 2016.

In total, these new contracts will account for 1,700,000

rear-view mirrors annually for a period of five years. The value of this Cookeville production will represent an economic value of 460 million dollars (405 million euros), and will begin in the first quarter of 2018.

The Cookeville plant, which is expected to be fully operational later this year, will be a leader in painting and injection processes thanks to the latest technology production equipment.

Furthermore, Ficosa North America is currently recruiting 240 new workers for positions including project managers, technicians, engineers, operators and human resources specialists

Cañellas highlights: "These projects will give the Cookeville plant a strong boost and not only reinforce the company's business in North America but allow us to give our workers a better, safer future".

For its part, the Mexican facility of Salinas Victoria (Nuevo León) will produce a fourth order consisting of 80,000 rear-view mirrors per year for a period of 5 years. This contract comes from an American OEM in the premium segment and is valued at a total of 50 million dollars (43.9 million euros). Production will start in the last quarter of 2018.

Consolidating its presence in North America

North America has become, after Europe, the most important market for this multinational corporation, which began operations in this region in 1994 and where it produces mirrors, gearboxes and brake systems. In the United States, Ficosa currently has a commercial office and development center, which employs 35 engineers, in Detroit (Michigan); a production centre in Shelbyville (Kentucky) and a new plant in Cookeville (Tennessee), which when at full capacity will replace the Crossville factory (Tennessee). The two Ficosa plants in Mexico, located in Salinas Victoria (Nuevo León) and Escobedo (Nuevo León), where the company also has an R&D plant, reinforce Ficosa's activity in the North American region.

STMicroelectronics Joins Forces with Automotive Software

STMicroelectronics Joins Forces with Automotive Software Experts ETAS and ESCRYPT to Streamline Development of Secure Connected-Car Applications

Combined competencies to offer a unique package for developing high-performance, safe, and secure automotive-embedded systems

End-to-end solution protects against malicious attacks on the car's Electronic Control Units (ECU) and secures communication among ECUs and the cloud

Easy-to-use AUTOSAR-compliant platform software addresses key time-to-market and standards-compliance challenges facing OEM and Tier-1 application developers

Geneva, Stuttgart, and Bochum/13 Jun 2016STMicroelectronics(NYSE:STM),aglobalsemiconductor leader serving customers across the spectrum of electronics applications, announced its collaboration with ETAS, a provider of innovative solutions for developing automotive embedded systems, and ESCRYPT, an ETAS subsidiary focused on security for embedded software, to deliver a complete platform comprising microcontrollers, software tools, and security solutions that accelerates development of new automotive control units for the connected-car age.

Today's auto designers rely more and more on electronic control units (ECUs) to manage intricately featured applications, including brake-by-wire, automatic transmission, multi-mode lighting, parking assist, collision avoidance and many others. These ECUs are enabling "digital" control of each function of the car through sending commands over the communication network that interconnects the vehicle sub-systems. Moreover, more cars are becoming connected to the cloud enabling new functionalities like Over-The-Air (OTA) software updates, remote diagnostics, and the forthcoming V2X communication[1].

To safely support such trends, there is an acceleration in the deployment of robust hardware and software security platforms that are managed over the entire vehicle lifetime. ST is working with ETAS and ESCRYPT to deliver a cost-effective platform for sub-system developers to create ECUs that ensure a high level of protection for vehicle-owners' privacy, OEMs' intellectual property, ECU functional integrity, and secure communication among the car's ECUs and the cloud.

"This well-architected and easy-to-use development platform will deliver unprecedented convenience to customers in the form of a ready-made solution that combines the security know-how of ESCRYPT, ETAS, and ST," said Luca

Rodeschini, Director Strategic Business Development and Microcontroller Business Unit, Automotive and Discrete Product Group, STMicroelectronics.

The solution ST is developing with ETAS and ESCRYPT leverages the SPC58 series of power-efficient and real-time-capable automotive microcontrollers, which feature a built-in Hardware Security Module (HSM) as well as multiple state-of-the-art CAN FD interfaces, plus LIN, FlexRay, and Ethernet with time-stamping to implement both control units with a functional integrity check and an in-vehicle network with encrypted communication. This approach expands ST's offering for connected-car defense, which also includes Secure Elements, or embedded SIMs (Subscriber Identity Modules), for protection against Internet-based attacks on ECUs and gateways that can steal personal data or compromise important vehicle systems.

"SPC58 automotive microcontrollers deliver the underlying ruggedness and hardware security the industry needs at a competitive price. They have already been selected by a major Tier-1 supplier for a secure OTA (Over-The-Air) application that enables remote software fixes and upgrades without requiring customers to bring their vehicles to a repair garage," added Rodeschini.

ESCRYPT is contributing its expertise in secure ECU communication, including distribution of OTA software updates, and provides firmware and middleware for ECU developers to utilize the SPC58 HSM. Together, the HSM and ESCRYPT's security technologies handle all the necessary authentication of trusted sources and prevention of access by unauthorized agents. "We provide our productCycurHSM, the essential solution that exercises the HSM and our Key Management Solution to secure every aspect of the ECU's activity, including secure boot-up, programming, and updates, as well as secure in-vehicle communication," explained Dr. Thomas Wollinger, Managing Director of ESCRYPT.

The solution leverages ETAS' proven RTA software products that support ECU code development. RTA-BSW (Basic Software) consists of a full AUTOSAR solution including AUTOSAR R4-compliant basic software capable of supporting safety-critical ECUs for both passenger cars (ISO 26262) and off-highway

(ISO 25119) domains. RTA-BSW is complemented by ISOLAR-A and ISOLAR-EVE tools for authoring and testing a full ECU software stack in a virtual environment.

AUTOSAR, the AUTomotive Open Systems Architecture, is the accepted automotive industry framework for scalable, interoperable, standards-compliant embedded systems, which enables developers to bring new products to market quickly and cost-effectively while allowing scope to create differentiating features.

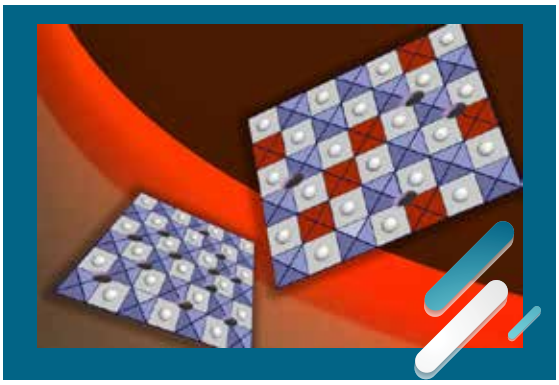
"We are building on a proven record of successful collaborations with ST," said Dr. Nigel Tracey, leader of the ETAS Application Field RTA Solutions. "With our comprehensive ECU development environment, and the added dimension of advanced security from our subsidiary ESCRYPT, this new platform will enable OEMs to maximize the value of the connected-car concept and quickly build confidence among partner organizations and end users."

Researchers find a way to extend life and improve performance of fuel cell electrodes

Researchers at MIT have developed a practical and physically-based way of treating the surface of materials called perovskite oxides, to make them more durable and improve their performance. These materials are promising candidates to serve as electrodes in energy-conversion devices such as fuel cells and electrolyzers. This surface treatment could solve one of the major challenges that has hindered widespread deployment of fuel cell technology that, when operated reversibly, can present a promising alternative to batteries for renewable-energy storage.

The new findings are being reported today in the journal Nature Materials, in a paper by MIT Associate Professor Bilge Yildiz of the departments of Nuclear Science and Engineering and Materials Science and Engineering, former MIT postdoc Nikolai Tsvetkov, graduate students Qiyang Lu and Lixin Sun, and Ethan Crumlin of the Lawrence Berkeley National Laboratory.

Perovskites have become a bustling area of research in recent years, with potential applications in areas ranging from fuel cell electrodes, to nonvolatile memory chips for computers, to solar thermochemical fuel production through the splitting of water and carbon dioxide. They are a broad class of oxide materials, and many teams are exploring variations of perovskite composition in search of the most promising candidates for different uses. But the relative instability of the material's surface over time has been one of the major limitations to use of perovskites.



The surfaces of these materials, when exposed to water or gases such as oxygen or carbon dioxide at elevated temperatures, as they often are in actual applications, "suffer from degradation because of chemical segregation and phase separation," Yildiz explains. She says

In earlier work, Yildiz and her team uncovered the reasons behind such detrimental surface segregation of strontium. This idea is contrary to the conventional understanding that oxygen vacancies assist reactions with oxygen molecules at the perovskite oxide surface and improve the rate of oxygen reduction reaction in fuel cells.

So, simply adding a small fraction of more oxidizable elements at the perovskite surface "annihilates some of the oxygen vacancies, makes the surface more oxidized, and prevents the formation of insulating phases that block oxygen exchange reactions at the surface of the material," Yildiz says. In this way, the surface retains the intrinsically good electronic, ionic, and catalytic properties of the perovskite oxide and enables fast oxygen exchange reactions.

The team's analysis shows that there is a sweet spot in the addition of more oxidizable elements to the surface, both in terms of the composition and the concentration. In these initial experiments, they tried several different elements to provide the protective effect. The improvement increases up to a certain concentration, and then adding more of the surface additives starts to make things worse again. So for any given material, there will be an optimum amount that should be added, they found. Using hafnium, the new treatment has been shown to reduce the rate of degradation, and increase by 30 times the rate of oxygen exchange reactions at the surface.

NXP Semiconductors to Divest its Standard Products Business

NXP Semiconductors N.V. (NASDAQ:NXPI) today announced an agreement to divest its Standard Products business to a consortium of financial investors consisting of Beijing Jianguang Asset Management Co., Ltd ("JAC Capital") and Wise Road Capital LTD ("Wise Road Capital"). Under the terms of the agreement the consortium will pay approximately $2.75 billion for the business. The transaction is expected to close in the first quarter of 2017, pending all required regulatory approvals and employee representative consultations.

The NXP Standard Products business is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors focused on the Automotive, Industrial, Computing, Consumer, and Wearable application markets. At the close of the transaction, the NXP Standard Products business will be branded Nexperia, which will be headquartered in Nijmegen, the Netherlands. For fiscal 2015, the NXP Standard Products business had annual revenue of $1.2 billion.

"We are committed to provide Nexperia the capital it requires to accelerate its global growth strategy, which we believe will help to accelerate product introductions in key target markets, while assuring no disruption to Nexperia's global customer and supplier base. Although servicing a variety of markets, Nexperia will be especially increasing focus on automotive applications and providing their required high-level of quality solutions. In addition, we will help Nexperia expand its strong position in the fast-growing global emerging markets, through our strong network of industrial leaders," said Michael Zhang, Managing Partner of Wise Road Capital.

Under the agreement, the entire scope of the NXP Standard Products business, including its management team, led by Frans Scheper, and approximately 11 thousand NXP employees will be transferred to Nexperia. Nexperia will be an independent company incorporated in the Netherlands, and will be fully owned byJAC Capital and Wise Road Capital upon the close of the transaction. Additionally, NXP's Standard Product front end wafer fabs in Manchester, UK, and Hamburg, Germany, and the back-end facilities in Guangdong, China, Seremban, Malaysia, and Cabuyao, Philippines, will be transferred to Nexperia, as well as the in-house equipment manufacturer ITEC and all relevant patents and intellectual property associated with the Standard Products business.

The transaction, including the entry into and the terms of the definitive agreements and the approval of JAC Capital and Wise Road Capital as the acquirers are subject to review and approval by the US Federal Trade Commission, the European Commission, MOFCOM and other agencies. Credit Suisse acted as exclusive financial adviser to NXP.

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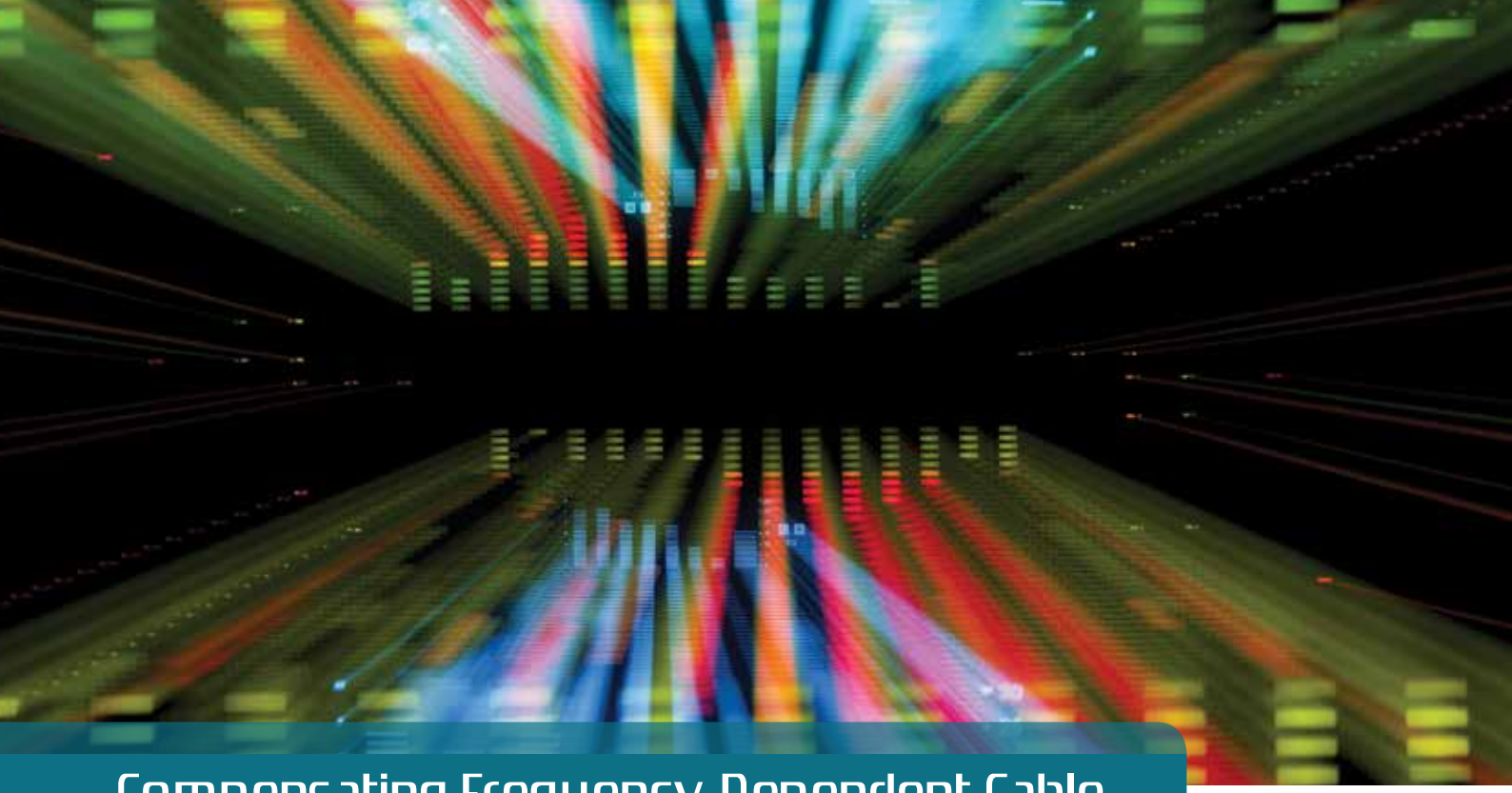

Compensating Frequency-Dependent Cable Loss in CATV Systems with Mini-Circuits Voltage-Variable Equalizers

› Ben Kahtan, Mini-Circuits

In broadband communications systems such as CATV equipment, system performance may critically rely on gain or attenuation flatness. In particular, CATV systems are often plagued by issues resulting from the frequency-dependent attenuation of very long cables (increasing with frequency) as well as the negative gain slope of certain amplifiers. This negative gain slope exhibited by CATV system components can cause a variety of headaches for system designers.

For example, suppose the system's operating bandwidth is split into a number of channels. Channels at lower frequencies are subject to much less attenuation than those at higher frequencies, so the "louder" low-frequency channels may saturate an amplifier exhibiting sufficient gain to amplify the "quieter" high-frequency channels. Obviously an amplifier driven to saturation in a spectrally rich multi-channel system would result in a whole mess of impossible-to-filter-out intermodulation products, so this situation is highly undesirable.

Out-of-band spurious spectral content (e.g. intermodulation products, harmonics) from the louder lower-frequency signals may also degrade the quality of the quieter, higher-frequency signals (be it in terms of MER, SNR, CNR, or any other Figure-Of-Merit flavors) – and so on.

Because both the amplifiers and the cables exhibit a negative gain/attenuation slope, in many cases a designer may wish to flatten this slope at the expense of overall gain. This can be done with a device that has a positive attenuation slope (over the desired operating frequency range), called an equalizer. Equalizers may be realized, for example, as resistive pi or tee networks with the series resistive elements "bypassed" by parallel capacitors and the shunt resistive elements "bypassed" by parallel inductors, effectively forming a lossy low-order high-pass structure. Figure 1 illustrates this concept.

Passive equalizers are relatively simple to design, and inexpensive to implement, but they lack versatility due to passive component values being fixed.

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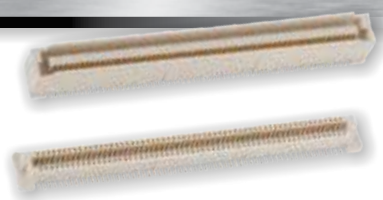

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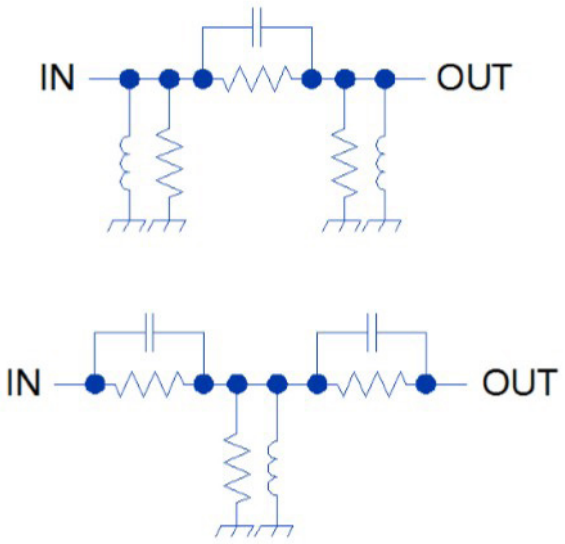


Figure 2 Implementation of AT Safeguards

that component performance varies with temperature, manufacturing tolerances, humidity, the installation technician's choice of breakfast on the preceding Tuesday, and so on. So, an equalizer that exhibits an optimal attenuation slope for 300 feet of Manufacturer A's coaxial cable, roasting at high noon during a Texan summer, might not work so well with 50 icicle-draped feet of Manufacturer B's cable in Maine. A designer may choose to design into her or his system a switchable bank of equalizers, which may be inserted into the signal path as necessary, but a discretized solution like this can rapidly turn cumbersome. Because the "amount" of positive slope needed to effectively flatten the gain of a particular system will vary depending on cable length, amplifier performance, gain/attenuation variations thereof over temperature, and myriad other system parameters, passive equalizers are applicable to relatively narrow regimes of operating conditions. A tunable solution, on the other hand, would be highly desirable. Mini-Circuits' VAEQ-1220-75+ offers exactly that—an equalizer whose attenuation slope is adjustable via an analog control signal. This component offers significantly increased versatility under the widely-varied operating conditions to which CATV systems are subjected. An "intelligent" control system can tune the voltage-variable equalizer's (VVE) frequency response on the fly, continually adapting to changes in operating parameters, and maintaining peak system performance.

Figures 2 and 3 illustrate the performance of a simplified hypothetical CATV system (consisting of two Mini-Circuits PGA-106-75+ amplifiers and 100 feet of RG-6/U coaxial cable). The red plot shows the gain of this system without the equalizer, and the blue plot shows the gain of this system with Mini-Circuits' VAEQ-1220-75+ voltage-variable equalizer inserted. In this simulation, a tuning voltage of 3.05 volts is applied to the VVE through its control input.

In this hypothetical system, the VAEQ-1220-75+ reduces a slope of about -20 dB to a nearly flat region. While this model has a particularly flat response within the DOCSIS 3.1 downstream band—up to 1220 GHz (and change)—it is also operable down to 5 MHz.

The VAEQ-1220-75+ is designed for use in 75Ω systems and is operable over the entire DOCSIS

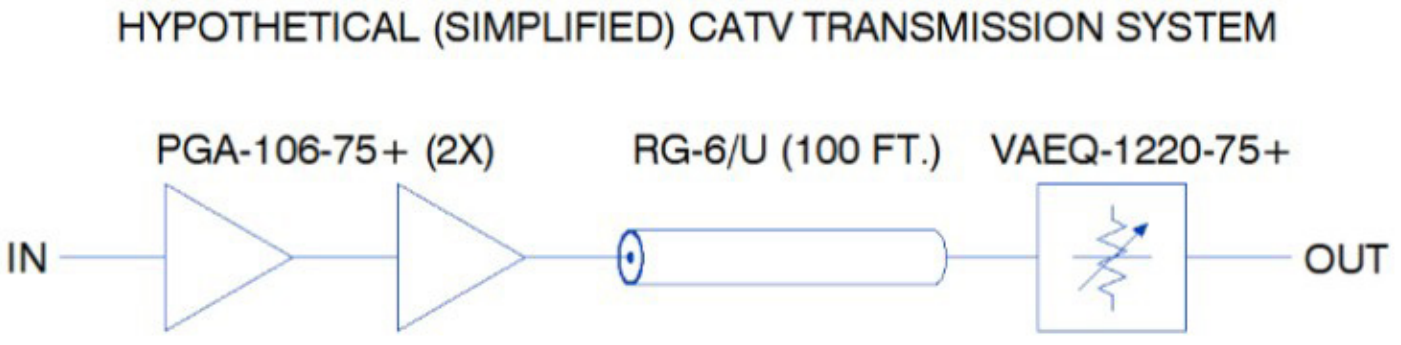


Figure 2: Hypothetical CATV transmission system including equalizer

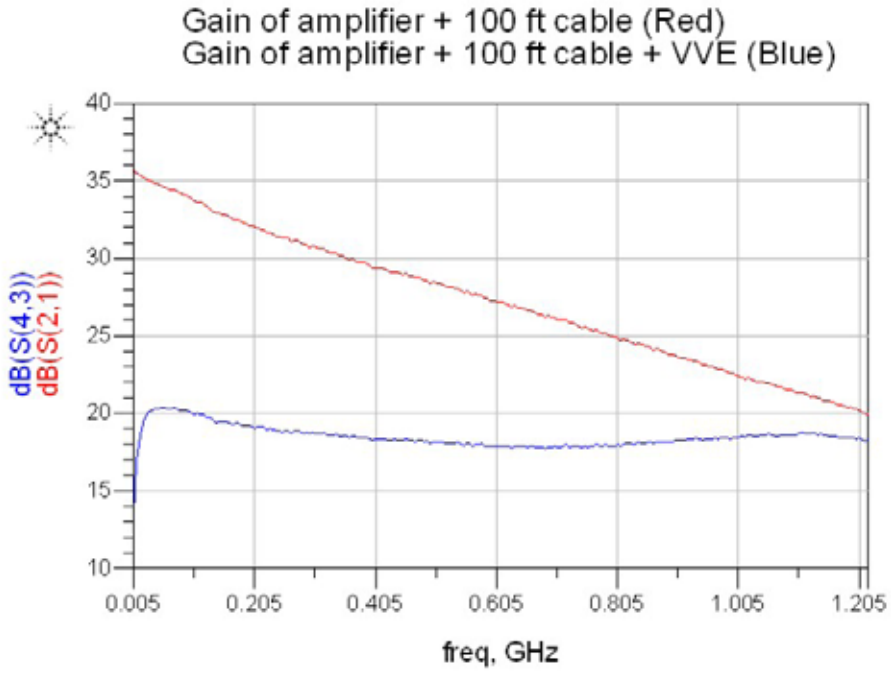


Figure 3: Simulation of simplified hypothetical CATV system consisting of two Mini-Circuits PGA-106-75+ amplifiers and 100 feet of RG-6/U coaxial cable with and without the VVE inserted.

3.1 bandwidth—both upstream and downstream frequencies—making it an ideal solution for the needs of the CATV world. S-parameter models at several control voltage states are available for this part, and Mini-Circuits can make additional data available on request to help you design the VAEQ-1220-75+ into your CATV systems.

In addition, if the VAEQ-1220-75+ isn't entirely suitable for your system, Mini-Circuits can assist in developing a special voltage-variable equalizer model to meet your exact needs, whatever they may be. Contact our applications engineering department (apps@minicircuits.com) for additional information on custom model development.

Foot Notes

[1]Wait for it…

[2]Consider the following anecdote from the early days of semiconductor engineering—before the days of stringent clean-room standards—occasionally cited by musty professors of integrated circuit design: A foundry, experiencing abnormally poor yields from wafers processed during the early afternoon, undergoes an intensive QA investigation to determine the problem's root cause. After months of careful auditing, the culprit is revealed to be contamination in the form of sodium chloride—crumbs of salt from potato chips eaten at lunch in the cafeteria. These stuck to careless engineers' hands, faces, and clothing, later falling into containers of chemicals used during the manufacturing process. Such an issue would surely never occur in modern industry, of course.

What Is RocketSim? Why Did Cadence Acquire Rocketick?

› Paul McLellan, Cadence

I talked to Uri Tal last week, who has just joined Cadence as a result of the Rocketick acquisition. Prior to the acquisition, he was Rocketick's CEO. He gave me a little history. Rocketick started development eight years ago. They have a product called RocketSim that accelerates logic simulation. They started by using GPUs to do this, but then switched to multi-core CPUs. They can run on all the cores in a socket, in practice up to 32 today, although like a surfer they will ride that wave as the number of cores per socket increases. I call this Core's Law: the number of cores on a processor doubles every two years.

6X for Verilog and SystemVerilog at RTL level

10X for gate-level functional simulation

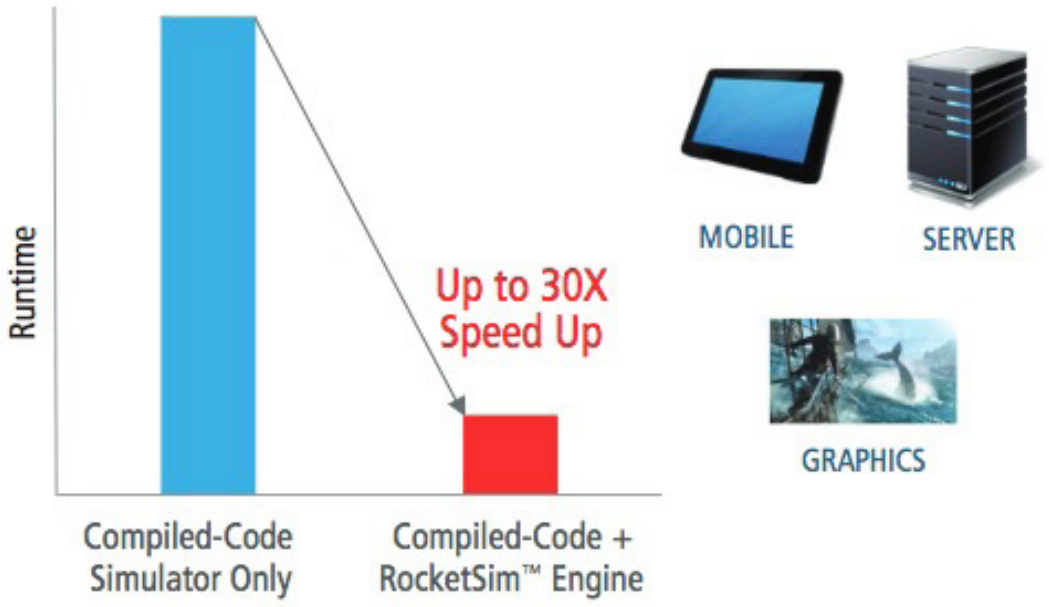
30X for gate-level DFT simulation

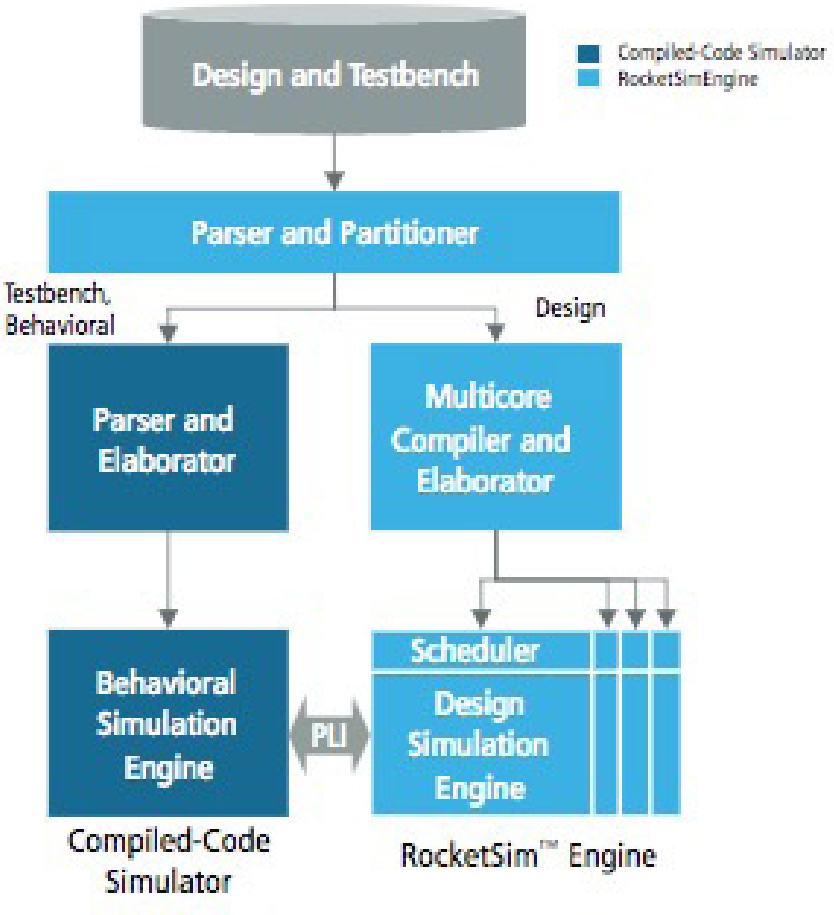
Another part of the value proposition is that you don't need to change any code, neither the RTL (or netlist) nor the testbench. As a result, RocketSim is in production use at many leading system and semiconductor companies. Intel Capital and NVIDIA were investors and NVIDIA has endorsed them (Intel doesn't endorse EDA suppliers).

The sweet spot seems to be large SoCs that are highly active, such as stress tests. The speedups are less with circuits that are not very active, which you would expect. No simulator needs to spend any time simulating inactive parts of a circuit, and it is obviously not possible to take less time than none. The focus of RocketSim is running complex simulations as fast as possible, so latency rather than throughput.

RocketSim block diagramUnder the hood, a simulation with Incisive and RocketSim runs the testbench on Incisive and the design simulation uses fine-grained parallelism to run on multiple threads. During compilation, the RocketSim engine's compiler runs on the host machine, separating the design from the testbench. During runtime, a large portion of the logic is offloaded to the RocketSim parallel simulation engine, running on standard multi-core servers, while the testbench runs on the host simulator. The PLI is used during simulation execution to maintain the state synchronization between the compiled-code simulator running the testbench and the RocketSim engine running the design.

Simulation is challenging to parallelize compared to something like a DRC since there is at least a global clock and potentially other high-activity signals that don't have well-behaved locality. When I was at Virtutech, we





could run large distributed simulations across many servers, but that was because we "cheated". We were not truly running a single system, but a lot of separate systems connected by networks. When you have a network like Ethernet, and processors running at GHz rates, there is no concept of the exact clock cycle when a packet "should" arrive, so it lessens the need for perfect synchronization. An SoC is not really like that. The need for synchronization leads to two problems. It can consume a lot of the bandwidth of the cores just to maintain time. And if it is done wrong, there is a risk that causality will be violated.

Some key features of RocketSim are:

Reduces host memory footprint by over 5X

Fast compilation of large designs

Full debug visibility

Billion+ gate capacity

Four-state logic

Compliant with Verilog IEEE 1364-2001, 1364-2005, VHDL, System Verilog, OVM, VMM, and UVM

PLI-compliant interface

Runs alongside the test bench

IGBT OVERCURRENT AND SHORT-CIRCUIT PROTECTION IN INDUSTRIAL MOTOR DRIVES

› Dara O'Sullivan, Analog Devices, Inc.

Abstract

A market-wide trend in industrial motor drives is an increasing demand for higher efficiency coupled with increased reliability and robustness. Power semiconductor device manufacturers are continually pushing the boundaries of conduction loss and switching time improvements. Some of the trade-offs in enhancing insulated gate bipolar transistor (IGBT) conduction loss are increased shortcircuit current levels, smaller die size, and reduced thermal capacity and short-circuit withstand time. This accentuates the importance of the gate driver circuit and its overcurrent detection and protection features. This article will discuss the issues involved in successful and reliable short-circuit protection in modern industrial motor drives, with experimental examples from an isolated gate driver in a 3-phase motor control application.

Short-circuits in Industrial Environments

Industrial motor drives can operate in a relatively harsh environment in which high temperature, ac line transients, mechanical overload, miswiring, and other contingencies can occur. Some of these events can result in large overcurrent levels flowing in the motor drive power circuits. Three typical short-circuit events are illustrated in Figure 1. These are described below:

1. Inverter shoot-through. This can be caused by the incorrect turn-on of both IGBTs in one of the inverter legs, which in turn can result from electromagnetic interference or a malfunction in the controller. It could also be caused by wearout/failure of one of the IGBTs in the leg while the healthy IGBT keeps switching.

2. Phase-to-phase short-circuit. This can be caused by insulation breakdown in the motor between windings due to degradation, overtemperature, or overvoltage events.

3. Phase-to-earth short-circuit. This can be caused by insulation breakdown between a motor winding and the motor casing; again usually due to degradation, overtemperature, or overvoltage events.

Generally speaking the motors are capable of absorbing very high current levels for relatively long periods (milliseconds to seconds depending on motor size and type); however the IGBTs - which make up the majority of industrial motor drive inverter stages - have short-circuit withstand times in the order of microseconds.

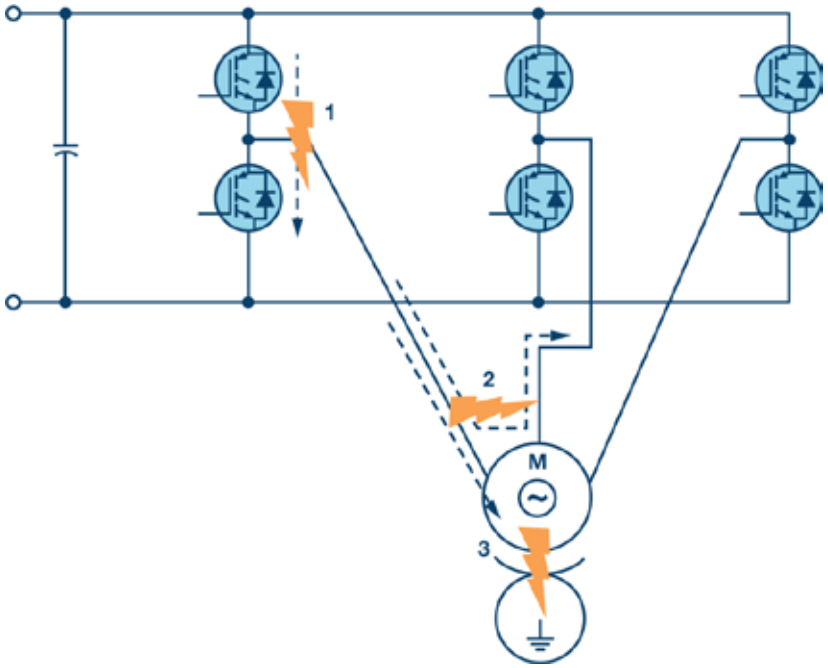


Figure 1. Typical short-circuit events in an industrial motor drive.

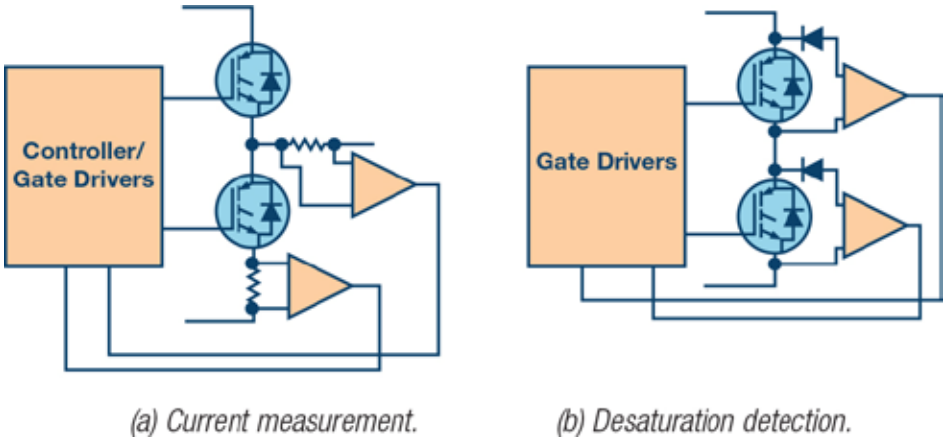


Figure 2. Examples of IGBT overcurrent protection techniques.

IGBT Short-Circuit Capability

The short-circuit withstand time of an IGBT is related to its transconductance or gain and the thermal capacity of the IGBT die. Higher gain leads to higher short-circuit current levels within the IGBT, so clearly lower gain IGBTs will have lower short-circuit levels. However, higher gain also results in lower on-state conduction losses, and so a trade-off must be made.1 Advances in IGBT technology are resulting in the trend of increased short-circuit current levels and consequently reduced short-circuit withstand times. In addition, the improvements in technology allow for the use of smaller die, 2 reducing module size but lowering thermal capacity, which further reduces the withstand time. There is also a strong dependency on the IGBT collector-emitter voltage, so the parallel trend toward higher dc bus voltage levels in industrial drives results in further reduction in short-circuit withstand times. Historically these have been in the 10 µs range, but in recent years they are trending toward 5 µs3 and down to 1 µs in some conditions.4 Moreover, the short-circuit withstand time can vary widely from device to device, so it is usually recommended to build in additional margin beyond the specified short-circuit withstand time, in IGBT protection circuits.

IGBT Overcurrent Protection

IGBT protection from overcurrent conditions is a critical part of system reliability, both in terms of asset destruction and indeed safety. IGBTs are not regarded as a fail-safe component and their failure can result in a dc bus capacitor explosion and complete drive failure.5 Overcurrent protection is typically implemented by means of current measurement or desaturation detection. These techniques are illustrated in Figure 2. For current measurement, measurement devices such as shunt resistors are required in both the inverter leg and phase output to cover shoothrough faults and motor winding faults. Fast acting trip circuitry in the controller and/or gate drivers must then shut down the IGBTs in a timely manner in order to prevent the short-circuit withstand time from being exceeded. The main disadvantage of this method is the requirement to include two measurement devices in each inverter leg, along with any associated signal conditioning

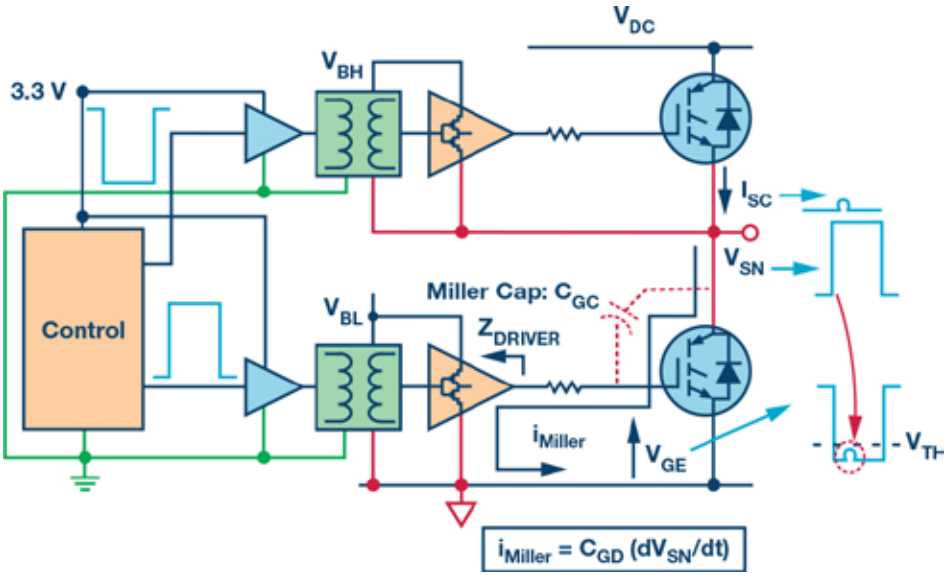


Figure 3. Miller induced inverter shoot-through.

and isolation circuitry. This can be alleviated by only adding shunt resistors in the positive and negative dc bus lines. However, in many cases, either a leg shunt resistor or a phase shunt resistor will be present in the drive architecture for the purposes of the current control loop and motor overcurrent protection, and these can also be potentially utilized for IGBT overcurrent protection - provided that the response time of the signal conditioning is fast enough to protect the IGBT within the required short-circuit withstand time.

Desaturation detection utilizes the IGBT itself as the current measurement component. The diodes shown in the schematic ensure that the IGBT collector-emitter voltage is only monitored by the detection circuit during the on-time, when in normal operation the collector-emitter voltage is very low (1V to 4V typically). However if a short-circuit event occurs, the IGBT collector current increases to a level that drives the IGBT out of the saturated region and into the linear region of operation. This results in a rapid increase in the collector-emitter voltage. The above normal voltage level can be used to indicate the existence of a short-circuit, and threshold levels for desaturation trip are typically in the 7 V to 9 V region. Importantly, desaturation can also indicate a gate-emitter voltage that is too low and that the IGBT is not being fully driven to the saturation region. Care needs to be taken in implementing desaturation detection to prevent false tripping. This can particularly occur during the transition from IGBT off state to IGBT on state when the IGBT is not fully in the saturated state.

A blanking time is generally inserted between the beginning of the turn-on signal and the point at which desaturation detection is activated in order to avoid false detection. A current source charged capacitor or an RC filter is also usually added to introduce a short time constant into the detection mechanism in order to filter spurious trips introduced by noise pickup. The selection of these filter components are a trade-off between providing noise immunity and acting within the IGBT short-circuit withstand time. Having detected the IGBT overcurrent, a further challenge is faced in turning off an IGBT at abnormally high current levels. Under normal operating conditions, the gate driver is designed to turn off the IGBT as rapidly as possible in order to minimize switching losses. This is achieved by means of low driver impedance and small gate drive resistance. If the same gate turn-off rate is applied for overcurrent conditions, the di/dt in the collector-emitter will be significantly larger due to the higher current change in a short time period. Parasitic inductance within the collectoremitter circuit due to wire bond and PCB trace stray inductance can result in large overvoltage levels being reached transiently across the IGBT (as $VL_{STRAY}=L_{STRAY}\times di/dt$). Thus, it is important to provide a higher impedance turn-off path when shutting the IGBT off during a desaturation event in order to reduce the di/dt and any potentially destructive overvoltage levels.

Apart from short circuits occurring as the result of faults within the system, momentary inverter shoot-through can also occur in normal operation. In normal operating conditions, IGBT turn-on requires that the IGBT be driven into the saturation region where the conduction losses will be minimized. This typically implies gate-emitter voltages of >12 V during the on state. IGBT turn-off requires that the IGBT be driven to the cutoff region of operation so that it can successfully block the reverse high voltage across it once the high-side IGBT has turned on. In principle this can be achieved by reducing the IGBT gate-emitter voltage to 0 V. However, a secondary effect must be taken into account when the transistor on the low-side of the inverter leg is turning on. The rapid transition of the switch node voltage on turn-on causes a capacitively

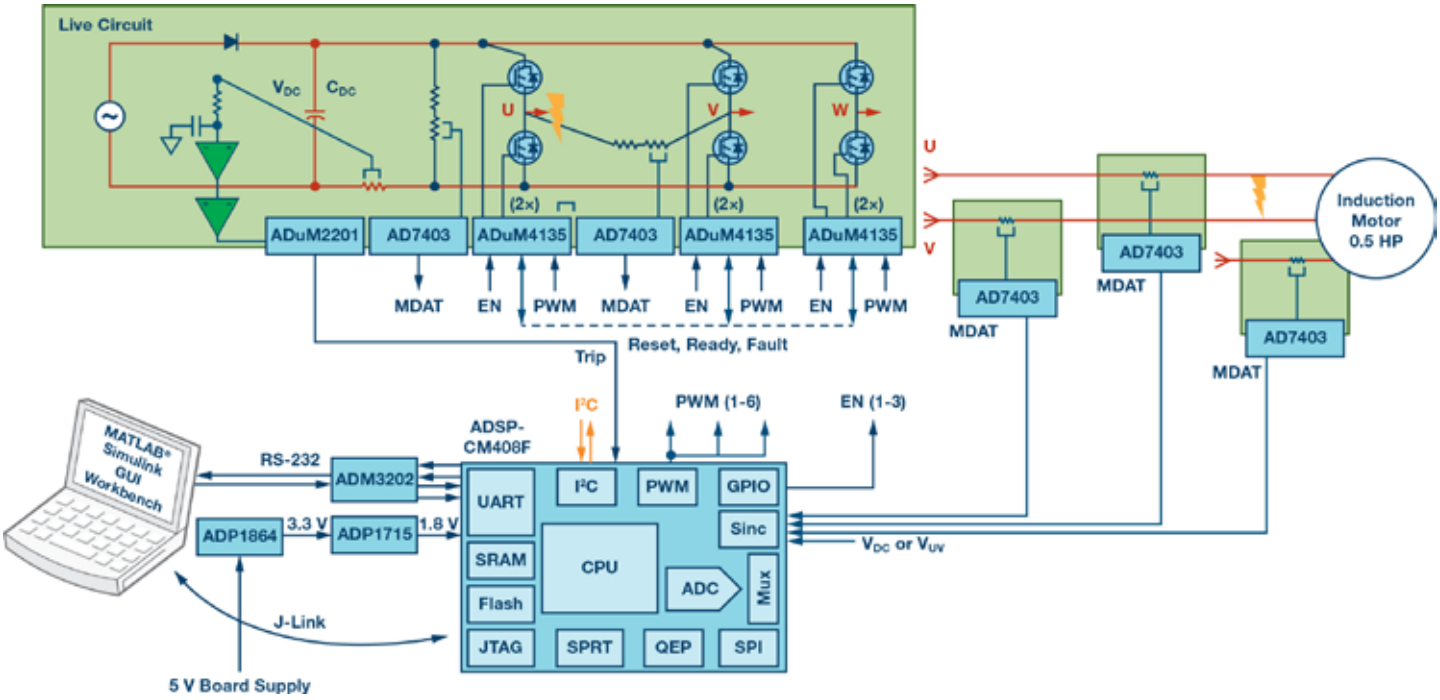


Figure 4. Experimental setup.

induced current to flow in the low-side IGBT parasitic Miller gatecollector capacitance (CGC in Figure 3). This current flows through the turn-off impedance of the low-side gate driver (ZDRIVER in Figure 3), creating a transient voltage increase at the low-side IGBT gate-emitter terminals, as shown. If this voltage rises above the IGBT threshold voltage, VTH, it can cause a brief turn-on of the low-side IGBT, resulting in a momentary inverter leg shoot-through since both IGBTs are turned on for a brief period. This will not generally result in IGBT destruction, but it does increase power dissipation and compromises reliability.

There are generally two approaches to addressing the induced turn-on of inverter IGBTs - using bipolar supplies and/or the addition of a Miller clamp. The ability to accept a bipolar power supply on the isolated side of the gate driver provides additional headroom for the induced voltage transient. For instance, a negative supply rail of -7.5 V means that an induced voltage transient of >8.5 V will typically be needed to induce a spurious turn-on. This is generally sufficient to prevent a spurious turn-on.

A complementary approach is to reduce the turn-off impedance of the gate driver circuit for a period of time after the turn-off transition has been completed. This is known as a Miller clamp circuit. The capacitive current now flows in a lower impedance circuit, consequently reducing the magnitude of the voltage transient. Additional flexibility in the control of switching rates can be provided by utilizing asymmetric gate resistors for turn-on and turn-off. All of these gate driver functions have a positive impact on overall system reliability and efficiency.

Experimental Example

The experimental setup utilizes a 3-phase inverter powered from the ac mains through a half wave rectifier. In this case this results in a dc bus voltage at 320 V, although the system can be also used up to dc bus voltage levels of 800 V. A 0.5 HP induction motor is driven under open loop V/Hz control in normal operation. The IGBTs are 1200 V, 30 A IRG7PH46UDPBF from International Rectifier. The controller is an ADSPCM408F Cortex®-M4F mixed signal processor from Analog Devices (ADI).

Phase current measurement is carried out using isolated Σ-Δ AD7403 modulators and isolated gate drive is implemented using the ADuM4135, a magnetically isolated gate driver with integrated desaturation detection, a Miller clamp, and other IGBT protection features. Short-circuit testing is carried out by manually switching a short-circuit between motor phases or between a motor phase and dc bus negative. The short-circuit to earth is not tested in this example. The controller and

Table 5 - Simplified overview of ARM Cortex M CPUs

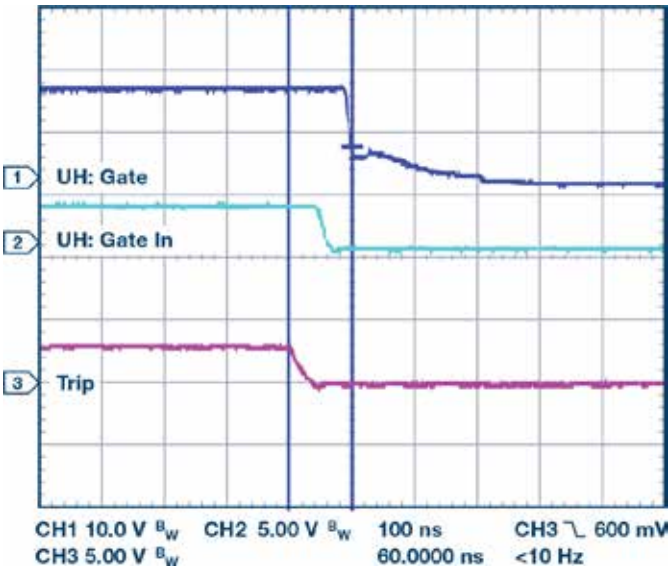


Figure 6. Overcurrent shutdown timing delay (Ch1: gate-emitter voltage 10 V/div, Ch2: PWM signal from controller 5 V/div, Ch3: active low trip signal 5 V/div; 100 ns/div).

power boards are shown in Figure 5. These are the ADSP-CM408F EZ-kit®6 and the EV-MCS-ISOINVEP-Z isolated inverter platform,7 both available from Analog Devices.

IGBT overcurrent and short-circuit protection are implemented using a range of methods in the experimental hardware. These are:

- DC bus current sensing (inverter shoot-through fault)
- Motor phase current sensing (motor winding faults)
- Gate driver desaturation detection (all faults)

For the dc bus current sensing circuit, a small filter must be added in order to avoid false tripping, since the dc bus current is discontinuous with potentially high noise content. An RC filter with 3 µs time constant is utilized. Having detected the overcurrent, the remaining delays to IGBT shutdown are delays through the op amp, comparator, signal isolator, trip response time in ADSP-CM408F, and gate driver propagation delay.

These amount to an additional 0.4 µs, resulting in a total fault-to-turn off time delay of 3.4 µs - well within the short-circuit time constant of many IGBTs. Similar timing applies to motor phase current sensing using the AD7403 in conjunction with the integrated overload detection sinc filters on the ADSP-CM408F processor. These operate well with a sinc filter time constant of around 3 µs.8 The remaining system delays in this case are only due to the internal routing of the trip signal to the PWM unit and the gate driver propagation delay, since the overload sinc filters are internal to the processor. Along with the reaction time of the current sense circuitry or digital fast filters, the very short propagation delay of the ADuM4135 in both instances is critical to achieving viable fast overcurrent protection using either of these methods. In Figure 6, the delay between the hardware trip signal, the PWM output signal, and the actual gate-emitter waveform of the upper IGBT in one of the inverter legs is shown. The total delay to commencement of IGBT turn-off is seen to be around 100 ns. Gate driver desaturation detection can act significantly faster than the overcurrent detection methods described previously, and is important for limiting the extent to which short-circuit currents are allowed to rise, thus enhancing overall system reliability beyond the levels achievable even with fast overcurrent protection. This is illustrated in Figure 7. As the fault occurs the current starts to increase rapidly - in reality the current is much higher than shown as the measurement is taken with a bandwidth limited 20 A current probe

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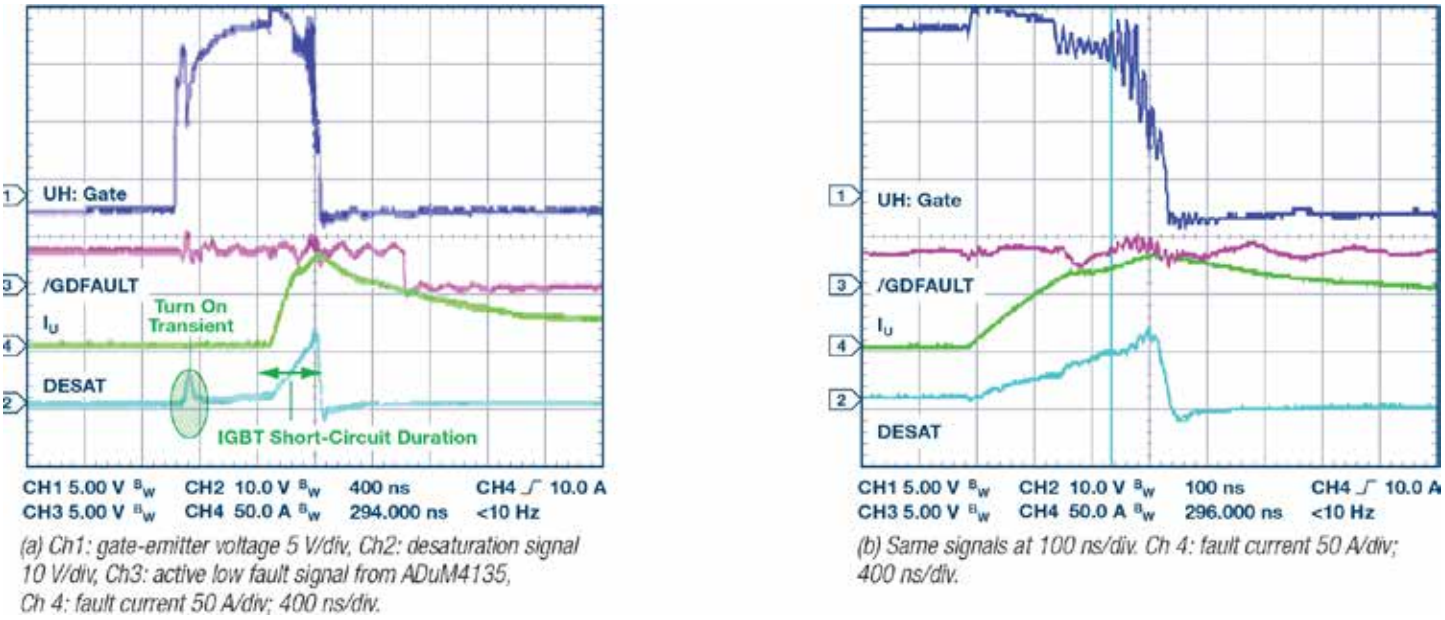

Figure 7. IGBT short-circuit detection.

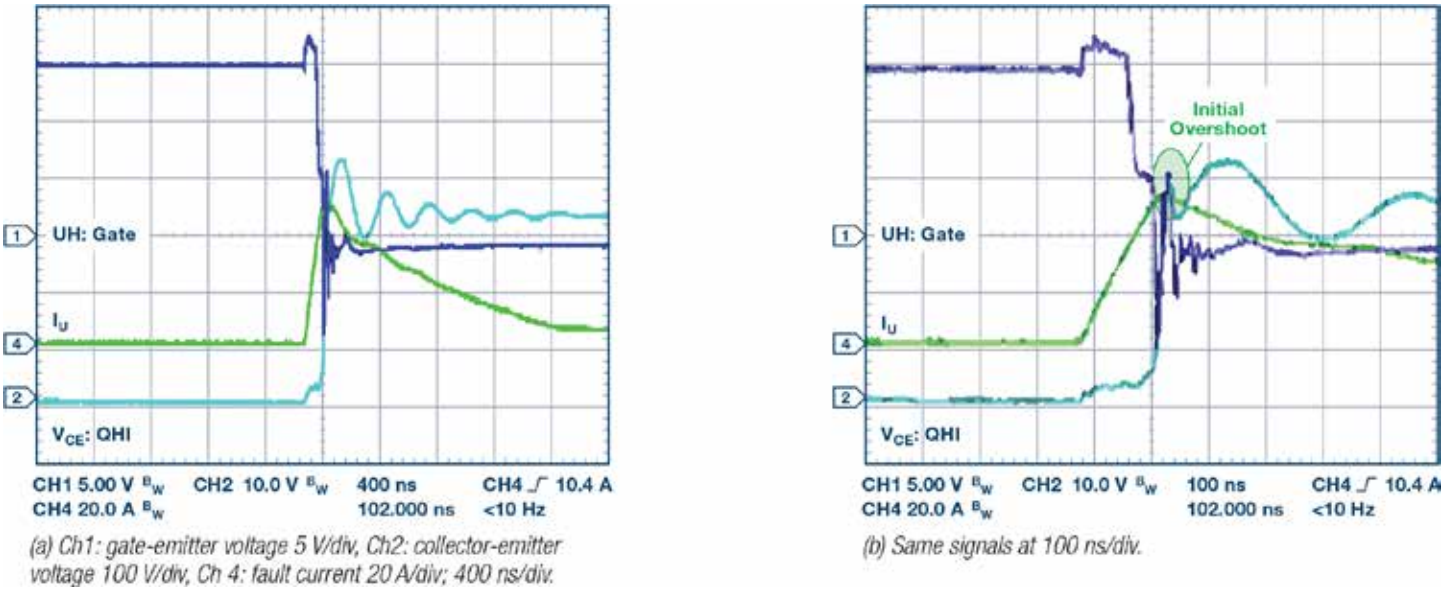

Figure 8. IGBT short-circuit turn-off.

for illustration only. The desaturation voltage reaches the 9 V trip level and the gate driver begins to shut down. It is evident that the entire duration of the short-circuit is <400 ns. The long tail on the current is the decay of the inductive energy by current freewheeling in the antiparallel diode of the lower IGBT. The initial increase in the desaturation voltage during turn-on is an example of the potential for spurious desaturation detection due to the transient state of the collectoremitter voltage. This can be eliminated by increasing the desaturation filter time constant to add additional blanking time. Figure 8 shows the collector-emitter voltage across the IGBT. There is an initial controlled overshoot of about 80 V above the 320 V_{DC} bus voltage due to the higher impedance in the turn-off during desaturation protection. The circulating of the current in the lower antiparallel diode and the circuit parasitic actually results in a slightly higher voltage overshoot up to about 420 V.

The value of Miller clamping in preventing inverter shoot-through in

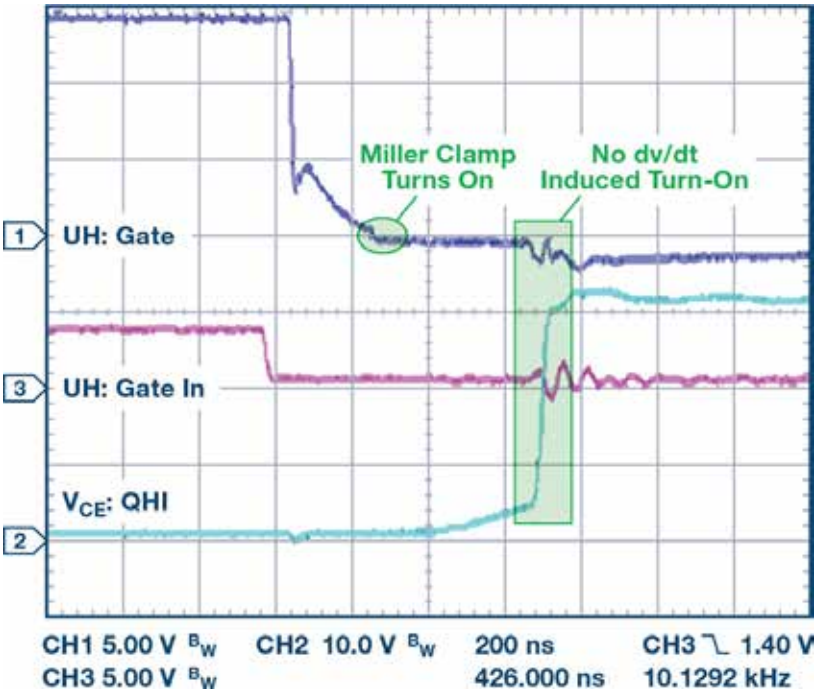

Figure 9. Miller clamping on turn-on. Ch1: gate-emitter voltage 5 V/div, Ch2: PWMsignal from controller 5 V/div, Ch 3: collector-emitter voltage 100 V/div; 200 ns/div.

normal operation is illustrated in Figure 9.

Summary

Overcurrent and short-circuit detection and turn-off in a very short time period are becoming ever more important as the short-circuit withstand time of IGBT decreases down to 1 µs levels. Industrial motor drive reliability is strongly linked to the IGBT protection circuits. This article has outlined some approaches to handling this issue, and has presented experimental results that underline the value of robust isolated gate driver ICs such as the ADuM4135 from Analog Devices.

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About the Author

Dara O'Sullivan is a system applications engineer for the Motor and Power Control Group at Analog Devices. His area of expertise is power conversion and control in ac motor control applications. Dara received his B.E., M.Eng.Sc., and Ph.D. from University College Cork, Ireland.

Troubleshooting Clock Jitter and Identifying PDN Sensitivities

› Steve Sandler, Picotest

Quickly identify PDN sensitivities, in-circuit, including clock jitter source locations, using a simple probe-based solution.

Power distribution network (PDN) noise is one of the most common issues in low power applications. Whether you are powering ADCs, clocks, LNAs, digital data networks or sensitive RF applications, properly tuning your power supply is of the utmost importance. These sensitive circuits can be disrupted by just a few millivolts of power supply noise or even less. Due to this extreme sensitivity and the interaction between the power supply, distribution network, and load, power supply troubleshooting often becomes necessary.

Due to the interactions between the source and load impedance, the troubleshooting must be performed in-circuit and there is often very limited physical access. As a result, this can be a time consuming process.

Even in a circuit that appears to be fully functional it's generally a good idea to evaluate power supply sensitivities. It's the best way to identify potential issues that could crop up as a result of operational and environmental tolerances.

In this sample application, we will demonstrate some simple test tools that couple with your spectrum and network analyzers that help support power supply noise source investigation.

Figure 1 shows the Picotest VRTS3 training demo board, which includes a variety of sample circuits, supporting many types of measurements.

One of these sample circuits is a 125 MHz clock (OSC401), powered by a low dropout (LDO) voltage regulator (U301). Four different output capacitors can be connected or disconnected from the LDO using a four-position dipswitch (S301), altering the stability of the power supply.

The circuit schematic in Figure 2 shows the LDO linear regulator (LT1086) that powers the 125 MHz clock oscillator, OSC401 through a slide switch (SEL1). Of note is the 0.01 uF decoupling capacitor C402 (on the right).

Identifying a power supply noise sensitivity can be accomplished quickly and easily using a wide band harmonic comb generator and a 1-port passive transmission line probe.

The J2150A harmonic comb provides a wideband noise source with a 50Ω output impedance. It is contained in an ultra-portable USB "stick" form factor. The harmonic comb provides

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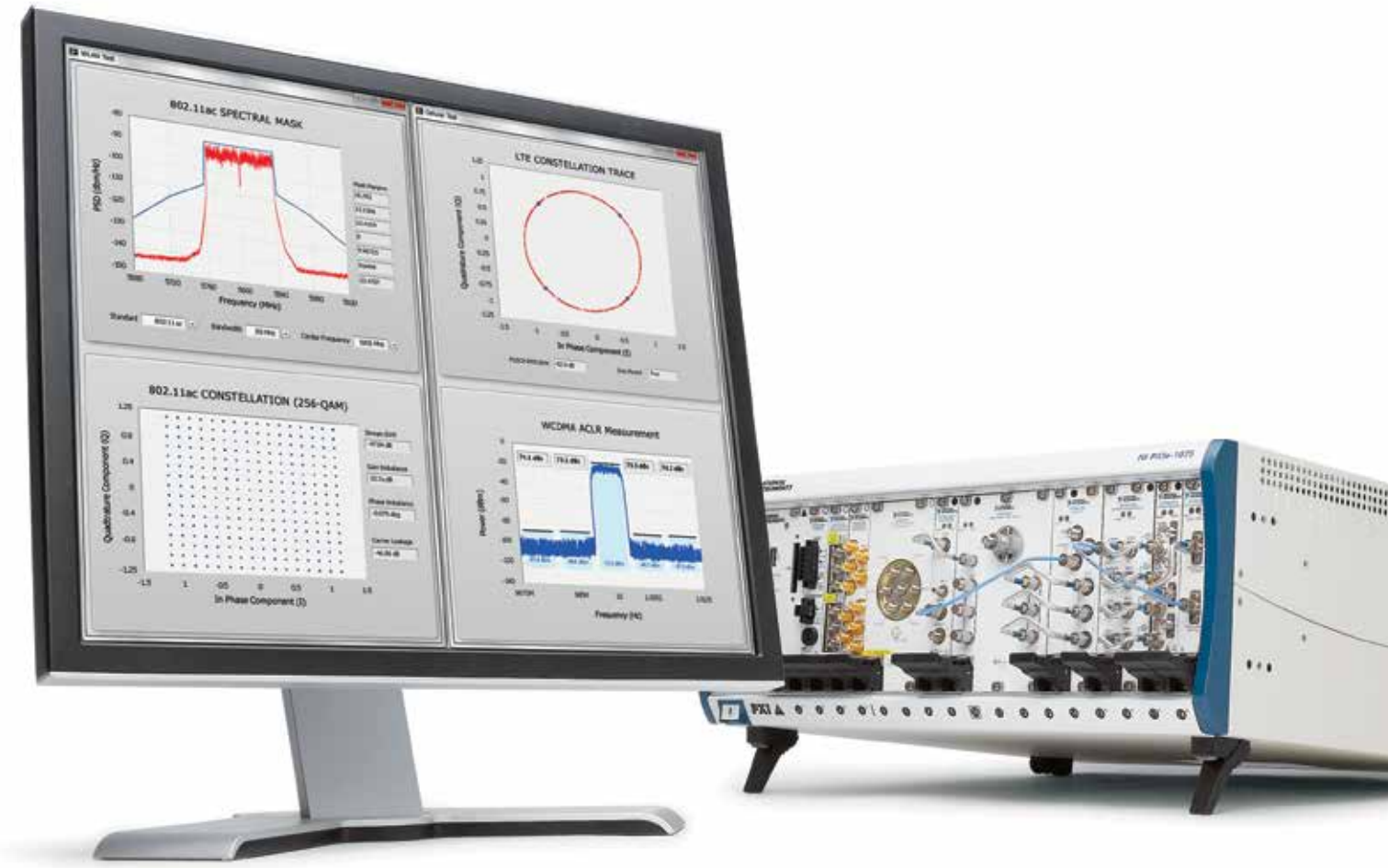

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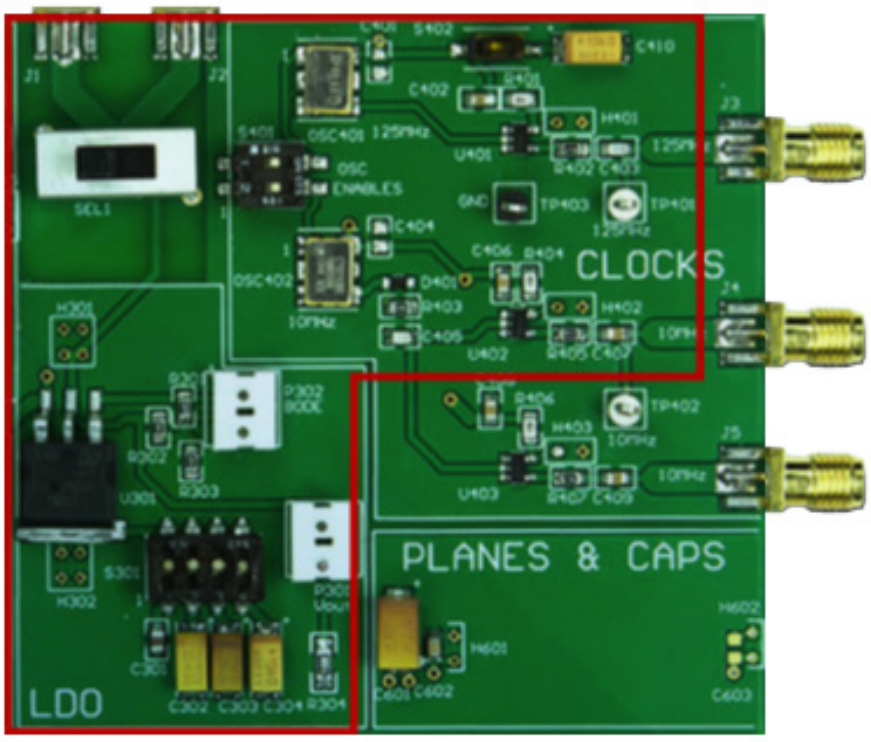


Figure 1: The Picotest VRTS3 training demo board showing the LDO and clock layout.

noise over a frequency range of 1kHz to more than 1GHz in three frequency ranges. The ranges are centered around 1kHz, 100kHz, and 8MHz. Harmonics are generated by time and frequency dithering of the output impulses. The comb can step through these ranges automatically or be locked onto a single frequency range. While most instruments have several unused USB ports available, the comb can also be powered from the popular cell phone backup batteries for a portable solution.

A wideband DC block is generally included between the comb injector and the probe in order isolate the 50Ω DC impedance from the circuit being tested. The clock spectrum is viewed on an oscilloscope with a spectrum analyzer option, a signal source analyzer or a spectrum analyzer. The voltage regulator stability and

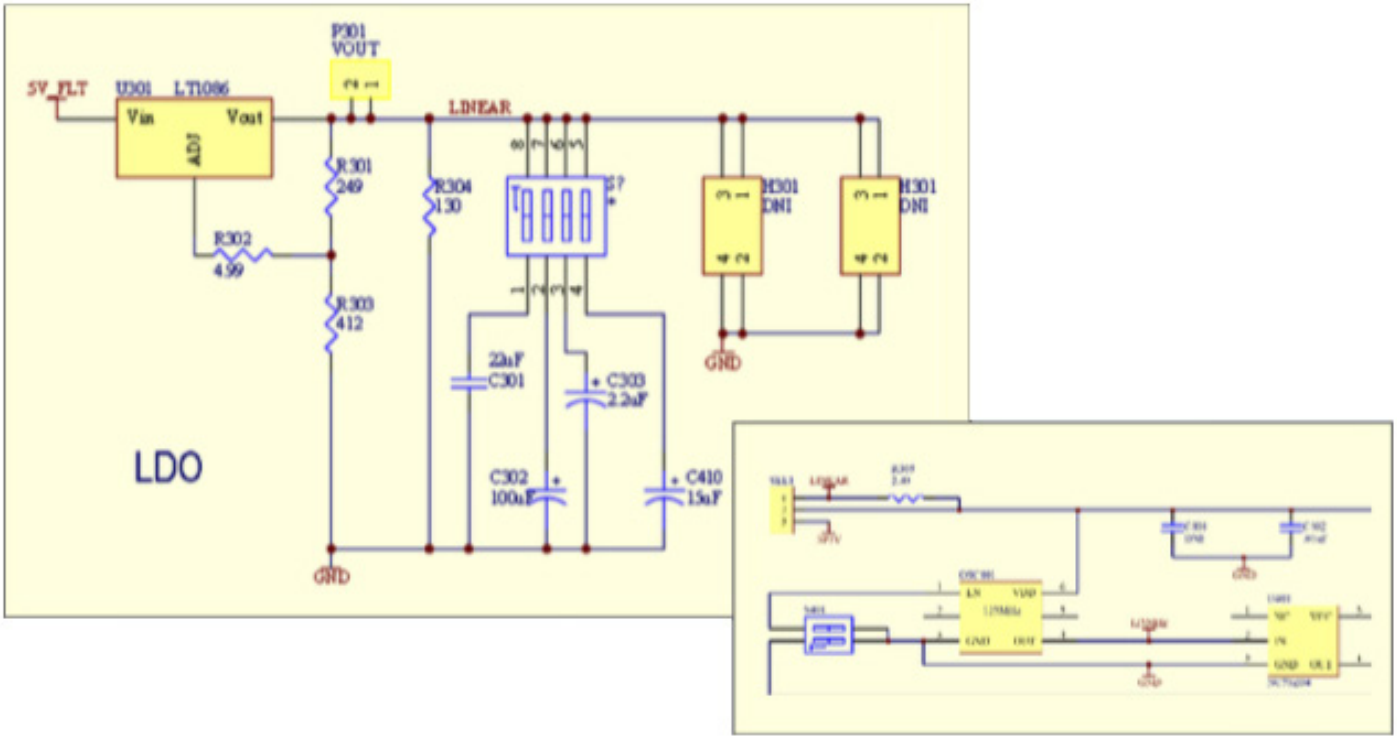


Figure 2: The LDO and clock circuitry

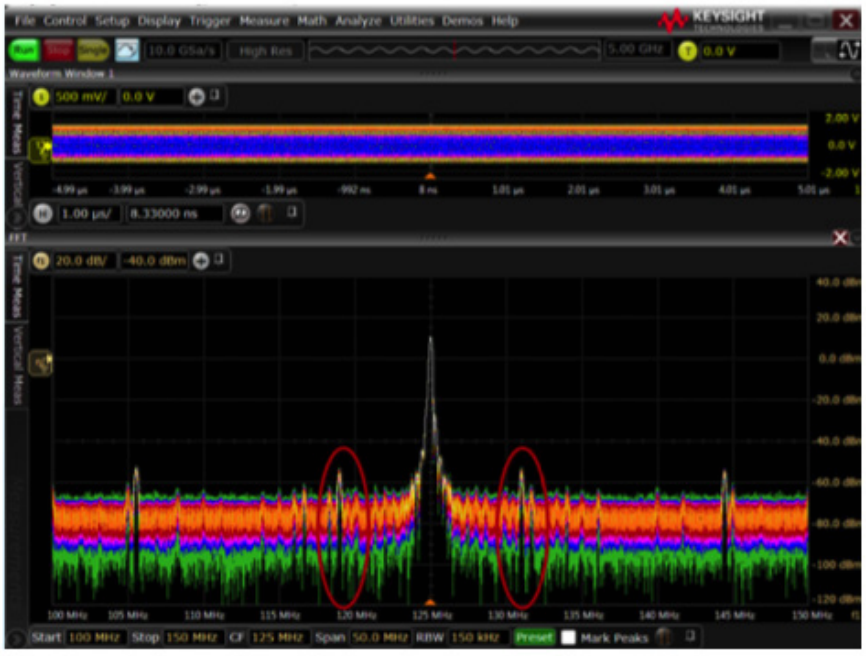


Figure 3: Clock spurs at approximately 6 MHz o set are highlighted in this oscilloscope spectrum plot. These spurs are used to demonstrate a simple and fast troubleshooting technique.

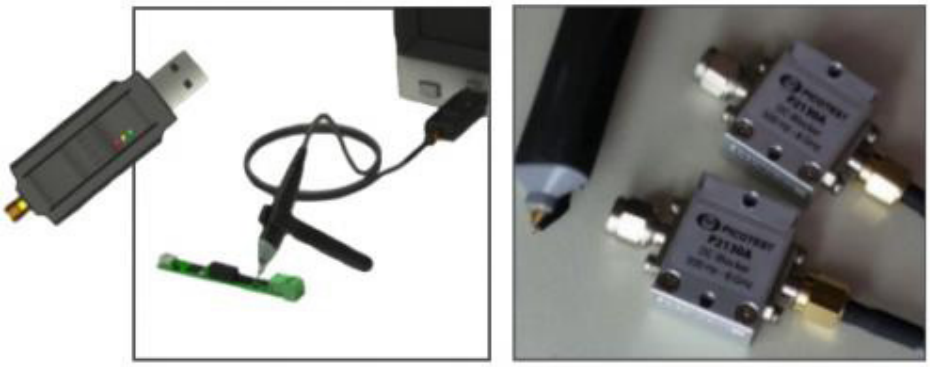


Figure 4: Simple but e ective tools support PDN interrogation and clock jitter assessment. These include a J2150A harmonic comb broadband signal generator (left) along with 1-port (center) and 2-port bi-directional 50Ω passive probes and DC blockers (left).

distribution impedance are easily seen as sidebands or jitter in the clock spectrum.

The Picotest transmission line probes are unique, providing unity gain, bidirectional 50Ω connections to various instruments with a comfortable browser style head for probing the power distribution network. This allows the probe to be used to inject signals, as in this example, or to measure noise using the same probe. The probe connection is a generic 50Ω SMA connector, allowing connection to most instruments.

In this example, the harmonic comb injects a broadband signal into the clock's decoupling cap (C402) using the 1-Port Probe, as seen in Figure 4. The clock's spectrum is monitored at SMA connector, J3.

Moving the noise injection point to the linear regulator (same printed circuit board trace but downstream of the clock) we notice that the clock sideband noise is much smaller in Figure 7 at -45dBc. This information tells us that resonance is between the regulator and the clock. The resonance is comprised of the inductance of the printed circuit board trace and the decoupling capacitor, C402.

Having located the resonance at the clock, we can calculate the characteristic impedance of the PCB connection using the value of the decoupling capacitor (10 nF) and the 7.5 MHz resonant frequency (7.5 MHz). The characteristic impedance can be calculated as 1/(2*PI*7.5 MHz*10 nF), in this case 2.1Ω. Placing SEL1 switch in the center (OFF) position inserts a 2.4Ω resistor (R305) between the linear regulator and the clock, damping the resonance. The elimination of the 7MHz clock spectrum sidebands, seen in Figure 8 con rms that the resonance has been effectively damped by increasing the series resistance between the linear regulator and the clock.

The resonance and the damping effectiveness can easily be confirmed by measuring the impedance at the clock's decoupling capacitor with a vector network analyzer (VNA). Measurements are shown in Figure 9 for two different linear regulator output capacitors, as well as, the insertion of R305.

While the sidebands may not have

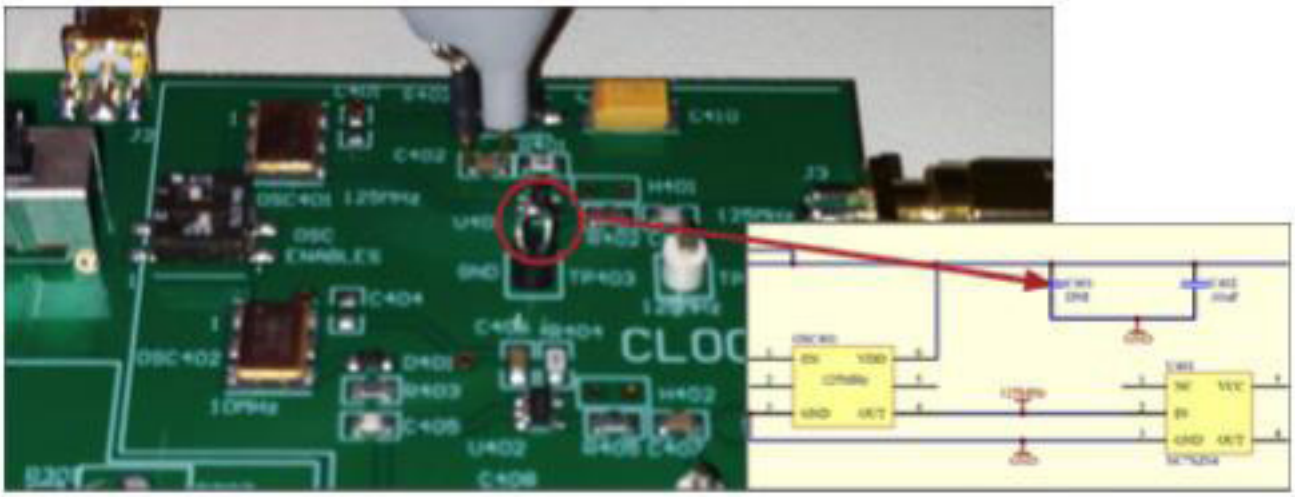


Figure 5: The J2150A harmonic comb (inset and in Figure 3) is connected to the 1-Port probe via a P2130A DC Blocker and used to inject a signal into C402 (VDD of a 125MHz clock oscillator). The clock spectrum is monitored at SMA connector, J3.

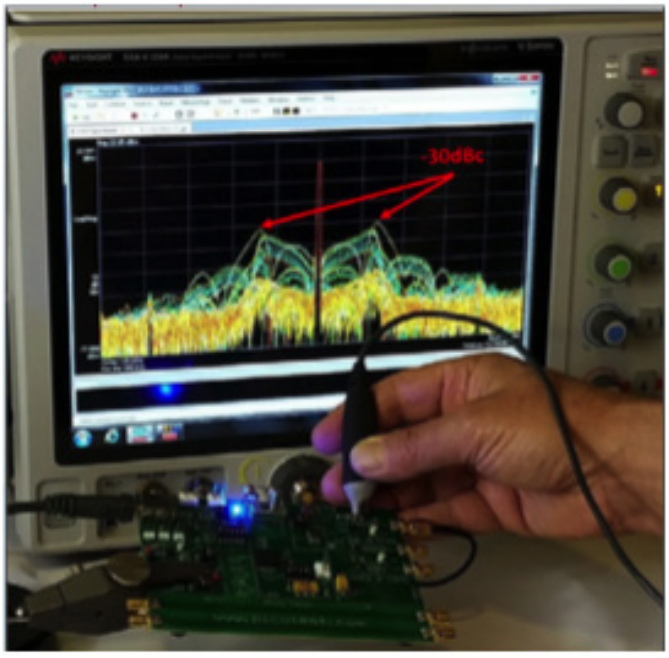


Figure 6: The PDN interrogation using the comb's search mode signal set reveals a resonance at approximately 7.5MHz as seen in the spectrum sidebands around the clock fundamental frequency. Note the peaks are approximately -30 dBc.

seemed all that severe, they can significantly impact performance—much more so than they might otherwise appear. First, note that the sidebands in Figure 3 appear at 6 MHz, while we determined the PCB resonance is at 7.5 MHz. Second, the measurement in Figure 9 shows that at 6 MHz the impedance is approximately 5 dB lower than at the 7.5 MHz peak and at 9 MHz the impedance is approximately 15 dB lower than the 7.5 MHz peak.

So, what excited the resonance? There is a 2.8 MHz switching point-of-load (POL) regulator also located on the VRTS3 demo board. The 2nd and 3rd harmonics are close enough to the resonant peak to impart clock noise. We can confirm the POL switching frequency as the noise generator, since an enable switch is included on the VRTS3 training board for this purpose. If we turn off the switching regulator the clock sidebands at 6MHz disappear. This also clearly demonstrates why we want to interrogate the circuit even if it appears to be functional.

The switching regulator operating frequency has a tolerance of 750 kHz while the decoupling capacitor also has tolerances. These tolerances can easily shift the second harmonic of the switching regulator to occur exactly

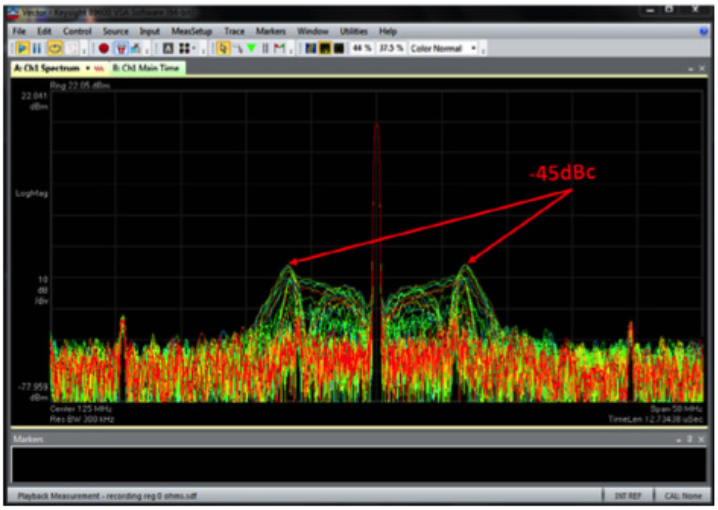


Figure 7: By injecting the noise at di erent locations within the PDN, the noise source is quickly located. Note the sidebands are about 15dB lower than in Figure 6. This tells us that the resonance is at the clock and not at the regulator.

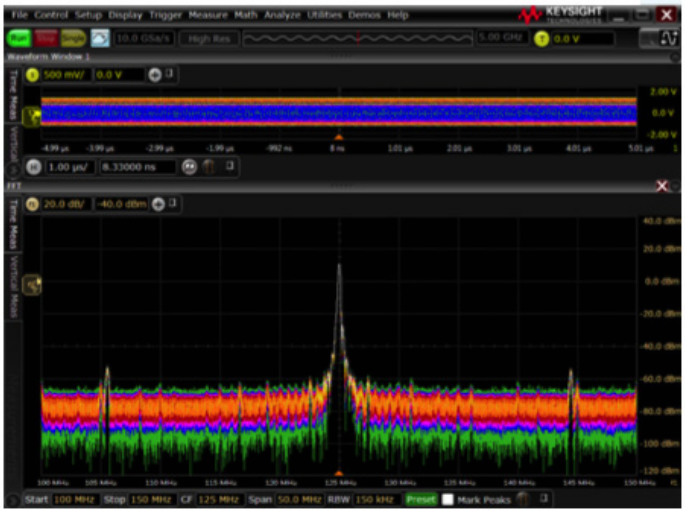


Figure 8: The 7MHz clock sidebands have been eliminated by inserting the series resistor between the regulator and the clock, damping the PCB resonance.

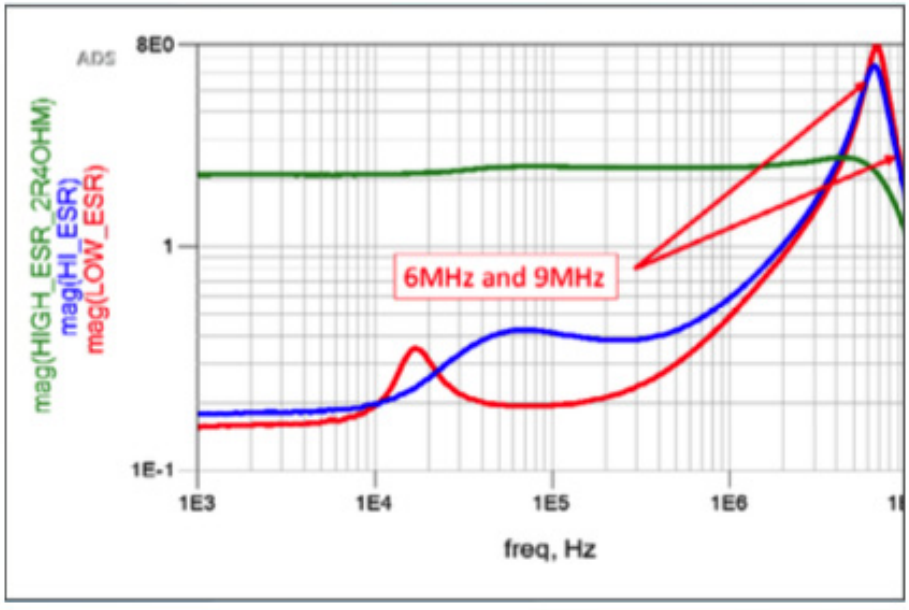


Figure 9: The 7.5 MHz resonance (red, blue traces) is clearly seen for two different linear regulator output capacitors, selected with switch S301. The insertion of the 2.4-Ω resistor damps the resonance (green trace), reducing the impedance at 7.5MHz by approximately 15 dB.

at the frequency of the impedance peak, increasing the clock noise significantly. While you would not likely see this frequency alignment occur in a nominal test, you are much more likely to know about its possibility via this PDN interrogation.

In summary, we quickly identified a PDN sensitivity that resulted in increased clock jitter. We identified the noise, determined its source and characteristic impedance, and easily corrected the issue by flattening the power rail impedance at the clock. This was all accomplished in just a few minutes using a highly portable harmonic comb generator (Picotest J2150A), a handheld 1-Port probe (Picotest P2100A) and an oscilloscope (Keysight Infiniium S).

Picotest offers several bundled solutions for optimizing, testing, and troubleshooting power integrity issues, such as clock jitter, with support for various instruments and measurement domains. The recently introduced J2150A harmonic comb generator paired with a P2100A 1-port probe is only one, albeit powerful, solution.

Anti-Tamper Technology: Safeguarding Today's COTS Platforms

› Steve Rohm, Edco Technologies

Introduction

Secure embedded computer and communications systems are critical for mission success in today's environment of escalating cyber threats. Data integrity must be protected as it is processed, stored, and transmitted. The strategic risk management of these systems is known as Information Assurance (IA), which entails a combination of physical, technical, and administrative controls. At the core of an assured system is an authentic, trusted foundation based on Anti-Tamper (AT) safeguards using layered security features at the hardware, firmware, and software level. Abaco Systems is responding to the need for assured systems by incorporating product features that enable anti-tamper safeguards. This paper focuses on the use of COTS anti-tamper frameworks to support secure platforms and provide information assurance.

Information Assurance: The Big Picture

The concept of Information Assurance pervades the design, acquisition, installation, operation, upgrade and replacement phases of defense-based information systems. The goal is to maintain an appropriate level of confidentiality, integrity, authentication, non-repudiation, and availability of information.

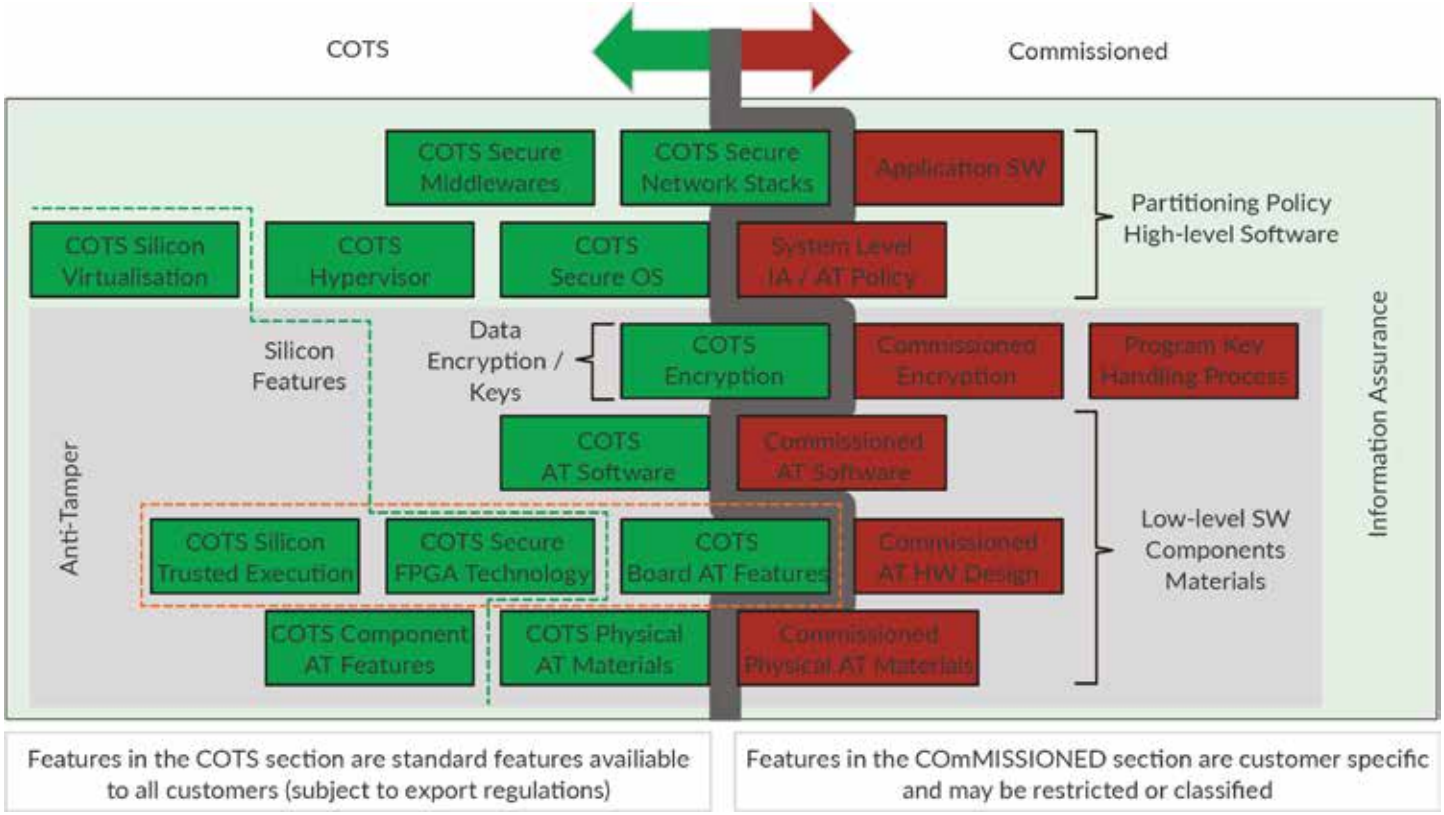
The standards for ensuring Information Assurance and Anti-Tamper are maintained through various national and international channels.

U.S. DoD Instructions and Directives

The Department of Defense established Instruction 5200.39 to mitigate the exploitation of Critical Program Information (CPI) and extend the operational effectiveness of military systems. These systems are to comply with directive 8500.01E, an Information Assurance policy, along with directive 8500.02, prescribed procedures to protect and defend information networks and systems, including anti-tamper capabilities.

Federal Information Processing Standards

The US government provides publicly-announced Federal Information Processing Standards (FIPS) for use in computer systems by government contractors, and the National Institute of Standards and Technology (NIST) issues the FIPS 140 Publication Series to coordinate the requirements for cryptographic modules which includes hardware and software. FIPS 140-2 establishes the Cryptographic Module Validation Program (CMVP) as a



joint effort with the Communications Security Establishment (CSE) for the Canadian government. Laboratory testing qualifies modules to one of four levels of security. FIPS140-3 is a draft standard which aims to incorporate additional concepts and provide modified requirements and limits within the four levels of security.

Going Global: Common Criteria

The Common Criteria for Information Technology Security Evaluation (CC), or ISO/IEC 15408, is an international standard for computer security certification. It is a unification of European, Canadian, and US DoD standards. Profiles and functional requirements drive design, and laboratory testing results in an Evaluation Assurance Level (EAL) which indicates the robustness of a security solution. The Common Criteria Recognition Arrangement (CCRA) provides for member countries to mutually recognize evaluated systems. CC is typically used for firewalls and operating systems, and does not specify cryptographic implementation.

Anti-Tamper in the COTS Domain

In-house design expertise and relationships with key partners and suppliers make it possible to offer standard COTS products with optional security features. However, it becomes necessary to draw a distinction between COTS capabilities and Commissioned content - sensitive, restricted, or classified customer-specific methods. See Figure 1. The AT features highlighted in yellow are the focus of this paper. The COTS/Commissioned dichotomy leverages lower-cost, reliable COTS software, partitioning, encryption, silicon features, and physical materials, while allowing customers to plug-in their highly-specialized proprietary technologies, policies, and procedures. For example, the hardware interconnect design - such as inputs from tamper detection sensors - can be COTS, while programmed behavior (such as in FPGAs) for tamper response can be Commissioned. The Commissioned behavior is never exposed since it is not part the COTS design process, yet the anti-tamper framework is tightly coupled with the architecture.

Prevent, Detect, Respond: The 3 Tenets of Anti-Tamper

An attacker seeks to gain information from a secure system. Attacks can be passive or active in nature. Passive attacks include side-channel analysis to ascertain secrets from timing, dynamic power consumption, or electromagnetic leaks; as well as probing circuits or imaging

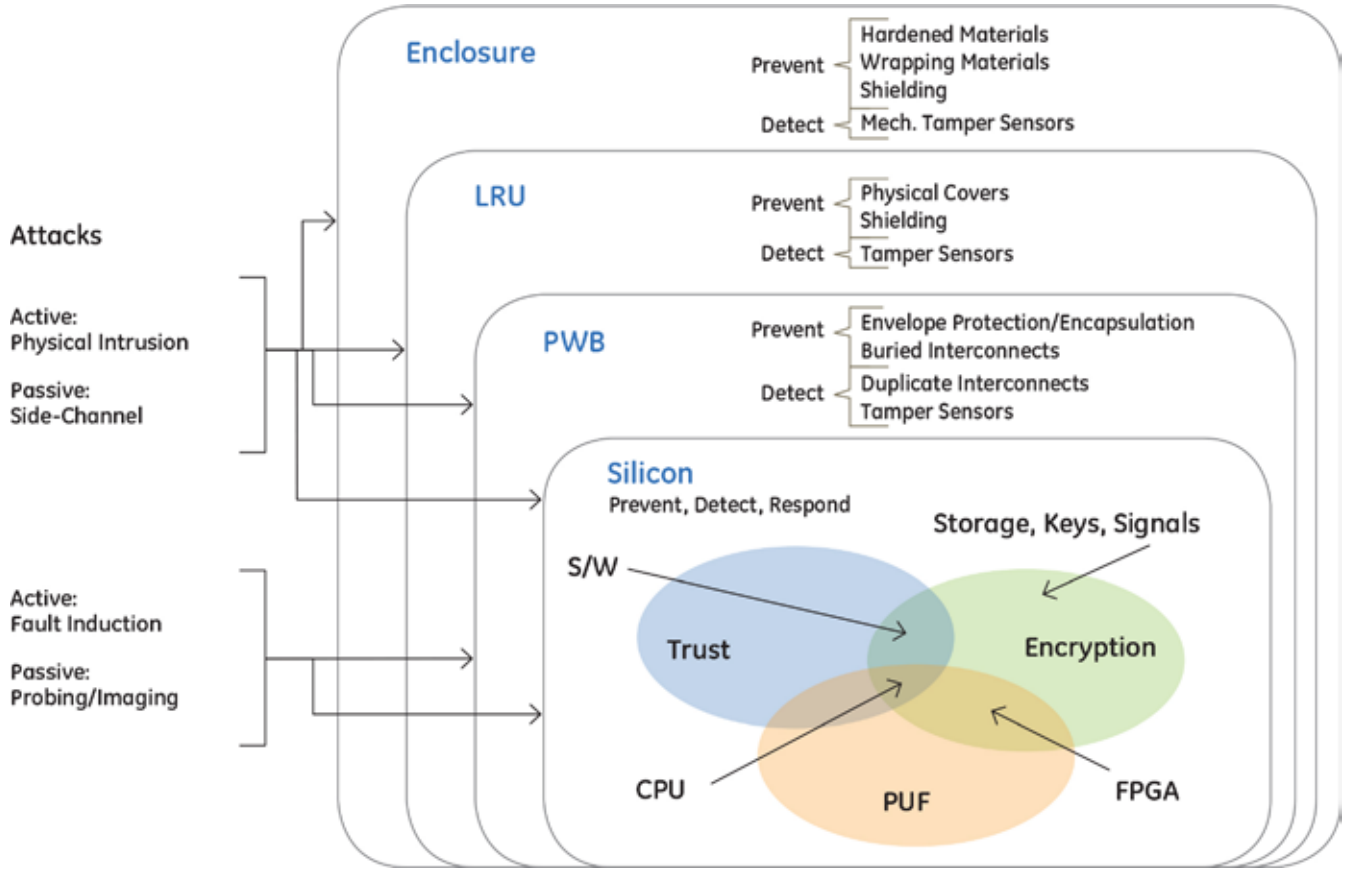


Figure 2 Implementation of AT Safeguards

components. Active attacks include physical intrusion and hardware modification; as well as fault induction through signal corruption, protocol attacks or malicious software.

Prevent

Ideally, AT in a secure system prevents attacks from compromising it, but in the event that a threat is more sophisticated than the security strategy, it will at least work to delay the acquisition of critical information, in the hopes that a sufficiently long time delay will render that information useless. Examples of preventive safeguards are shielding, encapsulation, and encryption.

Detect

AT safeguards can also detect threats, and then actively or passively thwart them. Protection meshes and low-power or no-power tamper sensors can signal breaches, and physical unclonable functions (PUFs) in silicon provide a means to uniquely identify devices for validation.

Respond

When a threat has been detected, the system can actively respond, often by destroying its own critical elements. Zeroizing memory resources, disabling communication interfaces, erasing encryption keys, and inducing pyrotechnic or high current damage are examples of responses to a tamper event. Figure 2 shows some basic AT features in four layers of an example system: the enclosure, the line replaceable unit (LRU) or pluggable circuit board, the printed wiring board (PWB), and the silicon. Figure 3 shows two Abaco products: a 6U OpenVPX rugged single-board computer and a ruggedized display computer.

AT from the Ground Up

The threat model for a given system will vary depending on how it is deployed, the capabilities of the attacker, the type of critical technology or program information, and other factors. Therefore the goal is to provide useful COTS-based anti-tamper options, and allow the inclusion of Commissioned aspects to best address specific threats. To achieve this, AT principles are incorporated into the early stages of hardware design.

The Root of Trust

At the lowest level, a robust AT design requires a root of trust, or a certified CPU-based hardware/firmware element that provides the basis for a secure boot process. The root of trust validates the next stage, starting a sequential process that builds the trusted system as each stage is validated. This protects against executing untrusted code, detects use of modified security values, and prevents software attacks. Intel and Freescale processors provide methods to that end using cryptographic keys and certified, un-modifiable BIOS or bootROMs. These features are discussed in the following sections. Another critical component is the FPGA-based security hub - a central system monitor that detects and provides customized responses to tamper events. The security hub works with the trusted processing system and provides independent control to manage AT policies. Finally, encrypted storage is used to protect data and application software. An example architecture is shown in Figure 4.

COTS Trusted Execution

Intel Trusted Execution Technology

Intel Trusted Execution Technology (TXT) defines a safe, isolated software execution space that cannot be observed or modified by unauthorized software. The execution space has dedicated resources that are managed by the processor, chipset, and operating system kernel. The

Figure 3 Abaco 6U OpenVPX single-board computer and a Rugged System Enclosure

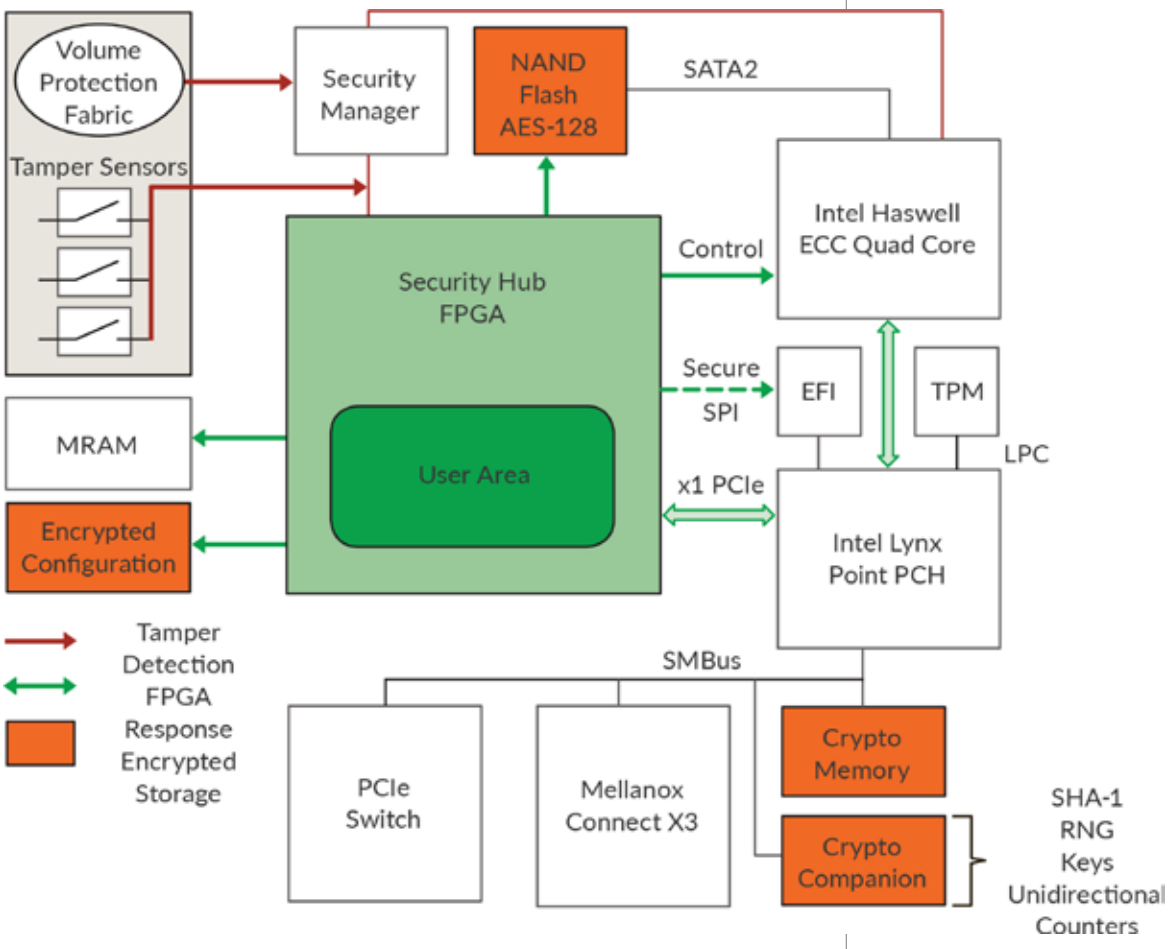


Figure 4 The FPGA Security Hub in an Intel-based Architecture

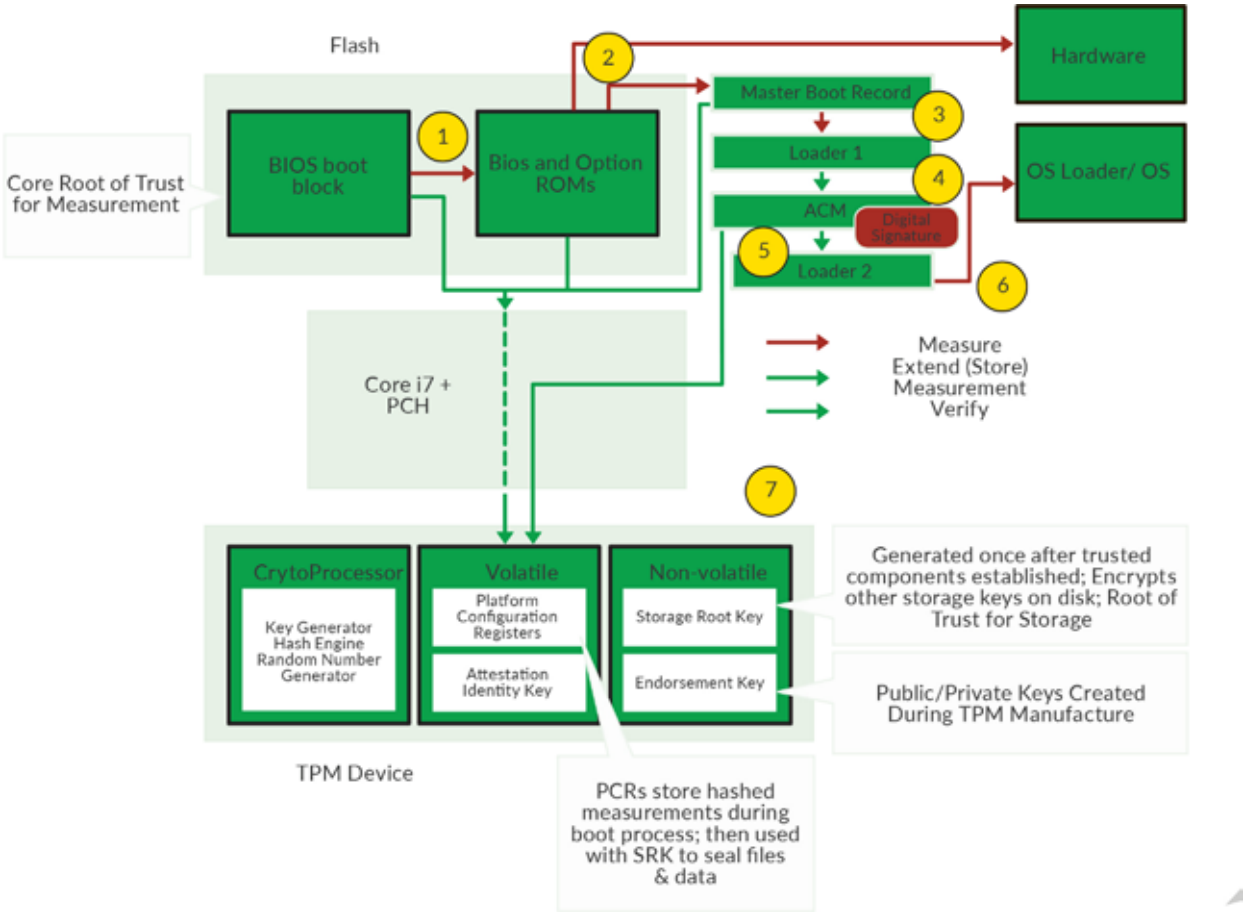


Figure 5 Intel TXT

CPU provides protected partitions for hardened access to memory. The platform controller hub (PCH) enforces memory protection policy and provides protected data transfer to graphics hardware and input/output devices. The PCH also interfaces to the trusted platform module (TPM), a hardware device that generates and stores cryptographic keys, stores the platform state during the secure boot process, and supports reporting or attestation of the secure state of the system. Figure 5 shows the steps for a secure Intel TXT boot process.

Measure and Extend:
1. After system reset, the BIOS boot block acts as the core root of trust for measurement (CRTM), and measures the system BIOS, the first initially untrusted component. The measurement is a hash value of BIOS code, and is stored in one of the TPM's platform configuration registers (PCRs). The storage operation is actually a concatenation of the existing PCR contents with the new measurement information, which means the stored value reflects any changes made to the system since the last boot. This process is called extension.
2. The BIOS measures the hardware and the master boot record, and extends the PCR.
3. The master boot record measures a pre-loader for Intel TXT, Loader 1, and extends the PCR. The pre-loader prepares memory for instructions that initiate trusted execution.

Verify:
4. Loader 1 verifies the authenticated code module (ACM). The digitally signed by Intel that verifies a list of applications that can be run next.
5. The ACM verifies Loader 2, which verifies platform configuration registers, system management mode code, and the operating system loader.

Execute:
6. Operating system loader prepares for and then launches the operating system.

TPM operation:
7. The secure operating system can

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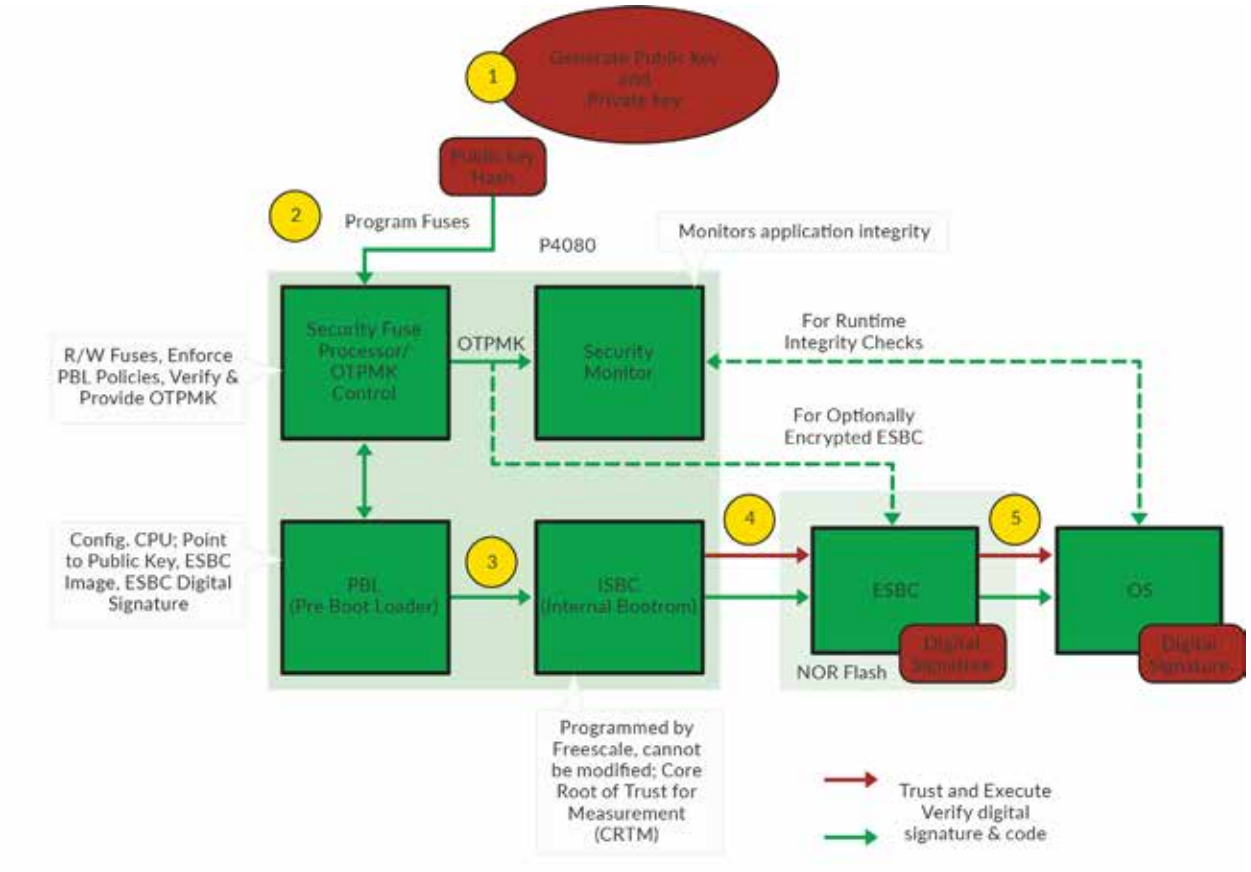


Figure 6 Freescale Trust Architecture

then take ownership of the TPM, which provides the ability to seal (encrypt) data using the current PCR values. The data can only be unsealed (decrypted) if the PCR values are the same as they were at the time the data was sealed. Ownership of the TPM can only be changed if the TPM is cleared, and any attempt to unseal data sealed by the previous key owner will fail. In networked so act as a root of trust for reporting (RTR) by signing a quote of its current PCR set.

Freescale Trust Architecture

Freescale's QorIQ Trust Architecture provides secure boot, secure runtime, secure debug, tamper detection, and devicespecific secret key usage. This prevents the CPU from executing untrusted code and prevents the use of modified security keys. Security features are self-contained in the QorIQ system-on-chip - no external trusted devices are required. Figure 6 shows the steps for the Freescale secure boot process.

Code Signing and Provisioning:

1. The trust architecture relies on the generation by the user of a public and private key pair, which can be accomplished using Freescale code signing tools. The private key is used to digitally sign all code that is to execute on the QorIQ processor. The private key must be protected. Any modifications to the signed code can then be detected during the secure boot process.
2. The public key is hashed and programmed into the CPU during device provisioning. This provides a basis to verify digital signatures of the external secure boot code (ESBC).

Pre-Boot Phase:

3. After reset, all device activity is blocked. Fuse values are sensed by the security fuse processor (SFP) which locks down interfaces and memory and enforces security policy before boot. The pre-boot loader (PBL) then loads a reset configuration word from external non-volatile memory to begin system configuration.

Internal Secure Boot Code (ISBC) Phase:

4. The CPU is allowed to boot and

Silicon AT Features	Type	Category
Volatile AES-256 BBRAM Key Storage	Passive	Prevention
Non-volatile AES-256 eFUSE Key Storage	Passive	Prevention
256-bit AES Bitstream Decryption	Passive	Prevention
HMAC SHA-256 Bitstream Authentication	Passive	Prevention
Hardened Readback Disabling Circuitry	Passive	Prevention
Robust Key Load Finite State Machine (FSM) Circuitry	Passive	Prevention
JTAG Disable	Active	Prevention
JTAG Monitor	Active	Detection
Internal Configuration Memory Integrity	Active	Detection
On-chip Temperature and Voltage Monitor/ Alarms	Active	Detection
Program Intercept	Active	Detection
Unique Identifiers (Device DNA and User eFUSE)	Active	Detection
Internal Configuration Memory Clear	Active	Response
Internal AES-256 BBRAM Key Erase	Active	Response
Global 3-State	Active	Response
Global Set-Reset	Active	Response

Table 1 Xilinx Artix AT Features

begins executing internal boot code from a hardwired location within the internal boot ROM. The ISBC is inherently trusted. It confirms the binding of the public key to the device, validates the digital signature of the ESBC, validates the ESBC image, and confirms that the first instruction falls within the validated range and executes.

External Secure Boot Code (ESBC) Phase:

5. The ESBC can be a monolithic image, or multi-stage boot images, which validates the digital signature and image of the operating system or application, thereby extending the chain of trust.

COTS Secure FPGA Technology

The FPGA security hub receives input from tamper detection sensors throughout the system and has the ability to interface with the processor; erase data, configuration and key storage; and disable interfaces to provide an appropriate tamper response. The FPGA can use either a standard COTS or a Commissioned configuration to define its response behavior. The FPGA configuration is encrypted with various safeguards to protect content. Both Xilinx Artix and Lattice MACHXO2 devices are used to serve as security hubs.

Xilinx

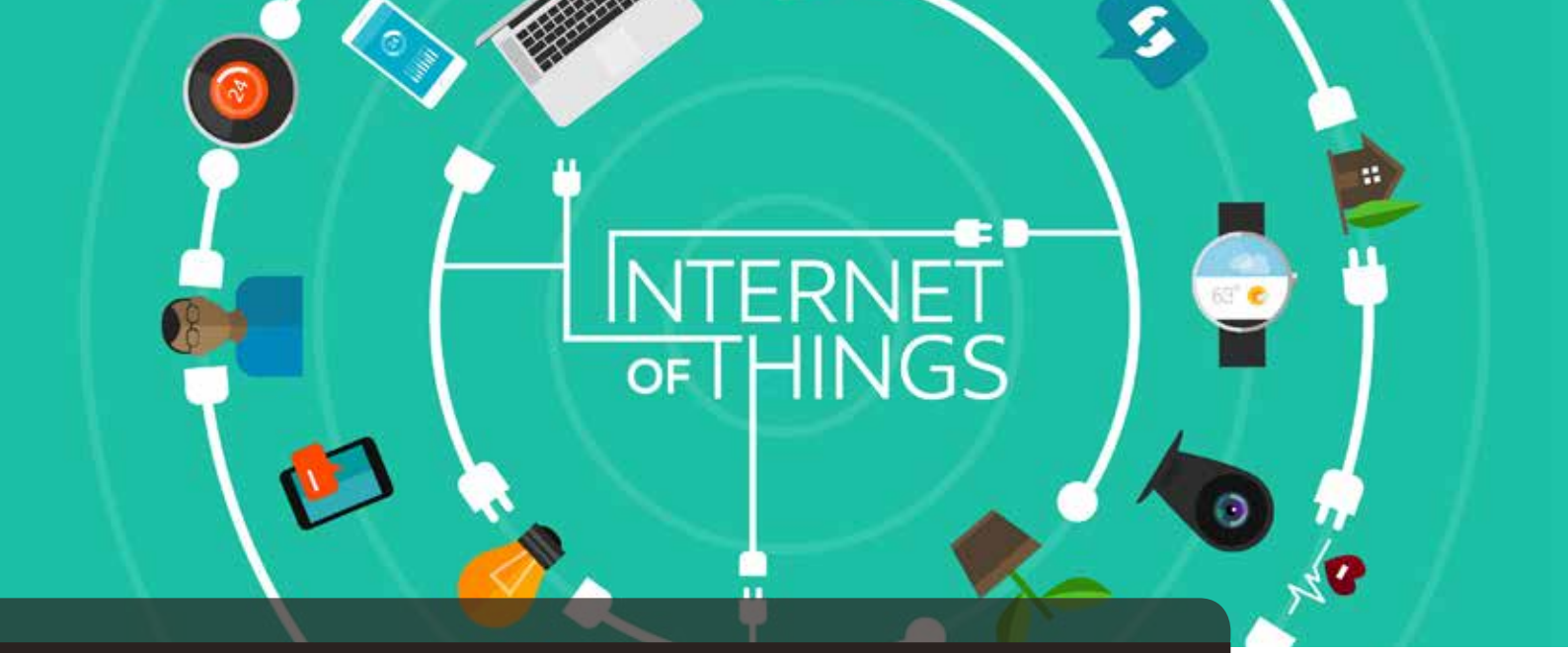
Xilinx Artix FPGAs provide various AT features. Passive features are built-in to the silicon - COTS features - and do not require design development, while active features can be incorporated as needed as part of the Commissioned FPGA design effort. available AT features.

Lattice

Lattice MACHXO2 FPGAs incorporate on-chip embedded flash memory to eliminate configuration bit-stream vulnerability. Device security bits prevent read-back of the configuration from the device, and a one-time-programmable mode prevents erasure or reprogramming of the configuration.

Conclusion

Anti-tamper plays a vital role in the overall information assurance scheme for embedded systems. A successful AT campaign provides layered safeguards for prevention, detection, and response. A carefully considered COTS/Commissioned combination leverages lower-cost, reliable COTS elements while allowing customers to incorporate sensitive or restricted technologies, policies, and procedures. Abaco uses its partner relationships and engagements to provide synergy between the hardware, middleware, stacks, partitioned operating system, and hypervisors. The use of Intel's Trusted Execution Technology and Freescale's Trust Architecture provides industry-standard trust mechanisms, while a Xilinx- or Lattice-based FPGA security hub augments a robust tamper response. Hardware build options are available to provide the flexibility to meet customer requirements



ARIS Board

Arrow

Arrow Electronics has announced the introduction of the ARIS Board, a ready-to-use Internet of Things (IoT) hardware and software solution. ARIS is the acronym for Arrow Renesas IoT Synergy, therefore showing the close cooperation between Arrow Electronics and Renesas and their Renesas Synergy™ development platform. The newly announced IoT Board is to enable users to develop their applications quickly and easily, in order to bring them to market in the shortest time possible. The ARIS Board was developed by the Italian company RELOC which focuses on embedded designs and the vertical integration of IoT applications. In addition to the development and production of the Board, RELOC also dealt with the implementation of the drivers and the generation of the middleware for managing the peripheral devices and has thus established an out-of-the-box IoT development environment.

On the basis of the Renesas Synergy™ development platform, it helps to speed up the generation of IoT designs by offering a faster and easier launch into the development process with a fully qualified and optimum hardware and software solution that boosts innovation and product differentiation.

The system is built around a Renesas S7G2 high-performance MCU, as is shown in Fig. 1. The microcontroller unit consists of a 240 MHz ARM Cortex-M4 embedded processor with a 4 MB flash memory and a 640 KB SRAM. Furthermore it is provided with a 512 MB serial flash, a 256 MB SDRAM memory, and an additional microSD card slot. The three-axis acceleration sensor and the two-axis gyroscope supply information with regard to the position and movement of the Board. These sensors can be activated via an SPI connection. Further sensors mounted on the Arrow ARIS Board are a thermal sensor and a humidity sensor that can be activated via the I²C interface to supply further ambient data. In order to optimally process the data collected by the sensors, a strong focus was directed on the communication and connectivity of the device. This has enabled the ARIS Board to now also communicate with its environment in a wireless fashion via Wi-Fi, Bluetooth Low Energy (BLE 4.1/4.2), and NFC, in addition to its means of communication via Ethernet 10/100 or a USB connection. In order to also make it possible for the user to interact with the Board, various user interfaces have been implemented. Via the GPIO interface, LEDs, pushbuttons, and a TFT screen can be accessed. Furthermore a resistive touchscreen is supported via I²C. In order to make the Board an all-purpose tool, it was designed in Arduino layout which also enables the use of extension shields, thus making it possible to implement any conceivable application. Additional functions such as the on-board J-Link debugger, support for crypto bootloaders, and over-the-air (OTA) firmware updates make the development process easier, quicker, and more reliable.

The combination of the Arrow ARIS Board and the Renesas Synergy™

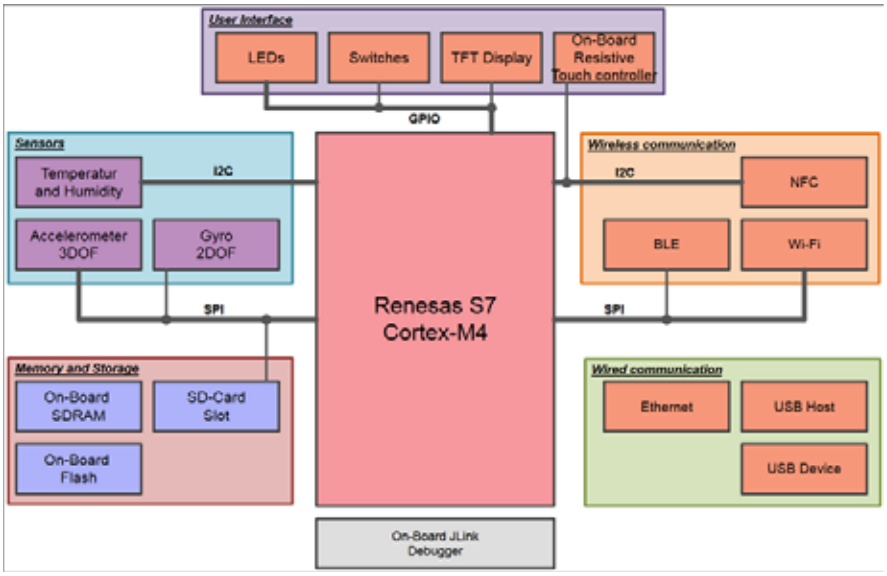


Fig. 1 – Block diagram of the ARIS Board

software development environment makes it possible for the developer to significantly reduce the time-to-market. This also ensures a significant reduction in the total operating costs throughout the entire service life of the product.

What makes the Renesas Synergy™ platform so unique?

In contrast to other development environments, all elements of the Renesas Synergy™ platform have been freshly developed from scratch and specially tailored to match embedded design applications. This provides for unprecedented scalability and compatibility, resulting in maximum re-usability of user codes and thus saving a great deal of development time. In future, the platform will be extended; new technologies will be employed, and new features will be permanently implemented, in order to launch embedded design applications more quickly and efficiently on the market. The integrated developed environment (IDE) implemented in this platform is Renesas Eclipse Embedded Studio, known as e² Studio. On the basis of Open Source IDE Eclipse, this solution offers a high level of flexibility and creativity. You can download and install the complete Renesas Synergy™ platform free of charge from the Renesas Synergy Gallery. In addition to the software required, this site also provides application samples that can be easily adapted to the ARIS Board.

A three-part hands-on training course provides for a perfect start on the development of individual solutions with the Arrow ARIS Board and the Renesas Synergy™ platform. In next to no time, the users learn to utilize all tools required for developing individual applications in the field of embedded and IoT systems. In the first instance it is explained and shown how the development environment is used. In a step-by-step programme, the training course includes the creation of a new project, the selection of the correct Board Support Package (BSP), and the implementation both of the modules required and of the user code. The BSPs provided are specifically tailored to boards that are supported on the Renesas Synergy™ platform. The use of this service makes complex programming in register entries and pin configurations dispensable. Symbolic links that are already predefined are used instead, making the generation of the user code considerably easier. The hands-on training programme includes examples that are implemented by means of a BSP specially designed for the Arrow ARIS Board, thus demonstrating the easy and fast utilization of ARIS. In addition to the use of the GPIO pin for controlling the on-board LEDs it is furthermore shown how USB communication can be established and how the Arrow ARIS Board can be established as a Wi-Fi access point.

Together with Renesas Electronics and their Synergy™ platform, Arrow Electronics therefore offers a perfect solution for exploring and mastering the world of IoT.

System Validation at ARM: Enabling our Partners to Build Better Systems

› Eoin McCann, ARM Processors

Functional validation is widely acknowledged as one of the primary bottlenecks in System-on-Chip (SoC) design. A significant portion of the engineering effort spent on productizing the SoC goes into validation. According to the Wilson Research Group, verification consumed more than 57% of a typical SoC project in 2014.

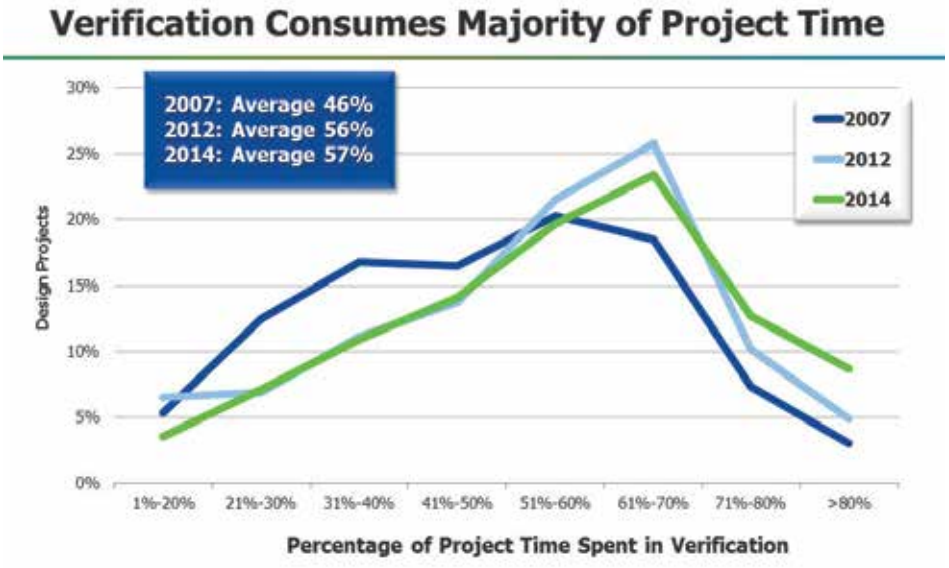
In spite of these efforts, functional failures are still a prevalent risk for first-time designs. Since the advent of multi-processor chips, including heterogeneous designs, the complexity of SoCs has increased considerably. As you can see in the diagram below, the number of IP components in a SoC is growing at a strong rate.

SoCs have evolved into complex entities that integrate several diverse units of intellectual property (IP). A modern SoC may include several components such as CPUs, GPU, interconnect, memory controller, System MMU, interrupt controller etc. The IPs themselves are complex units of design that are verified individually. Yet, despite rigorous IP-level verification, it is not possible to detect all bugs - especially those that are sensitized only when the IPs interact within a system. This article intends to give you some behind-the-scenes insight into the system validation work done at ARM to enable a wide range of applications for our IP.

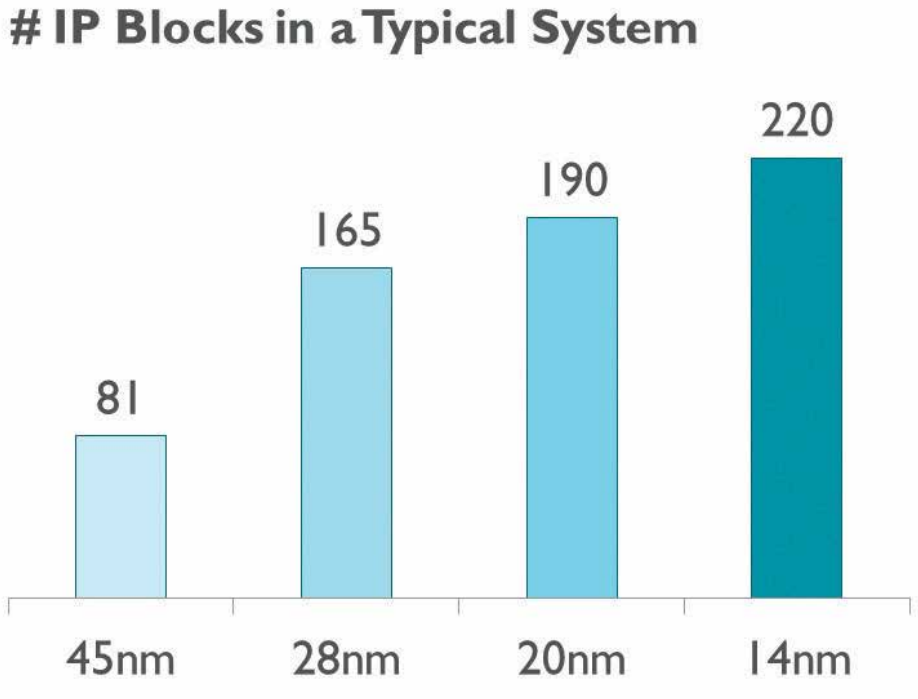
Many SoC design teams attempt to solve the verification problem individually using a mix of homegrown and commercially available tools and methods. The goal of system validation at ARM is to provide partners with high quality IP that have been verified to interoperate correctly. This provides a standardized foundation upon which partners are able to build their own system validation SOC solutions. Starting from a strong position, their design and verification efforts can be directed more at the design differentiation they add to the SoC and its interactions with the rest of the system.

Verification Flow

The verification flow at ARM is similar to what is widely practiced in the industry. Verification of designs starts early and at the granularity of units, which combine to form a stand-alone IP. During the entire verification cycle it is at unit-level when engineers have the greatest amount of visibility into the design. Individual signals that would otherwise be deep within the design may be probed or set to desired values to aid validation. Once unit-level verification has reached a degree of maturity, the units are combined to form a complete IP (e.g. a CPU). Only then can IP-level verification of the IP commence. For CPUs this is very often the first time assembly program level testing can begin. Most of the testing until this point is by toggling individual



Source: Wilson Research Group



Source: ChipDesignMag

wires/signals. At IP level the tests are written in assembly language. The processor fetches instructions from memory (simulated), decodes them executes etc. Once top-level verification reaches some stability multiple IPs are combined into a system and the system validation effort begins.

IPs go through multiple milestones during their design-verification cycle that reflect their functional completeness and correctness. Of these, Alpha and Beta milestones are internal quality milestones. LAC (Limited Access) represents the milestone after which lead partners get access to the IP. This is followed by EAC (Early Access), which represents the point after which the IP is ready to be fabricated for obtaining engineering samples and testing. By the REL (Release) milestone the IP has gone through rigorous testing and is ready for mass production.

IPs are usually between Alpha and Beta quality before going through the system validation flow. By this phase of the design cycle the IPs have already been subjected to a significant amount of testing and most low-level bugs have already been found. Stimulus has to be carefully crafted so that the internal state of the micro-architecture of each IP is stressed to the utmost. The stimulus is provided by either assembly code or by using specially designed verification IPs integrated into the system. ARM uses a combination of both methods.

Many of these bugs could result in severe malfunctions in the end product if they were left undetected. Based on past experience ARM estimates these types of bugs to take between 1-2 peta cycles of verification to discover and 4-7 man months of debug effort. In many cases, a delay that large would prove fatal to a chip's opportunity to hit its target window in the market. Catching them early enough in the design cycle is critical to ensure the foundations in the IP are stable, before they go on to being integrated as part of an SoC.

System Validation

The nature of ARM's IP means it is used in a diverse range of SoCs, from

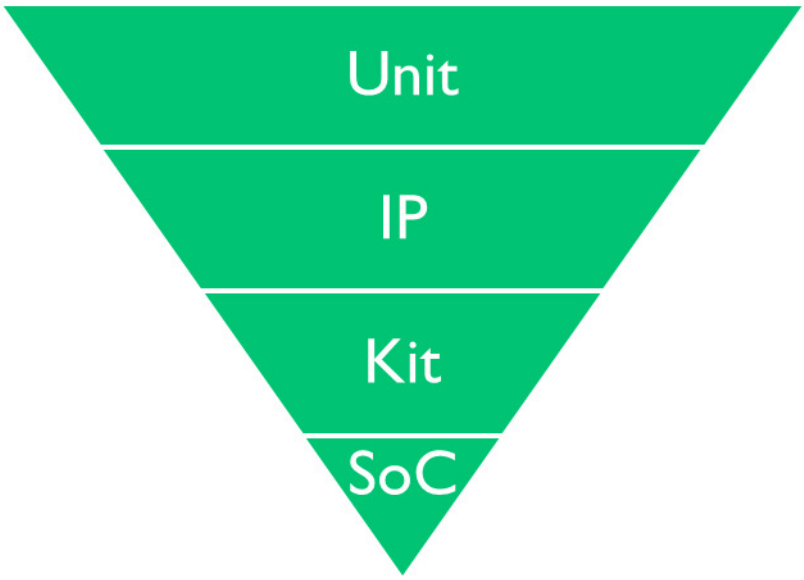


Diagram 3. The ARM verification flow pyramid

IoT devices to high end smartphones to enterprise class products. Ensuring that the technology does exactly what it is designed to do in a consistent and reproducible manner is the key goal of system validation, and the IP is robustly verified with that in mind. In other words, Focus of verification is IP but in a realistic system context. Towards this end, ARM tests IPs in a wide variety of realistic system configurations that are called Kits.

A kit is defined as a "group of IPs" integrated together in the form of a subsystem for a specific target application segment (e.g. Mobile, IoT, Networking etc.). It typically includes the complete range of IPs developed within ARM - CPUs, interconnect, memory controller, system controller, interrupt controller, debug logic, GPU and media processing components.

A kit is further broken down in to smaller components, called Elements. Elements can be considered building blocks for kits. It contains at least one major IP and white space logic around it, though some of the elements have several IP integrated in together.

These are designed to be representative of typical SoCs with different applications. One result is that it gives ARM a more complete picture of the challenges faced by the ecosystem of integrating various IP components together to achieve a target system performance.

The system validation team uses a combination of stimulus and test methodology to stress test kits. Stimulus is primarily software tests that are run on the CPUs in the system. The tests may be hand-created - either assembly or high-level language - or generated using Random Instruction Sequence - RIS tools, which will be explained in the upcoming sections. In addition to code running on CPUs, a set of Verification IPs (VIPs) are used to inject traffic into the system and to act as observers.

In preparation for validation, a test plan is created for every IP in the kit. Test planning captures various IP configurations, features to be verified, scenarios that will be covered, stimulus, interoperability consideration with IPs, verification metrics, tracking mechanisms , and various flows that will be a part of verification. Testing of kits starts with simple stimulus that is gradually ramped up to more complex stress cases and scenarios.

The testing performs various subsystem level assessments such as performance verification, functional verification, and power estimation. Reports documenting reference data, namely the performance, power, and functional quality, of selected kits are published internally. This document focuses on functional aspects only and more on Performance and Power related topics will be covered in future blogs.

The system validation team at ARM has established a repeatable and automated kit development flow, which allows us to build multiple kits for different segments. ARM currently builds and validates about 25 kits annually.

The mix of IPs, their internal configuration, and the topology of the system are chosen to reflect the wide range of end uses. The kits are tested on two primary platforms – emulation and FPGA. Typically testing starts on the emulator and subsequently soak testing is done on FPGA. On average every IP is subjected to 5-6 trillion emulator cycles and 2-3 peta FPGA cycles of system validation. In order to run this level of testing, ARM has developed some internal tools .

System Validation Tools

There are three primary tools used in System validation, which are focused on areas like Instruction pipeline, Ip level and system level memory system, system coherency, Interface level interoperability, etc. Two of these tools are Random Instruction Sequence (RIS) generators. RIS tools explore the architecture and micro-architecture design space in an automated fashion, attempting to trigger failures in the design. They are more effective at covering the space than hand written directed tests. These code generators generate tests to explore different areas of architecture and micro-architecture in an automated fashion. The tests

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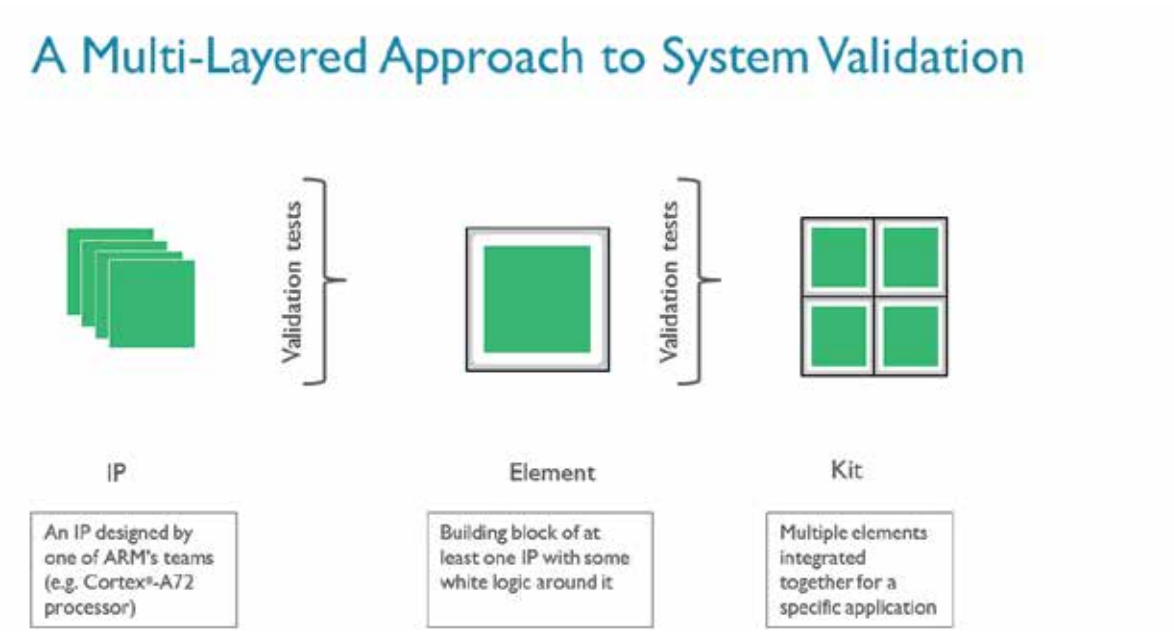


Figure 4. Experimental setup.

are multi-threaded assembly code, comprised of random ARM and Thumb instructions, designed to thoroughly exercise the functioning of different portions of the implementation.

The third tool is a lightweight kernel that can be used as a platform to develop directed tests. The validation methodology uses a combination of directed testing and random instruction based automated testing. It supports basic memory management, thread scheduling, and a subset of the pthreads API, which allows users to develop parameterized directed tests.

Methodology

In order to stress test IP at the system level a more random approach is used rather than a directed approach. This enables ARM to cover a range of scenarios, stimulate multiple timing conditions and create complex events. To this end, Kits support various verification-friendly features like changing the clock ratios at different interfaces, enabling error injectors, stubbing out components that are not required for a given feature verification etc. Bus clock ratios at various interfaces in the system like CPU, interconnect and dynamic memory controller can be changed to stimulate realistic system clocking conditions.

Diagram 5 shows how the system is initially brought up and how test complexity is gradually scaled up.

Integration Tests & KVS

Initial testing starts with a set of simple integration tests are run to confirm basic stability of the kit and flush out minor integration issues. Following which a suite of tests called Kit Validation Suite (KVS) is used to thoroughly test the integration of the kit. These tests are run early in the verification cycle to validate the Kit is good enough to run more stressful payloads. KVS can be configured to run on a wide variety of kits. It includes sub-suites to test integration, power, CoreSight debug and trace, and media IPs. There are specific tests in KVS to test integration of GPU and display as well as GPU coherence. Initial boot is usually done on simulation and gradually transition to emulators (hardware accelerators) for the integration testing.

RIS Boot and Bring up

After that we boot all the RIS tools with basic bring up tests on the kit to work through any hardware/software configuration issues.

RIS: Default and Focused Configurations

Once the kit is stable the complexity of tests and therefore the stress that they place on the system is increased. Random stimulus can cover the design space faster than directed stimulus and requires less effort towards stimulus creation. Therefore, for stress testing there is more reliance on random stimulus than directed tests. Initially default configurations of the RIS tools are run and after a suitable number of verification cycles, the tools are re-configured to stress the specific IPs in the kit.

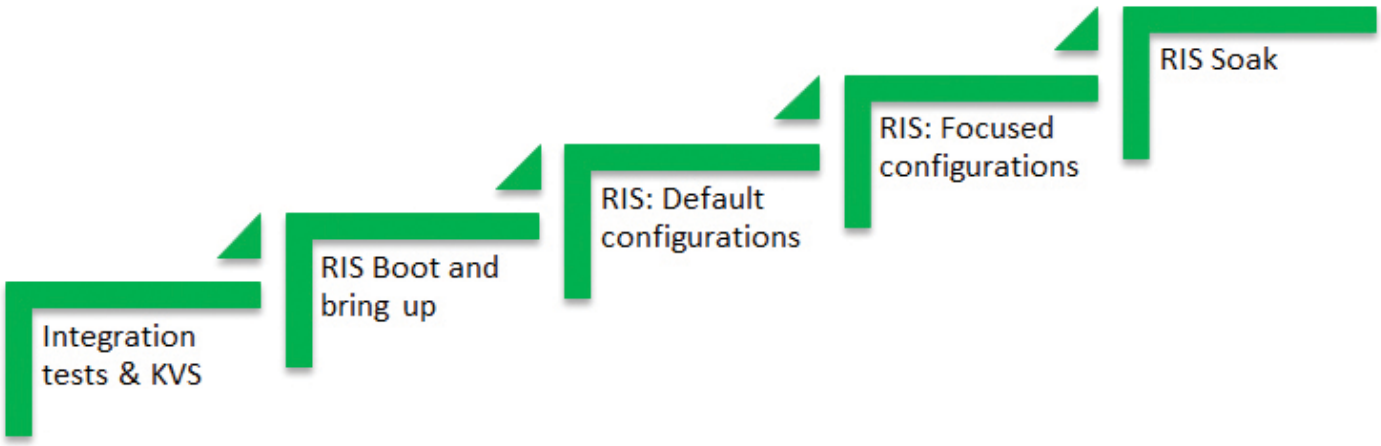


Diagram 5. System validation bring up

RIS Soak

In the final phase of system validation the kit is soak tested on FPGAs. Though emulators are more debug friendly, FPGAs are faster and can provide a lot more validation cycles. Therefore, once the IPs are stable and mature, ARM does soak test on FPGAs to find complex corner cases.

Metrics, Tracking, Coverage and Milestone Closure

The number of validation cycles run for every Kit is one of the metrics that is tracked to ensure the target number of validation cycles have been met. This is especially useful to ensure the soak-testing cycle target has been met, increasing the confidence of the quality of the IP in various applications. In addition to that we quantify and track coverage using a statistical coverage method to ensure the full design including potential corner cases have been exercised sufficiently.

The latest version of the ARM Juno test chip was subjected to a total validation run time of 6,130 hours, the equivalent of 8 and a half months of testing. This gives a unique perspective into corner cases within the system that makes ARM better able to support partners who are attempting to debug issues within their own design. Furthermore, the bugs that are found during the validation process are then fed back into the IP design teams who use the information to improve the quality of the IP at each release milestone, as well as guide next-generation products.

Summary

System complexity has increased in line with SoC performance capabilities, causing a significant growth in the amount of time and money spent on validation. ARM verifies its IP for interoperability before it is released to partners to make sure it is suitable for a wide range of applications. ARM's IP teams are continuously designing at the leading edge, and are helped by the system validation team to ensure they work together in the systems our partners are building.

Frank Schirrmeister of Cadence Design Systems cites the validation of their tool interoperability as one benefit. "As an ARM ecosystem partner, Cadence relies on pre-verified ARM cores and subsystems that can be easily integrated into the designs that we use to validate our tool interoperability. ARM's software-driven verification approach reflects the industry's shift toward the portable stimulus specification and allows us to validate the integration and interoperability of ARM cores and subsystems on all Cadence System Development Suite engines, including simulation, emulation and FPGA-based prototyping engines."

Due to the wide variety of applications that the ARM partnership designs for, it is necessary to ensure our IP is functional in many different systems. The multi-stage approach to system validation at ARM gives our partners the peace of mind that they can rely on our IP. Over time the validation methodology has evolved into one that tests several system components and stresses most IPs in the system. In the future we have plans to extend and further improve our test methods to ensure an even higher standard of excellence across ARM IP.

(Huge thanks to the system validation team in Bangalore for providing me with all of the technical information here. Much appreciated!)

Manage the IoT on an Energy Budget part 2

› Silicon Labs

Do even more while sleeping

The thermistor example shows one method of operating an external sensor in a very energy efficient way, assuming that the MCU has the hardware to support it.

There are also other ways of solving the thermistor problem. On the EFM32 Gemstone products, as well as the Blue Gecko, based on EFM32 Gecko technology, the ADC can now operate while the system is in deep sleep mode (EM2). The "improved" approach above, where the RTC/RTCC woke up the CPU to take an ADC sample, can now be changed to making the RTCC automatically trigger the ADC through the peripheral reflex system (PRS). An ADC with these products also has the ability to evaluate the ADC result and only give the CPU an interrupt if the sample is outside or inside given thresholds.

It is important to also duty-cycle the thermistor properly. Where LESENSE does this for you automatically, the ADC does not, and it has to be controlled either via PRS or from the CPU. It makes sense to turn the thermistor on in sufficient time before sampling, and off immediately after. Let us see what happens if we try to use an RTCC event through PRS to enable and disable the thermistor. This scenario is shown in Figure 5.

As the figure shows, an RTCC event is longer than the ADC takes to warm up and sample the thermistor. Based on a 32 kHz clock, the RTCC event keeps the thermistor on for 22 µs longer than necessary. You can cut this time down by using some PRS tricks. For example, the ADC produces a short PRS output whenever it is done. Using the RTC event, PRS signal, and the ADC to complete the PRS pulse, it's possible to create a signal that goes high on the RTC trigger and low when the ADC is complete. This signal can automatically enable the thermistor in the system.

The conceptual circuit for this example is shown in Figure 6. Initially, the latch output Q is low because the RTCC event output and the ADC conversion done output are low. Whenever the RTCC event now goes high, the external sensor is enabled and the ADC starts taking a sample. Once the ADC is done, the conversion done signal goes high, setting the latch output Q high, which forces the external sensor off. When the RTCC event signal goes low again, the latch is reset, making the system ready for the next event.

The circuit shown in Figure 6 can easily be implemented on an EFM32

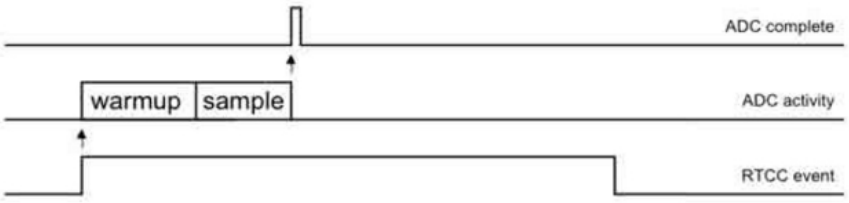


Figure 5 - ADC sample triggered by RTCC event through PRS.

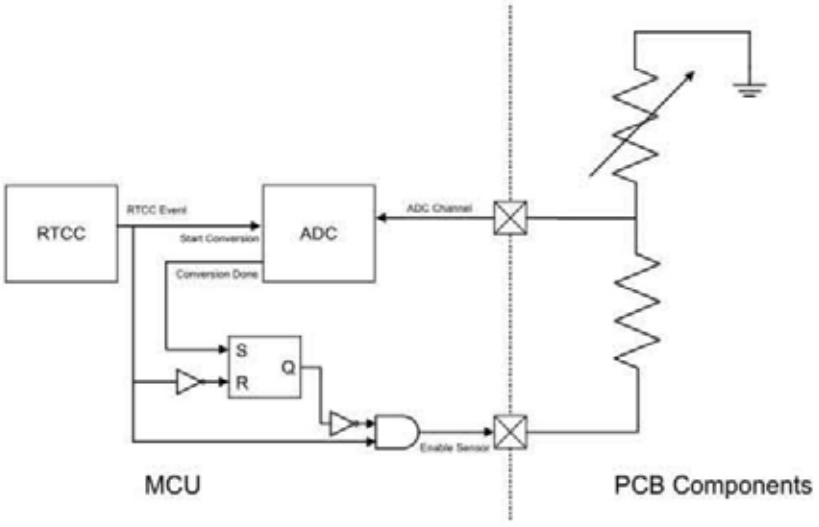


Figure 6 - Conceptual circuit, which starts external sensor excitation on RTCC trigger, and ends excitation when ADC sample has been taken.

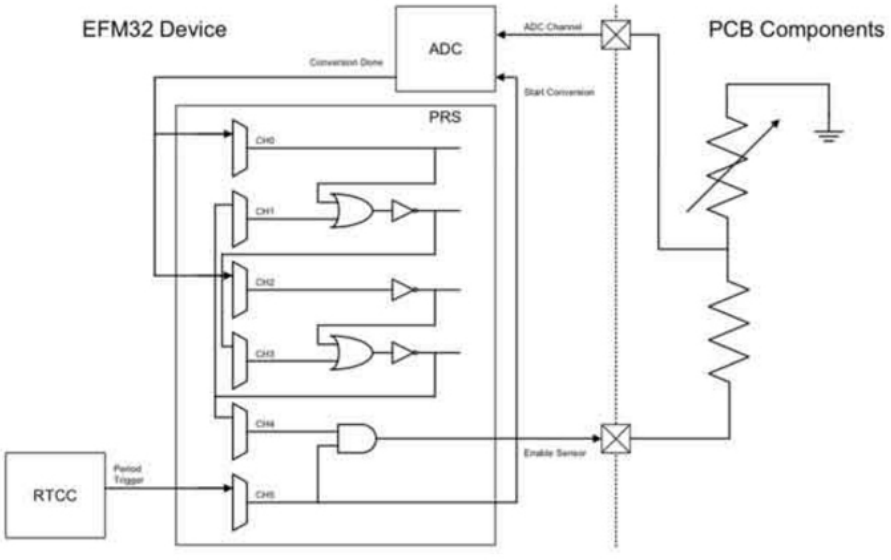


Figure 7 - PRS implementation of circuit performing optimal excitation of external sensor.

Gemstone MCU using the Peripheral Reflex System (PRS), which contains logic elements that can be connected together in various ways. Figure 7 shows what this implementation would look like using six of the available PRS channels. Table 4 shows how the 6 PRS channels are configured to enable this functionality.

Using the ADC autonomously running in EM2, with PRS for optimal excitation of the thermistor, as we have shown here, shows a fourth way of implementing monitoring of an external sensor. To monitor it autonomously, the ADC was set to test whether the thermistor value was within a certain window, and only notify the CPU if the value happened to be outside.

The results are on par with the results using LESENSE in the previous section, but compared to LESENSE, which uses a comparator for detection, this example employs a full 12-bit ADC, and thus higher monitoring accuracy. Current consumption results are shown below, and Figure 8 shows the 128 Hz scenario in detail.

a. Pearl Gecko, sampling ADC in EM2 @ 1 Hz: 2.22 µA
b. Pearl Gecko, sampling ADC in EM2 @ 16 Hz: 2.30 µA
c. Pearl Gecko, sampling ADC in EM2 @ 128 Hz: 2.75 µA
d. Pearl Gecko, sampling ADC in EM2 @ 1024 Hz: 6.51 µA

What we have built here is an autonomous system customized to do a specific task in hardware, allowing the CPU to sleep as much as possible. The above is simply an example, and many other configurations are possible. Low power applications like this are enabled on the EFM32

PRS CH	INPUT	AND	OR	INV	RESULTING OUTPUT
0	ADC				ADC conversion done
1	PRS_CH3		PRS_CH0	Y	!(CH0 || CH1)
2	ADC			Y	!ADC conversion done
3	PRS_CH1		PRS_CH2	Y	!(CH2 || CH3)
4	PRS_CH3	PRS_CH5			CH4 && CH5 Enable sensor
5	RTCC				RTCC event Start conversion

Table 4 - PRS configuration to implement circuit performing optimal excitation of external sensor.

Figure 8 - Pearl Gecko, EM2 autonomous, sampling ADC @ 128 Hz.

platform because of a wide range of low energy mode functionality in the MCU itself:

- Analog functions (ADC, DAC, ACMP, and IDAC) operate down to EM3
- Most communication interfaces have modes allowing them to operate down to EM2/EM3
- Low power timers have broad amounts of functionality: LETIMER, RTC, and RTCC
- Specialty hardware (e.g. PCNT and LESENSE) allows complex operations that would normally require the CPU

As an example, the pulse counter (PCNT) can monitor higher frequency processes all the way down to EM3:

- Monitor absolute rotation or translation through an integrated quadrature decoder:
  - Wake up or notify the PRS on a direction change, absolute rotation, or absolute position
- Monitor signal frequencies:
  - Wake up or notify the PRS on a frequency change
- Monitor event counts
  - Number of ADC samples taken, PWM pulses generated, etc., through PRS
  - Number of excitations from external sensor or other device through IO

Optimizing the system

The discussion so far has considered a system dealing with a single function and a single source of wakeups. Imagine a system with ten different components that need to be managed. Some can be controlled fully autonomously, like the thermistor above. For others, the CPU might have to wake up periodically in order to take control.

If care is not taken with such a system, it can end up in a situation like the one shown in case A of Figure 9, with many more wakeups than necessary, resulting in a less efficient system. The figure shows two deterministic processes, which execute periodically, and one sensor event, firing nondeterministically. In case A, the processes arbitrarily wake up to perform their tasks, which results

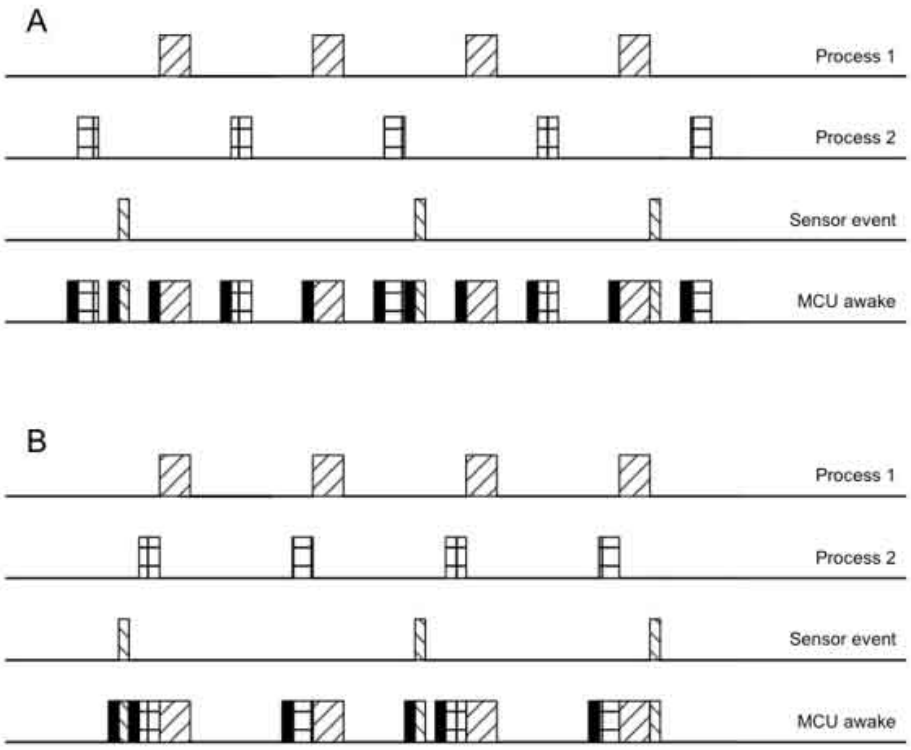


Figure 9 - Sleep Planning. The black segments show time wasted due to wake-up time from deep sleep modes.

in a total of 11 wakeups, wasting a significant amount of energy due to the time it takes to transition between sleep modes.

To improve on case A, you can do sleep planning. For all deterministic processes, i.e. processes we know of beforehand that are going to require a wakeup, care should be taken to align the wakeups as much as the system allows, minimizing the number of wakeups.

In case B, the wakeups by Process 2 have been aligned with the wakeups from Process 1, resulting in a total of 6 wakeups during the same period, a significant reduction from case A.

Sleep Planning

As we have discussed, minimizing awake time is important. In many cases, software running on the CPU is waiting for something to happen. If the CPU is set to wait for a fixed time, the best approach is to use a hardware timer. Hardware timers come in a range of types with varying functionality, current consumption, and accuracy.

On an EFM32 system, if the CPU needs to sleep for a short number of clock cycles while maintaining full MCU operation, the software should use the TIMER peripheral and place the system in EM1 while waiting. This method will significantly reduce current consumption, and wakeup is instantaneous.

If only EM2-EM4 level functionality is necessary while waiting and the wait-time is more than 31 µs, the period of a 32768 Hz oscillator, the low-frequency timers LETIMER, RTC, or RTCC can be used and the system can go to EM2 for maximum efficiency. If high accuracy is required, a TIMER can be synchronized to the low-frequency timer upon wakeup through PRS to time out the last clock cycles with the accurate high-frequency TIMER.

If wait time is relatively long, i.e. multiple milliseconds, and does not have to be accurate, and the system only needs EM4 functionality while sleeping, sleep can be done using the CRYOTIMER, running on the 1 kHz ULFRCO oscillator for extremely low sleep current in the 100 nA range. Note that wakeup from EM4 costs more energy than wakeup from EM2, because the wakeup is through a reset, so even though EM4 could be used for sleeping for 5 ms, it might not be the most energy efficient. With sleep times of minutes or more, EM4 starts becoming extremely efficient.

Note that on EFM32 devices, a write to the low-frequency timers (LETIMER, RTC, or RTCC) is instantaneous, compared to other MCUs, where a write takes multiple low-frequency cycles. This means that on EFM32, if the RTC value is currently 99, the MCU can decide to go to sleep and wake up on value 100. For most other systems, the earliest RTC value possible to wake up on would be 102, making it difficult to sleep if the wait period is less than 100 µs.

CPU efficiency

No matter how much you try to optimize for sleep, the CPU needs to execute code now and then. This can include everything from regular application logic to network stacks and signal processing algorithms. The CPU is an important part of the MCU. Here are the top five items to ensure

CPU	MOST EFFICIENT ON
Cortex M4	Large applications and/or applications with signal processing
Cortex M3	Large applications with mixed requirements
Cortex M0+	Smaller applications, stacks, control logic

Table 5 - Simplified overview of ARM Cortex M CPUs

the CPU runs code efficiently:

1. Let the compiler optimize your code.

This tip might seem obvious, but make sure the code is compiled with full optimizations enabled. If the compiler is able to do link-time optimization, use this as well. Code compiled for debugging is inefficient on many compilers, one reason being that values are fetched from memory, calculated and then written back on every operation. Without optimization, it is also not fully utilizing the capabilities of the CPU, which also slows down execution.

2. Target the right architecture.

Choose the right CPU for your application and ensure that the compiler creates code optimized for that correct device. For example, Cortex M4 is excellent for bigger applications that contain number crunching. Cortex M3 does not have all the DSP capabilities and no floating point, compared to the Cortex M4, but is still relatively high performance. Cortex M0+ is the most efficient of the bunch as long as the amount of signal processing is at a minimum. It is excellent for stacks and control logic.

3. Operate at the right frequency.

Even though lower frequencies give lower current consumptions, it is generally better to finish the job quickly to be able to go to sleep; in other words, a higher frequency might give better energy efficiency. If the different parts of the system require different needs (i.e. USART needs 4 MHz, but the CPU needs 8 MHz), use pre-scalers for clock domains to make the frequency selection optimal.

4. Use available hardware accelerators.

Some operations perform more efficiently in hardware than on a CPU. One example is cryptography. The CRYPTO peripheral available on the EFM32 Gemstone devices can complete operations more than 10 times faster and much more efficiently than running them on the CPU. Another example is the alpha blending hardware on some of the EFM32 products. This hardware makes graphics compositing for external displays more efficient.

5. And, of course, sleep whenever possible.

Hardware efficiency

So far, we've focused on how the MCU is inherently efficient and can control the application in an efficient manner. The picture is almost complete. The remaining details must center on how the hardware is built, as well as how energy is stored and supplied to the system.

While this topic is too broad to delve deeply into here, one important point is operating voltage. In general, the lower voltage supplied to a component, the more efficient the component is, down to the functional limit of the device. A lot of traditional components have operating voltages around 3 V, but we're seeing a shift toward components running at a nominal 1.8 V.

This improvement is great for energy efficiency; however, a lot of energy sources, including coin cell batteries and lithium polymer batteries, output much higher voltages than this. In order to regulate the voltage down to the target voltage of the system in the most efficient way possible, you should use an efficient switched-mode buck converter (DCDC).

Some of the EFM32 Gemstone devices include a built-in DC-DC converter, able to supply both the MCU and external components with a total of up to 200 mA. This allows you to build a highly energy-efficient system without adding external converters.

For example, a 3 V lithium coin cell battery would have a mean voltage output of around 2.8 V. Using an LDO to regulate down to 1.8 V results in efficiency of around 64 percent. However a switching DC buck converter could regulate the same 1.8 V supply with efficiency of over 80 percent, which would extend the battery life by more than 25 percent, perhaps turning a four-year battery life into five years. Note that there is

a small additional cost associated with using even an integrated switching converter, as it requires an external inductor and some capacitors to be added to the PCB. In most applications where low power is important, this is a small price to pay for a significant increase in energy efficiency.

Conclusion

At the heart of most embedded products lives a microcontroller with power sources that may be limited to small coin sized batteries. When focusing on using available power more efficiently, designers will be able to create energy-friendly products and applications that are smaller, have longer battery life and cost less. These applications can then also use alternative and limited energy sources, such as energy harvesting.

In order to achieve this, designers must know how to leverage all the low power capabilities of the MCU that is controlling the application. A product should include hardware that monitors, controls and operates autonomously. This allows the system to be in deep sleep modes for the majority of its lifetime. Attention must be paid to the overall power architecture of the system, while leveraging the MCU to manage as much of it as possible. Whenever software needs to intervene, it should be swift and efficient.

MCUs and RF SoCs from Silicon Labs provide a unique combination of energy efficiency and flexibility. They are built for autonomous operation in deep sleep modes and provide the needed energy efficient for sleepy systems. Highly efficient active modes allow you to use the CPU as well, while staying inside your application's power budget. Ultimately, this allows smaller batteries or energy harvesting components, giving you the right combination of form factor, cost, and device availability.

LG UNVEILS SPECIAL EDITION PORTABLE SPEAKER FEATURING ARTIST JONONE IN PARIS

LG Electronics (LG) today took the wraps off its new LG Portable Speaker art series by JonOne in Paris, France. Featuring the bright artwork of popular artist JonOne, LG's latest wireless audio product sounds as great as it looks.

JonOne has earned a reputation for originality, with his open-ended approach to style and artistic innovation earning him a following around the globe. Growing up in Harlem in New York City, he was influenced by the freedom of the street art and graffiti tags that covered the city. His upbringing in America influenced his later work, leading to a strong emphasis on creativity and innovation. JonOne enjoys a strong following worldwide, particularly in France where the government has recognized him with the country's most prestigious Ordre national de la Légion d'honneur for his artistic vision and achievements.

Offering the best of the art world alongside the crystal clear sound of LG audio technology, the LG Portable Speaker art series is perfect for customers interested in audio products that not only exhibit exceptional performance, but look great at the same time. The three designs that were selected to represent the collaboration were inspired by art, culture and city life. Reflecting the ideas and themes that shape his

art, the speakers bring listeners into the world of JonOne every time they press play.

All the devices in the LG Portable Speaker art series are equipped with features found only in LG's advanced wireless audio products. Users can easily connect and control the speakers with up to two devices simultaneously via multi-Bluetooth paring and can also use two paired speakers as left and right stereo channels via Dual Play. These features combine to ensure that LG Portable Speaker art series will appeal to those that value individuality in their music, art and life.

The LG Portable Speaker art series by JonOne was launched at La Place Hip Hop Cultural Center in Les Halles, a landmark in the local hip hop scene known as the proving ground for new talents in France. At the launch event, JonOne himself created some of his distinct art in front of attendees while guests were able to experience how LG's portable speakers align with the philosophy that underpins JonOne's art.

"I have worked closely with LG at every stage of the design process, and I believe that these speakers act as the perfect medium for my artwork," said JonOne. "Trumpeting the value of individuality and self-expression, LG's latest portable speakers will inspire consumers to embrace their passions and live with more artistic intensity in their daily lives."

"Art can take many forms, and LG seeks to smash barriers by helping consumers include trendsetting artistic design in their everyday lives," said Park Hyoung-sei, executive vice president of the LG Home Entertainment Company. "The speakers we developed in collaboration with JonOne will encourage fans to apply innovation, style and art to everything that they do."

The LG Portable Speaker art series will roll out in France and other European countries starting this month.

New NANO Li-Ion Battery Does not Catch Fire, Designed for Defense Missions

Many battery cells experience thermal runaway, a condition that results in damage from overheating. Kokam Company produced a new battery, composed of Nickel Manganese Cobalt (NMC), Lithium Titanate Oxide (LTO) and Lithium Iron Phosphate (LFP), to overcome this problem.

NANO battery technology is a new kind of lithium-ion battery that passed ballistic testing and was made to withstand temperatures between -40° and 60° Celsius. Batteries can experience thermal runaway from specific temperatures, but Kokam created a design that surpassed many factors.

Kokam promises a longer life expectancy, greater safety, less recharge time, greater power delivery, and the ability to withstand harsh temperatures for its new battery. The real-world applications are endless, making the battery a good choice for government defense measures.

The lithium-ion battery was specially constructed for defense and aerospace missions. Its silent nature makes it a safer substitute for diesel and other types of engines, all while being available for volatile operations. The energy it provides makes it useful for many other applications as well.

The Kokam company has provided many other batteries as well over the past 26 years. In fact, it is widely respected across the world as being an environmentally-friendly provider of energy efficient solutions. Kokam also offers the Ultra High Power Nickel Manganese Cobalt (NMC) and Ultra High Energy NMC battery solutions for other types of government applications.

The Ultra High Power NMC battery solutions are applicable to high-tech weapons and military operations that garner a lot of power, while the Ultra High Energy NMC battery solutions are better suited for unmanned aerial vehicles, drones, and similar applications.

The cost productive NANO battery technology will hopefully open up other paths to safer battery alternatives in the near future. Especially with the rise of government-directed drone use, society might benefit from Kokam's future chemistry applications.

World's First Ever Solar Plant Provides Power Day and Night

Crescent Dunes Project, located in Nevada, goes down in history as the first ever solar power plant, which provides clean electricity 24 hours a day.

Renewable energy is slowly getting closer to the place on the energy market that it deserves. Technology improves, reliability and efficiency increase, and consequently investments get a boost too. Limitations that were very apparent before, are now being tackled, helping the sector to reach more and more often great milestones.

A problem that has been recognized for a long time is that of energy storage and reliability of the source. Renewable energy generation is difficult to predict (although advances have been made in too), while energy storage systems are still struggling to keep up with the demand.

This, however, does not seem to remain a problem for too long. In fact, the solar power industry might have just found a way to overcome it. Meet Crescent Dunes Project, the first ever solar power plant, which generates electricity day and night, regardless of whether the sun is shining.

Developed and run by SolarReserve, Nevada-based Crescent Dunes Project provides energy to 75,000 homes. The 110-megawatt plant uses concentrated solar technology with more than 10,000 continuously moving mirrors. The energy is concentrated onto a central tower, where molten salt is heated to over 1,000 degrees Fahrenheit.

The most crucial element of the system is the molten salt, which is used in two ways. First, it acts as an energy storage, or thermal battery. The heat is retained until needed to be used. At night, or when the sun is not shining, the salt is then used to create hot steam via a heat exchanger. This steam then powers a steam turbine, which produces electricity.

This system is different from the

conventional solar arrays, which convert incoming solar rays directly into electricity, but do not operate when the sun is not shining. The principle behind SolarReserve is more similar to that of fossil fuel plants, only minus the emissions. This makes it the world's first 24-7 solar power plant.

According to SolarReserve, the project has been a brilliant investment. The numbers are follows: the investment was $1 billion, the duration of the contract that SolarReserve has signed is 25 years for $135 per megawatt hour. Crescent Dunes generates approximately 110 megawatts of energy every 12 hours, which sums up to about 1 million megawatts per year. This adds to a gross return of assets of about 13.5%.

SolarReserve is developing two more concentrated solar projects that are about to hit a milestone. One is the Redstone Solar Thermal Power Project, under construction near Postmasburg, South Africa, where it will be the first such plant in the whole of Africa. The second project is Copiapo Solar Energy, in Chile, which will have both concentrated solar and conventional solar panels. Needless to say, it will be the first of this kind in South America.

Image (c) SolarReserve

Samsung and Intel Launch Tech Initiative to Develop Recommendations for a National Internet of Things Strategy

Intel and Samsung today announced the formation of the National IoT Strategy Dialogue, an initiative to convene like-minded industry partners and organizations to collaboratively develop strategic recommendations for U.S. policy makers on the Internet of Things (IoT). The initiative, to be managed by the Information Technology Industry Council (ITI), will convene ITI's member companies as well as other industry stakeholders.

The launch of the National IoT Strategy Dialogue coincides with the new Department of Commerce IoT proceeding and the pending bicameral and bipartisan Developing Innovation and Growing the Internet of Things (DIGIT) Act – which would establish a working group of federal agency leaders to provide recommendations to Congress on how to plan for and encourage the proliferation of the IoT in the U.S. – in consultation with industry. The launch of this new IoT initiative answers the call of a chorus of technology leaders seeking a forum to proactively coordinate and drive industry's role in this process and help policymakers enable the U.S. to fully realize the vast benefits of IoT for economic and societal good.

Leaders representing the two co-founding companies and ITI – Samsung's OH Kwon, Intel's Doug Davis and ITI's Dean Garfield – shared the stage this morning at The Washington Post to announce the new National IoT Strategy Dialogue.

Vice Chairman and CEO of Samsung Electronics Dr. Oh-Hyun Kwon, "We look forward to working with Intel, ITI and other stakeholders in Washington to find the collaborative path forward in bringing the transformative benefits and solutions of IoT to scale."

"Intel looks forward to collaborating and driving recommendations with fellow ITI members, industry stakeholders and federal policy makers to help enable US IoT leadership," stated Doug Davis, senior vice president of IoT at Intel. "The National IoT Strategy Dialogue is consistent with the goals of the pending DIGIT Act and as a co-founder Intel is pleased to help drive this important technology transformation in the US."

"ITI is very excited to host this critically important initiative," said ITI President and CEO Dean Garfield. "Samsung, Intel, and our member companies, representing the biggest global names in tech, have been at the forefront of the evolution of IoT. Together, we will harness the inventive spirit and capability of these innovative companies and organizations to chart a clear path forward on IoT for U.S. policy makers."

Among its focus areas, the National IoT Strategy Dialogue will act as a convener and lay the foundation for industry to develop strategic policy recommendations to drive U.S. IoT infrastructure investment; facilitate interoperability; foster security; promote voluntary, industry-led global consensus-based standards

and best practices; leverage public-private partnerships; and enable IoT innovation to flourish.

Samsung, Intel and a broad base of other ITI member companies have been actively engaged in driving a pro-innovation policy environment that would enable U.S. leadership in the global IoT future. Both Intel and ITI called for the formation of a National IoT Strategy when testifying before Congress last year. In addition, ITI's member companies, including Intel, Samsung, and other technology leaders, developed IoT principles for advocacy outreach with government officials.

Samsung Shows Dedication to IoT with $1.2 Billion Investment and R&D

World's largest manufacturer of consumer electronics pledges to work collaboratively with industry and government to bring IoT to scale and improve quality of life for people everywhere

Samsung Electronics Vice Chairman & CEO Dr. Oh-Hyun Kwon unveiled today Samsung's vision for 'Human-Centered IoT,' including a strategy to spend $1.2 billion over 4 years for U.S.-based Internet of Things (IoT) R&D and investments. This will be led by the Samsung Strategy and Innovation Center, Global Innovation Center and Samsung Research America, part of Samsung's U.S. footprint of more than 15,000 employees across the country.

Vice Chairman Kwon delivered this news in a speech as part of a Samsung-hosted forum in Washington, D.C. The event, entitled Internet of Things: Transforming the Future, brought together technology industry leaders with policymakers and influencers to discuss the many ways IoT can benefit society, and how to tackle the challenges that remain in bringing it to scale.

Vice Chairman Kwon called for his peers to "start talking and thinking differently about IoT," with a human-centered approach, embracing the life-changing possibilities of the technology and working together to bring these benefits to society at-large.

"I am excited to show how we are moving IoT to the center of our strategy and am delighted to announce that Samsung is planning to spend $1.2 Billion in U.S.-centered IoT investments and R&D over the next 4 years," said Vice Chairman Kwon.

"At Samsung, putting people at the center of everything we do is our highest value," said Kwon. "The same must be true for IoT if we want to realize its full transformative power. Today, IoT is changing individual lives – helping people to age in their own homes. But tomorrow, using IoT, we can give the same independence to millions of Americans. We can keep people out of hospitals and nursing homes. As our populations live longer, these benefits and cost savings for society cannot be ignored."

In his keynote Vice Chairman Kwon offered industry and policymakers two principles in addition to a 'human-centered' approach: to be open and collaborative.

"If we want innovators everywhere to make use of IoT, we must make sure all tools are open to them. This means technologies that connect to each other, because we know that boundaries around technologies hold back innovation and scale," the Vice Chairman said.

He also warned that sector-specific regulations would inherently fragment the development of IoT, impeding devices and platforms from connecting to each other.

As the IoT ecosystem is by nature connected and interwoven, collaboration is vital to promoting this level of openness and interconnection. In this vein, Vice Chairman Kwon urged attendees to pursue cross-sector dialogue and partnerships, and announced Samsung's role as a co-founder of the newly launched National IoT Strategy Dialogue.

The Dialogue, to be hosted by the Information Technology Industry Council (ITI), will design a National IoT Strategy as a tool to inform policy makers on enabling the technology to deliver benefits for individuals, communities, innovators and the U.S. economy.

This announcement, Vice Chairman Kwon reinforced, "is not about the first steps – that's because IoT is already happening all around us. It's time to imagine the transformative potential of IoT for our societies – and learn how to achieve its human, social benefits at scale."

The event is part of Vision for Tomorrow, Samsung's recently launched public affairs platform for

cross-sector collaboration around issues affecting the policy dialogue in the U.S. and around the world.

For more information and to join the conversation visit @SamsungDC, #VisionforTech

Analog Devices' Optical Sensor Improves Reliability of Gesture Recognition Applications

Analog Devices, Inc. (ADI) announced an optical sensor for gesture recognition, which improves sensing accuracy and reliability over existing solutions by measuring a subject's position, proximity, and gestures from a single sensor. Competitive solutions requiring multiple sensors are often inaccurate, as the sensors "see" objects differently from varying angles making the signals difficult to combine. The single-point sensing used in the ADUX1020 optical sensor improves reliability of the application and reduces design complexity and cost for the system developer by requiring fewer components. Gesture recognition is an emerging user interface method in building and industrial control panels, where a user interacts with a device simply by motioning or gesturing. It is especially important in situations where touch-screen interfaces are challenged, such as in wet conditions, when a user is wearing gloves, or when a control panel is difficult to reach.

View the ADUX1020 product page, download data sheets, order samples and evaluation boards: http://www.analog.com/ADUX1020.html

Learn about ADI's optical sensor product portfolio http://www.analog.com/en/products/sensors/optical-sensors.html

Connect with engineers and ADI product experts on EngineerZone®, an online technical support community: https://ez.analog.com/welcome

In addition to single-point sensing, the ADUX1020 optical sensor features high ambient light rejection, which allows reliable and accurate operation under challenging lighting conditions. This too results in a more reliable application end user experience. Other optical sensors are often challenged by ambient light from sources like full sun, high frequency LED and fluorescents, all of which can disrupt the sensor's ability to interpret gestures accurately.

Analog Devices will be demonstrating the ADUX1020 optical sensor in booth #516 at the Sensors Expo & Conference, June 22-23 at the McEnery Convention Center, San Jose, CA.

ON Semiconductor Announces Sensorless Three-Phase Motor Controller for Automotive BLDC Implementation

ON Semiconductor (Nasdaq: ON), has further expanded its portfolio of motor controllers with the introduction of the LV8907UW. Supporting an operating voltage range from 5.5 to 20 volts (4.5 to 40 V transient), this high performance and feature-packed device enables streamlined solutions for driving three-phase brushless motors. The LV8907UW integrates gate drivers for six N-channel MOSFETs, and a dual-stage charge pump for 100% duty-cycle operation. In its lowest cost configuration the IC can operate without an external microcontroller. The device requires no programming, as key parameters and functions - such as startup and speed setting - can be configured via SPI interface and stored in embedded non-volatile (OTP) memory. Open-loop and closed-loop speed control are possible. For more complex applications the LV8907UW can also support a small microcontroller with its integrated linear regulator (3.3V or 5V, 50mA), a local interconnect network (LIN) transceiver for automotive connectivity, and a watchdog timer.

AEC-Q100 qualified, the LV8907UW's operational temperature range reaches up to 175°C, thereby ensuring reliable operation in challenging automotive environments. Integrated protection

mechanisms include over-current, over-voltage, short circuit, under-voltage, and over-temperature. The features of the device make it ideal for use in automotive water pumps, oil pumps, fuel pumps, HVAC systems, radiator fans, and headlamp cooling units.

“Compelled by market pressures and increasingly stringent legislative measures, automotive manufacturers need to find ways to improve the fuel economy of their models. Electrification of former mechanical applications – such as pumps and fans – is a key step in this path”, explains Ikuya Kawasaki, General Manager of System Solutions Group at ON Semiconductor. “Thanks to its high degree of integration and support for sensor-less operation, the LV8907UW enables motor systems to attain maximum efficiency levels without a microcontroller. The resulting designs have reduced complexity and bill of materials, and enhanced reliability.”

Packaging and Pricing

The LV8907UW is supplied in a SQFP48K package format. It is priced at $5.55 per unit in 2,500 unit quantities.

Follow @onsemi on Twitter: www.twitter.com/onsemi

Hitachi Automotive Systems is selected for Volkswagen's “FAST” strategic partner program in the field of gasoline injection systems

Hitachi Automotive Systems, Ltd. today announced that it has been selected by Volkswagen AG as a strategic partner in the field of gasoline injection systems for Volkswagen's Future Automotive Supply Tracks (FAST) program.

FAST was launched in February 2015, as a strategic partner program initiative for strengthening the relationship between Volkswagen and its suppliers, and accelerating innovations and global expansion in new product development.

The selection of the FAST partners is based on product capabilities, development capabilities, global footprint, and other evaluation items such as the transparency of corporate activities. As the outstanding partner in each field, the selected suppliers will be able to collaborate right from the beginning in Volkswagen's development of new products.

So far, 55 suppliers in 61 fields have been selected. Hitachi Automotive Systems' selection in the gasoline injection category reflects Volkswagen's high evaluation of Hitachi Automotive Systems' supply of high-quality, high-reliability Direct Injection Engine systems. On June 1st, Hitachi Automotive Systems and the other selected FAST partners convened at a FAST Summit held in Berlin, Germany, at which Volkswagen shared its strategic goals.

Hitachi Automotive Systems is utilizing its outstanding mechatronics and control technologies to develop and supply automotive equipment systems that contribute to the protection of the environment and to the elimination of traffic accidents. Hitachi Automotive Systems supplies Engine Management Systems that contribute to increasing engine efficiency, including, for the powertrains of internal combustion engines that account for more than 90% of the global vehicle market, Direct Injection Engine systems that are effective at reducing CO2 emissions, as well as Multi-Point Injection (MPI) systems that conform to international exhaust emissions regulations.

Hitachi Automotive Systems will further spread high-function systems in Europe and contribute to the protection of the environment through Volkswagen's FAST partner opportunity.

Qualcomm Announces Broad Support for Galileo Across Snapdragon Processor and Modem Portfolios

Qualcomm Incorporated (NASDAQ: QCOM) today announced that its subsidiary, Qualcomm Technologies, Inc., is supporting the European Galileo Global Navigation

Satellite System (GNSS) broadly in its product portfolios. While Qualcomm Technologies began implementing hardware support for Galileo several years ago in select chipsets, this announcement signals the mobile industry's first pervasive, end-to-end location-services platform for smartphone, computing, infotainment, telematics, and IoT applications.

With these optimized software enhancements, the Qualcomm® IZat™ location services platform now utilizes up to six satellite constellations concurrently without incremental device hardware or cost. Users now benefit from more than 80 different satellites when calculating global position for navigation or location-based applications. The addition of another GNSS is intended to provide more accurate location performance faster time-to-first-fix, and improved robustness all over the world, particularly in challenging urban environments where the combination of narrow streets and tall buildings can reduce accuracy.

"Accurate, reliable, and rapid position location is an important part of the mobile experience," said Alex Katouzian, senior vice president, product management, Qualcomm Technologies, Inc. "Qualcomm Technologies is helping to improve consumers' experiences with location-based services by adding Galileo support to our IZat location platform and deploying it broadly across our modem and application processor portfolios."

This feature is integrated in the latest Qualcomm® Snapdragon™ 800, 600, and 400 processors and modems. Galileo will be supported on smartphones and compute devices with the appropriate software release on Snapdragon 820, 652, 650, 625, 617, and 435 processors, automotive infotainment solutions utilizing Snapdragon 820A, and telematics and IoT solutions with Snapdragon X16, X12, X7, and X5 LTE Modems, and Qualcomm® 9x15 and MDM6x00 modems.

These enhanced processors and modems are designed to enable infotainment and telematics solution providers to satisfy an important component of the European eCall mandate ahead of the March 2018 deadline. "We are happy to announce support for the European Galileo satellite navigation system and to see that longstanding efforts and cooperation between the GSA, the European Commission, Qualcomm Technologies and the mobile ecosystem are delivering a key component of the European Digital Single Market," said Enrico Salvatori, president, Qualcomm Europe. "eCall and Galileo, together with upcoming advances in automotive connectivity pave the way to enhancing road safety and delivering new services to consumers."

"The Galileo constellation relies on 14 satellites in orbit today. Following our cooperation on Galileo integration, we welcome the announcement that Qualcomm Technologies is contributing to the rapid adoption of Galileo, in view of the Initial Services foreseen by end of 2016. The Galileo signal has demonstrated high performance and we believe will enhance user experience with more accurate and robust positioning," said Carlo des Dorides, executive director, European GNSS Agency.

The Snapdragon modem and application processor platforms' widespread ecosystem reach can accelerate mobile industry support for Galileo. To date, over 200 Galileo-enabled Qualcomm Technologies-based designs are already planned, and Qualcomm Technologies expects general availability of the required software in the 3rd quarter of 2016. IZat location solutions have been shipped in more than 5 Billion devices globally.

For more information on Qualcomm Technologies' mobile location technology please visit: https://www.qualcomm.com/products/izat.

Foldable 3-D, Man-Made Proteins Could Make "Use By" Dates for Medicines Obsolete

Soldiers often operate in extreme environments, where they may be exposed to the elements for long periods of time. Standard equipment such as electronics and armor are designed to withstand such stresses, but that is not true for the contents of a medic's bag. Most medicines, including essential biotherapeutics such as insulin, degrade rapidly when stored outside of specified temperature, humidity, and light conditions. DARPA's Fold F(x) program aims to develop new classes of rugged, shelf-stable medicines based on

non-natural, synthetic polymers that can better withstand extreme conditions in the field. The Agency will hold a workshop next week to describe recent successes and discuss applications with potential collaborators.

Biopolymers are large molecules created by stringing together smaller biochemical units, called monomers. Proteins are biopolymers made of hundreds or thousands of monomers called amino acids. The specific amino acids that are strung together to make a protein, and their linear order or "sequence," define the protein's final three-dimensional shape and, by virtue of that shape, its function. For example, insulin binds to specific molecular structures on the surface of cells precisely because of its specific 3D (folded) shape, which is determined by the sequence of its amino acid building blocks. Performers in the Fold F(x) program are leveraging this concept of "sequence defines shape defines function" to mimic the activity of naturally occurring biopolymers using completely new, laboratory-produced monomers. Because these monomers are synthetic, they can be designed to be more robust than their natural amino acid counterparts, opening the door to making proteins with new functional properties.

Since the late 1960s, researchers worldwide have attempted to design specific non-natural polymer sequences that would fold into specific three-dimensional shapes and perform a desired medicinal function. These one-off, targeted attempts at "rational drug design" have not yielded much success, in large part because scientists still have only a rudimentary means of predicting how the multitude of monomers in a biopolymer will interact and fold on one another. Performers in the Fold F(x) program are taking a completely different approach. Instead of trying to create the one perfectly folded polymer that will accomplish a desired biomedical function, they are creating massive suites of non-natural polymers with at least a billion distinct sequences that are hypothesized to fold into some generally desirable class of 3D shapes. They are then screening these polymer libraries with cutting-edge sorting technologies to identify which sequences in each library bind to a particular target of interest. The approach mimics that of the human immune system, which does not instantly produce antibodies that bind specifically to a newly encountered pathogen but rather produces a shotgun blast of varied antibodies, then amplifies production of the antibody that proves most effective at binding to and disabling the attacking microbe. There are significant challenges to producing large libraries of biopolymers and to screening for those best suited to a desired task, but the Fold F(x) program has been enjoying a string of successes. To date, six performer groups have built billion-plus non-natural polymer libraries and identified members that bind to known targets in application areas ranging from biopharmaceutical production to biowarfare agent detection. One group at the Massachusetts Institute of Technology (MIT), for example, created a non-natural polymer with demonstrated thermal and environmental stability that can recognize the well-known biowarfare agent anthrax. That specific recognition may be exploited to develop a rapid, field-stable diagnostic test for anthrax.

MIT is now also screening its non-natural polymer library in collaboration with the U.S. Army Medical Research Institute of Infectious Diseases to create synthetic biopolymers that bind to Ebola, in the hope of creating a totally new and robust Ebola treatment. A separate effort at Stanford University will use a newly developed screening capability based on high-throughput imaging technology to identify non-natural polymers that bind to inactivated Burkholderia pseudomallei and Burkholderia mallei, two bacterial pathogens of significant interest to the DoD.

Other teams have used the billion-member library strategy of the Fold F(x) program to generate and rapidly identify synthetic biopolymers that interact in very specific ways with a number of other targets. Some biopolymers are predicted to be resistant to digestion, for example, opening the door to oral versions of medicines that today must be injected because they would otherwise break down in the stomach. Others show promise as temperature-resilient compounds that could remain potent for decades instead of years, or shelf-stable diagnostics that could someday replace current counterparts that need to be kept refrigerated. Collaborators in DARPA's Fold F(x) program include University of California at Irvine, Harvard University, Scripps Research Institute, Lawrence Berkeley National Laboratory, and SRI International.

“With impressive results like these and ambitious new projects already underway, Fold F(x) is on track to improve biotherapeutic treatments and diagnostics, with potential benefits not just for our soldiers in combat but also for a wide array of civilian and commercial medical challenges,” said Tyler McQuade, DARPA program manager. “Just as plastics, which are non-biological polymers, transformed manufacturing in the middle of the last century, I see biopolymers revolutionizing biology and medicine in the decades ahead.”

The Fold F(x) program is positioned to build on its initial successes by generating, screening, and testing ever larger numbers of non-natural polymers that specifically bind to targets of high relevance to both the DoD and the civilian public health sector. Both diagnostic and therapeutic applications are envisioned—not only for bacterial and viral pathogens but also for toxins and resilience-relevant host-response targets.

DARPA will host a workshop on June 29, 2016, in Southbridge, Massachusetts, at which DARPA-funded Fold F(x) researchers will share with military and civilian public-sector stakeholders as well as with venture firms and potential private-sector collaborators details about the role Fold F(x) non-natural polymers could play in the future of biomedicine. Registration is required for workshop attendance, and space is limited. Interested parties should contact Dr. McQuade at http://go.usa.gov/cJJxQ.

Image Caption: A 3-D printed model of a non-natural Xenoprotein Anthrax Binder developed under DARPA's Fold F(x) program by researchers at MIT. This particular folded shape binds to the Anthrax pathogen, which is of interest to DoD. (DARPA Photo).

Hyperloop One Announces New Russian Partnership And Global Challenge Updates

Hyperloop One today extends its leadership on the path toward building the world's first full-scale Hyperloop. The company and The Summa Group, a diversified firm with significant infrastructure investments in Russia, signed a Memorandum of Understanding (MOU) with the city of Moscow to explore building high-capacity passenger systems connected to Moscow's transport grid. The agreement was signed at the St. Petersburg International Economic Forum. Hyperloop One now has feasibility studies underway in Finland and Sweden, The Netherlands, Switzerland, Dubai, the Port of Los Angeles and the United Kingdom.

"We are excited for the partnership between the Summa Group, the Russian Government and Hyperloop One to construct a Hyperloop in Moscow," said Shervin Pishevar, Co-founder and Executive Chairman of Hyperloop One. "Hyperloop can improve life dramatically for the 16 million people in the greater Moscow area, cutting their commute to a fraction of what it is today. Our longer term vision is to work with Russia to implement a transformative new Silk Road: a cargo Hyperloop that whisks freight containers from China to Europe in a day."

"The implementation of Hyperloop technology provides tremendous benefits to the Russian Federation in terms of the geopolitical development of the intracontinental transit potential and building of an economically attractive alternative to the existing global logistics flows," said Ziyavudin Magomedov, owner of the Summa Group. "In the long term, Hyperloop could catalyze the development of regional economic integration, including the Eurasian Economic Union and the Chinese initiative "One Belt - One Road."

The company also announced the judges for the Hyperloop Global Challenge, a first of its kind competition that will identify and select teams and locations with the best proposals to make Hyperloop a reality around the world.

The growing panel of judges for the Hyperloop One Global Challenge includes five of the world's leading experts in transportation, technology, economics and innovation: Peter Diamandis, Founder and Executive Chairman of the XPRIZE Foundation; Bassam Mansour, International Railway Industry Advisor; Clive Burrows, one of the world's most respected transport engineers; Alan Berger, Professor of Landscape Architecture and Urban

Design at Massachusetts Institute of Technology; and Ulla Tapaninen Senior Advisor or Economic Development at the City of Helsinki, Finland. This international panel of judges will review the entries towards the end of 2016. A shortlist of projects will then be scrutinized in more detail, and the panel will advise on the selection of three winners to be announced in March 2017.

"We have assembled the best and brightest minds, bringing together the world leaders in their respective fields to judge the Hyperloop One Global Challenge," said Rob Lloyd, CEO of Hyperloop One. "This growing panel of world-class experts has the experience and ability to work with us to decide what could be the world's first Hyperloop project."

The Hyperloop One Global Challenge launched on May 10, 2016 during the same time as the company's successful, full-scale Propulsion Test in North Las Vegas, Nevada, and has been a tremendous success with over 225 registrants from 45 countries in a little over a month's time. The Hyperloop One Global Challenge will provide an opportunity for individuals, companies and governments to develop competitive proposals using the first Hyperloop One solutions on transport corridors in their regions. For a complete list of what is needed for involvement as well as the appropriate entry forms, please see the Who Should Enter section at www.hyperloopchallenge.com.

The deadline for entries is September 15, 2016. Hyperloop One and the expert judges panel will select by March 2017 three finalists that best demonstrate the transformative power of Hyperloop and will be most likely to receive government, financial and regulatory support. Finalists will get additional access to the Hyperloop One ecosystem, technology, coaching, guidance and a dedicated Hyperloop One point person to work on taking plans to the next level. Teams that demonstrate real opportunity, favorable economics, strong government relations, a positive investment climate, and the willpower to advance regulatory climate stand the best chance of winning. Winners will be able to tap further into the network, getting full access to the technology and the ability to help raise capital in creative ways.

For more information on how to register for the Hyperloop One Global Challenge, please visit www.hyperloopchallenge.com.

STMicroelectronics Collaborates with Qualcomm on Sensors for Smart Mobile Devices

STMicroelectronics (NYSE: STM) , a global semiconductor leader serving customers across the spectrum of electronics applications, today announced that Qualcomm Technologies Inc., a subsidiary of Qualcomm Incorporated, intends to add software support for ST's inertial sensor solutions including its award-winning iNEMO™ inertial module. The Companies expect that the support will enable the rapid introduction of Android™ smartphones based on Qualcomm® Snapdragon™ processors with minimized power consumption and high-performing sensor capabilities through the use of hardware features integrated into the sensor. The reference software is already available to address the specific needs of OEMs creating new devices.

While the agreement extends to all of ST's inertial modules and sensors (motion, environmental, and acoustic), first efforts will focus on supporting ST's award-winning LSM6DS3 inertial module, recipient of the MEMS & Sensors Industry Group 'Product of the Year' recognition[1], in key Qualcomm Technologies' reference designs. The LSM6DS3 is an always-on, low-power inertial module combining a 3D accelerometer and a 3D gyroscope with superior sensing precision. The unique, flexible architecture of ST's sensors complements Snapdragon's ultra-low power approach to contextual-data processing. It supports extended battery life with Qualcomm All-Ways Aware™ hub for Android background sensor functions and numerous value-added features including the fusion of sensors with location technology, modem, and camera subsystems.

"Qualcomm Snapdragon products constitute one of the most technologically influential ecosystems in our increasingly mobile world," said Keith Kressin, senior vice president, product

management, Qualcomm Technologies, Inc. “We are pleased to work with ST to bring support for Snapdragon based platforms offering users improved sensing capabilities with improved battery life. Our joint efforts in offering superior, robust, tested, and certified solutions will help OEMs quickly and efficiently implement across regions.”

“We continue to see the expansion of different sensor types and combinations across the smartphone and mobile markets globally, and the work between ST and Qualcomm Technologies is expected to further grow the types of sensors in these devices,” said Andrea Onetti, General Manager, MEMS Sensors Division, STMicroelectronics. “We believe that the combination of ST sensors and Qualcomm Technologies’ processors in superior, robust, tested, and certified solutions that OEMs can design-in quickly can enable waves of new ultra-low-power devices to amaze and excite the ecosystem.”

Qualcomm and Snapdragon are trademarks of Qualcomm Incorporated, registered in the United States and other countries. Qualcomm All-Ways Aware is a trademark of Qualcomm Incorporated.

About STMicroelectronics

ST is a global semiconductor leader delivering intelligent and energy-efficient products and solutions that power the electronics at the heart of everyday life. ST’s products are found everywhere today, and together with our customers, we are enabling smarter driving and smarter factories, cities and homes, along with the next generation of mobile and Internet of Things devices. By getting more from technology to get more from life, ST stands for life.augmented.

In 2015, the Company’s net revenues were $6.90 billion, serving more than 100,000 customers worldwide. Further information can be found at www.st.com

[1] MEMS Executive Congress 2014 -- MEMS Industry Group slides 12/13 .

General Motors Global Compact Car Platform Now Includes Microchip’s MOST50 Automotive Infotainment Networking Solution

Microchip Technology Inc. (NASDAQ: MCHP), a leading provider of microcontroller, mixed-signal, analog and Flash-IP solutions, today announced that General Motors (GM) is using Microchip’s Media Oriented Systems Transport (MOST®) Intelligent Network Interface Controllers (INICs) to manage the infotainment system networking functions in their global compact car platform. This includes the Chevy Cruze, Chevy Volt, Opel Astra, Buick Excelle and Buick Verano. In addition to these GM compact cars, the synchronous, flexible, and cost-effective MOST networking technology has also been implemented in GM mid-size, full-size, performance, cross-over and SUV, truck and luxury platforms across all vehicle brands.

MOST is the de-facto networking system standard for 30 global car maker brands and over 204 vehicle models. MOST-based vehicles are now being manufactured worldwide, including North America, Asia and Europe. Since a MOST network can support multiple data types simultaneously, it enables the car manufacturers to offer system and feature set flexibility for current and future automotive infotainment applications. This also helps reduce the wiring harness weight for easier compliance with environmental regulations.

GM’s infotainment network utilizes Microchip’s MOST50 INIC with an electrical Physical Layer (ePHY), which is optimized for use with unshielded twisted pair (UTP) copper wire and meets the automotive industry's stringent EMC standards. MOST INICs provide industry-standard hardware interfaces to processor and peripheral devices for the efficient routing of audio, video, packet data, and control messages, which greatly simplifies module designs. End users can immediately access the vehicle’s infotainment system due to the MOST INIC’s ultra-fast network startup feature.

“The launch of MOST technology in GM’s compact cars solidifies the global acceptance of Microchip’s MOST system solutions in a wide variety of vehicle platforms and proves its value beyond the luxury car brands,” said Dan Termer, vice president of Microchip’s Automotive Information Systems Division. “Car makers can offer networking features cost-effectively because

of MOST technology's inherent synchronous nature and intelligent use of network bandwidth. Another advantage is Microchip's excellent systems-based applications engineering support throughout the car makers' platform development process."

MOST continues to extend its worldwide adoption as the high-speed networking technology developed by carmakers for carmakers. The MOST Cooperation, the organization through which the technology is standardized and refined, recently announced a procedure to begin the transfer of the MOST specifications to ISO (the International Organization for Standardization). This is being done to make the specifications more accessible through an internationally recognized and accredited standards organization, and establish an international standard that meets the OEM requirements of long-term stability, maintenance and reliability. This action follows international norms for continued development and supports involvement of worldwide stakeholders.

Samsung Introduces New Line-up of LED Components for Automotive Lighting, Featuring Chip-Scale Packaging

Samsung Electronics, a world leader in advanced component solutions, announced today that it has introduced "Fx-CSP", a line-up of LED packages which features chip-scale packaging* and flexible circuit board technology, for use in automotive lighting applications.

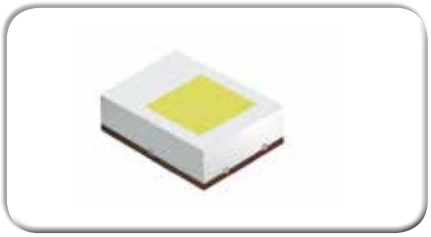
"Our new Fx-CSP line-up will bring greater design flexibility and cost competitiveness to the automotive lighting industry," said Jacob Tarn, executive vice president, LED Business Team, Samsung Electronics. He added that, "We will continue to introduce innovative LED products and technologies, such as multi-chip array technology, that can play a key role in the growth of the automotive LED lighting industry."

Samsung's new Fx-CSP provides an advanced combination of chip-scale packaging and flexible circuit board technology, which together enable more compact chip sizing and a higher degree of reliability. The use of a flexible circuit board also enables more heat to dissipate, which leads to lower resistance and brings about a greater degree of lumen-per-watt efficiency than using a ceramic board.

In addition, the new Samsung automotive LED line-up allows car designers to use a variety of chip arrangements such as a single chip, a 1 by 4, or a 2 by 6 multi-chip arrangement to suit different lighting configurations. The Fx-CSP line-up can be widely used in automotive lighting applications that include position lamps** and daytime** running lamps as well as headlamps** that require higher luminous flux and reliability than other automotive lamps.

The Fx-CSP line-up consists of single packages, Fx1M and Fx1L, with 1-3 watts each, as well as packages with a 14W high voltage array, Fx4 and a 40W high voltage array, Fx2x6. The variation in wattage levels allows Samsung LED lighting packages to work well with a wide range of exterior automotive lighting.

By adding the new Fx-CSP line-up to its existing mid-power and high-power automotive LED component line-ups, Samsung now provides a highly competitive family of automotive lighting components.



NASA Electric Research Plane Gets X Number, New Name

With 14 electric motors turning propellers and all of them integrated into a uniquely-designed wing, NASA will test new propulsion technology using an experimental airplane now designated the X-57 and nicknamed "Maxwell."

NASA Administrator Charles Bolden highlighted the agency's first X-plane designation in a decade during his keynote speech Friday in Washington at the American Institute of Aeronautics and Astronautics (AIAA) annual Aviation and Aeronautics Forum and Exposition, commonly called Aviation 2016.

"With the return of piloted X-planes to NASA's research capabilities – which is a key part of our 10-year-long New Aviation Horizons initiative – the general aviation-sized X-57 will take the first step in opening a new era of aviation," Bolden said.

As many as five larger transport-scale X-planes also are planned as

part of the initiative. Its goals – like the X-57 – include demonstrating advanced technologies to reduce fuel use, emissions and noise, and thus accelerate their introduction to the marketplace.

The X-57 number designation was assigned by the U.S. Air Force, which manages the history-making process, following a request from NASA. The first X-plane was the X-1, which in 1947 became the first airplane to fly faster than the speed of sound.

“Dozens of X-planes of all shapes, sizes and purposes have since followed – all of them contributing to our stature as the world’s leader in aviation and space technology,” said Jaiwon Shin, associate administrator for NASA’s Aeronautics Research Mission Directorate. “Planes like the X-57, and the others to come, will help us maintain that role.”

artist's concept of NASA's X-57 Maxwell aircraft

This artist's concept of NASA's X-57 Maxwell aircraft shows the plane's specially designed wing and 14 electric motors. NASA Aeronautics researchers will use the Maxwell to demonstrate that electric propulsion can make planes quieter, more efficient and more environmentally friendly.

Credits: NASA Langley/Advanced Concepts Lab, AMA, Inc.

NASA researchers working directly with the electric airplane also chose to name the aircraft “Maxwell” to honor James Clerk Maxwell, the 19th century Scottish physicist who did groundbreaking work in electromagnetism. His importance in contributing to the understanding of physics is rivaled only by Albert Einstein and Isaac Newton part of a four-year flight demonstrator plan, NASA’s Scalable Convergent Electric Propulsion Technology Operations Research project will build the X-57 by modifying a recently procured, Italian-designed Tecnam P2006T twin-engine light aircraft.

Its original wing and two gas-fueled piston engines will be replaced with a long, skinny wing embedded with 14 electric motors – 12 on the leading edge for take offs and landings, and one larger motor on each wing tip for use while at cruise altitude.

NASA’s aeronautical innovators hope to validate the idea that distributing electric power across a number of motors integrated with an aircraft in this way will result in a five-time reduction in the energy required for a private plane to cruise at 175 mph.

Several other benefits would result as well. “Maxwell” will be powered only by batteries, eliminating carbon emissions and demonstrating how demand would shrink for lead-based aviation fuel still in use by general aviation.

Energy efficiency at cruise altitude using X-57 technology could benefit travelers by reducing flight times, fuel usage, as well as reducing overall operational costs for small aircraft by as much as 40 percent. Typically, to get the best fuel efficiency an airplane has to fly slower than it is able. Electric propulsion essentially eliminates the penalty for cruising at higher speeds.

Finally, as most drivers of hybrid electric cars know, electric motors are more quiet than conventional piston engines. The X-57’s electric propulsion technology is expected to significantly decrease aircraft noise, making it less annoying to the public.

The X-57 research started as part of the NASA Aeronautics Research Mission Directorate's Transformative Aeronautics Program's Convergent Aeronautics Solutions project, with the flight demonstrations being performed as part of the Flight Demonstration Concepts project in the Integrated Aviation Systems Program.

For more information about NASA's electric propulsion research, go to: http://go.nasa.gov/1S55SPP

Mellanox Solutions Accelerate the Fastest Supercomputer in the World

Mellanox® Technologies, Ltd. (NASDAQ: MLNX), a leading supplier of end-to-end interconnect solutions for data center servers and storage systems, today announced that Mellanox interconnect solutions accelerate the world's fastest supercomputer, at the supercomputing center in Wuxi, China. The new number one supercomputer delivers 93 Petaflops (3 times higher compared to the previous top system), connecting nearly 41 thousand nodes and more than ten million CPU cores. The offloading architecture of the

Mellanox interconnect solution is the key to providing world leading performance, scalability and efficiency, connecting the highest number of nodes and CPU cores within a single supercomputer.

Mellanox's InfiniBand solutions now accelerate 45 Petascale systems, nearly 50 percent of the world Petascale-performance systems on the TOP500 list, 1.6 times more than the closest competitor. With the release of the new smart InfiniBand solutions, ConnectX-5 adapters and Switch-IB2 switch systems, and the expected release of 200G HDR InfiniBand in 2017, Mellanox InfiniBand-based Exascale technology will continue to enable supercomputing leadership across applications and geographies.

“InfiniBand technology has been accelerating multiple generations of the world's fastest supercomputers due to its performance, efficiency, scalability, robustness, and proven and standards-based leadership. Mellanox enabled the first Petaflop system in 2008, and now enables the world's first 100 Petaflop supercomputer,” said Eyal Waldman, president and CEO of Mellanox Technologies. “The world-wide demand for higher performance and faster real-time data analytics, requires smart interconnect solutions that deliver high data speeds, as well as open, standards-based technology to ensure backward and future compatibility for our applications. Mellanox InfiniBand and Ethernet solutions deliver data speeds from 10 to 100Gb/s, offloading the CPU to enable the highest data center return on investment and lowest cost of ownership. As we plan to introduce 200 and 400Gb/s solutions next year, Mellanox will continue to enable faster and more efficient high-performance computing, cloud, web2.0, database, deep learning and storage platforms.”.

The TOP500 supercomputer list has evolved to include both high-performance computing systems as well as cloud and Web2.0 Hyperscale infrastructures, mainly from the Asia-Pacific region. For the high-performance computing systems on the list, InfiniBand continues to demonstrate its technology leadership accelerating 70 percent of the systems. Overall, InfiniBand connects 41.2 percent of the TOP500 systems.

Mellanox's interconnect offloading architecture enables the most efficient system on the TOP500 list. Offloading architecture becomes more critical with the usage of accelerators and higher scale. InfiniBand enabled 53% higher system efficiency, higher system utilization and lower cost compared to Omni-Path. Additional comparisons demonstrated an average of 45% higher system performance at 25% lower cost per application performance in a recent HPC CPAR (Cost per Application Rating) benchmark review.

Published twice a year and publicly available at: www.top500.org, the TOP500 list ranks the world's most powerful computer systems according to the Linpack benchmark rating system. A detailed TOP500 presentation can be found here: www.mellanox.com/page/top_500

Visit Mellanox Technologies at ISC High Performance 2016 (June 20-23, 2016)

Visit Mellanox Technologies at its ISC High Performance booth #905 to see demonstrations and the full suite of Mellanox’s end-to-end high-performance InfiniBand and Ethernet solutions. For more information on Mellanox’s event and speaking activities at ISC 2016, please visit: www.mellanox.com/isc16

Supporting Resources:

Top500

Follow Mellanox on: Twitter, Facebook, Google+, LinkedIn, and YouTube

Join the Mellanox Community

The information regarding the inclusion of Mellanox interconnect solutions as part of the supercomputing center in Wuxi, China was first reported by Jack Dongarra (University of Tennessee) in his report on the Sunway TaihuLight System, published earlier today (Tech Report UT-EECS-16-742).

Safe Harbor Statement under the Private Securities Litigation Reform Act of 1995

This press release contains forward-looking statements within the meaning of the safe harbor provisions of the Private Securities Litigation Reform Act of 1995, including statements related to the performance of Mellanox’s InfiniBand and Ethernet solutions, ConnectX-5 adapters, Switch-IB2 switch systems and interconnect offloading architecture as well as statements related to the release and performance of Mellanox’s 200G

HDR InfiniBand. Forward-looking statements can often be identified by words such as "projects," "anticipates," "expects," "intends," "plans," "predicts," "believes," "seeks," "estimates," "may," "will," "should," "would," "could," "potential," "continue," "ongoing," similar expressions and variations or negatives of these words. These forward-looking statements are not guarantees of future results and are subject to risks, uncertainties and assumptions that could cause our actual results to differ materially and adversely from those expressed in any forward-looking statement. More information about the risks, uncertainties and assumptions that may impact our business is set forth in our annual report on Form 10-K filed with the Securities and Exchange Commission (SEC) on February 26, 2016 and our quarterly report on Form 10-Q filed with the SEC on April 29, 2016. Other risks, uncertainties and assumptions that could cause our actual results to differ materially from those projected may be described from time to time in reports we file with the SEC, including reports on Forms 10-Q and 8-K. We undertake no obligation to update or revise any forward-looking statements, whether as a result of new information, future events or otherwise.

Bluetooth® 5 quadruples range, doubles speed, increases data broadcasting capacity by 800%

New version of Bluetooth technology delivers “connectionless” IoT, advancing beacon and location-based capabilities in home, enterprise and industrial

Kirkland, Washington – June 16, 2016 – The Bluetooth Special Interest Group (SIG) announced that its next release, coming late 2016 to early 2017, will be called Bluetooth 5 and will include significantly increased range, speed, and broadcast messaging capacity. Extending range will deliver robust, reliable Internet of Things (IoT) connections that make full-home and building and outdoor use cases a reality. Higher speeds will send data faster and optimize responsiveness. Increasing broadcast capacity will propel the next generation of “connectionless” services like beacons and location-relevant information and navigation. These Bluetooth advancements open up more possibilities and enable SIG companies – now at an all-time high of 30,000 member companies – to build an accessible, interoperable IoT.

“Bluetooth 5 will transform the way people experience the IoT by making it something that happens simply and seamlessly around them,” said Mark Powell, executive director of the Bluetooth SIG. “Increasing operation range will enable connections to IoT devices that extend far beyond the walls of a typical home, while increasing speed supports faster data transfers and software updates for devices. And now with the ability to broadcast a much richer set of information, Bluetooth 5 will make beacons, location awareness, and other connectionless services an even more relevant part of an effortless and seamless IoT experience”

Bluetooth 5, projected for release in late 2016 to early 2017, will quadruple range and double speed of low energy connections while increasing the capacity of connectionless data broadcasts by 800 percent. It achieves all this alongside its industry-leading power performance. With the major boost in broadcast messaging capacity, the data being transferred will be richer, more intelligent. This will redefine the way Bluetooth devices transmit information, moving away from the app-paired-to-device model to a connectionless IoT where there is less need to download an app or connect the app to a device.

More than 371 million Bluetooth enabled beacons are projected to ship by 2020, according to Patrick Connolly, Principal Analyst at ABI Research. With eight times the broadcast messaging capacity, Bluetooth 5 will further propel the adoption and deployment of beacons and location-based services in the home automation, enterprise, and industrial markets. In scenarios where contextual awareness like navigation and pin-point location are crucial – such as hassle-free airport navigation experiences, asset tracking of warehouse inventory, emergency response, even smart city infrastructure that helps the visually impaired be more mobile – Bluetooth 5 will send custom information people actually find useful in that moment without connection and application barriers.

Added Powell, “Today, there are 8.2 billion Bluetooth products in use, and the enhancements in Bluetooth 5 and planned future Bluetooth technical advancements mean that Bluetooth will be in more than one-third of all installed IoT devices by 2020. The drive and innovation of Bluetooth will ensure our technology continues to be the IoT solution of choice for all developers. ”

The addition of the Bluetooth SIG’s 30,000th member company shows that more and more companies are choosing Bluetooth as both the technology and the organization that will help them develop IoT products and services with the best consumer experiences and help bring those products and services to market faster and more successfully. Membership has grown over 11 percent since the end of 2015, now reaching a record-high with its 30,000th member, Blossom Group. The startup, which is building infrasound and low-frequency noise relaxation products, is just the latest validation that companies of all sizes and verticals are joining the SIG because the organization is working in collaboration with its members to advance the technology and make the world smarter, safer, better, and more enjoyable.

“Implementing Bluetooth as our wireless technology and joining the SIG organization was the obvious choice to ensure our products’ success,” said Luke Sanger, CEO and co-founder of Blossom Group. “Bluetooth has the ubiquity of a trusted wireless communication platform and a great history of supporting market trends and working with developers and members to produce ground-breaking products and applications. We know Bluetooth will stay ahead of the game by working with its members and embracing technological advancements – from power efficiency to IoT connectivity – to push the limits of innovation.”

Parallel programming made easy

New chip design makes parallel programs run many times faster and requires one-tenth the code.

Larry Hardesty | MIT News Office

Computer chips have stopped getting faster. For the past 10 years, chips’ performance improvements have come from the addition of processing units known as cores.

In theory, a program on a 64-core machine would be 64 times as fast as it would be on a single-core machine. But it rarely works out that way. Most computer programs are sequential, and splitting them up so that chunks of them can run in parallel causes all kinds of complications.

In the May/June issue of the Institute of Electrical and Electronics Engineers’ journal Micro, researchers from MIT’s Computer Science and Artificial Intelligence Laboratory (CSAIL) will present a new chip design they call Swarm, which should make parallel programs not only much more efficient but easier to write, too.

In simulations, the researchers compared Swarm versions of six common algorithms with the best existing parallel versions, which had been individually engineered by seasoned software developers. The Swarm versions were between three and 18 times as fast, but they generally required only one-tenth as much code — or even less. And in one case, Swarm achieved a 75-fold speedup on a program that computer scientists had so far failed to parallelize.

“Multicore systems are really hard to program,” says Daniel Sanchez, an assistant professor in MIT’s Department of Electrical Engineering and Computer Science, who led the project. “You have to explicitly divide the work that you’re doing into tasks, and then you need to enforce some synchronization between tasks accessing shared data. What this architecture does, essentially, is to remove all sorts of explicit synchronization, to make parallel programming much easier. There’s an especially hard set of applications that have resisted parallelization for many, many years, and those are the kinds of applications we’ve focused on in this paper.”

Many of those applications involve the exploration of what computer scientists call graphs. A graph consists of nodes, typically depicted as circles, and edges, typically depicted as line segments connecting the nodes. Frequently, the edges have associated

numbers called “weights,” which might represent, say, the strength of correlations between data points in a data set, or the distances between cities.

Graphs crop up in a wide range of computer science problems, but their most intuitive use may be to describe geographic relationships. Indeed, one of the algorithms that the CSAIL researchers evaluated is the standard algorithm for finding the fastest driving route between two points.

Setting priorities

In principle, exploring graphs would seem to be something that could be parallelized: Different cores could analyze different regions of a graph or different paths through the graph at the same time. The problem is that with most graph-exploring algorithms, it gradually becomes clear that whole regions of the graph are irrelevant to the problem at hand. If, right off the bat, cores are tasked with exploring those regions, their exertions end up being fruitless.

Of course, fruitless analysis of irrelevant regions is a problem for sequential graph-exploring algorithms, too, not just parallel ones. So computer scientists have developed a host of application-specific techniques for prioritizing graph exploration. An algorithm might begin by exploring just those paths whose edges have the lowest weights, for instance, or it might look first at those nodes with the lowest number of edges.

What distinguishes Swarm from other multicore chips is that it has extra circuitry for handling that type of prioritization. It time-stamps tasks according to their priorities and begins working on the highest-priority tasks in parallel. Higher-priority tasks may engender their own lower-priority tasks, but Swarm slots those into its queue of tasks automatically.

Occasionally, tasks running in parallel may come into conflict. For instance, a task with a lower priority may write data to a particular memory location before a higher-priority task has read the same location. In those cases, Swarm automatically backs out the results of the lower-priority tasks. It thus maintains the synchronization between cores accessing the same data that programmers previously had to worry about themselves.

Indeed, from the programmer’s perspective, using Swarm is pretty painless. When the programmer defines a function, he or she simply adds a line of code that loads the function into Swarm’s queue of tasks. The programmer does have to specify the metric — such as edge weight or number of edges — that the program uses to prioritize tasks, but that would be necessary, anyway. Usually, adapting an existing sequential algorithm to Swarm requires the addition of only a few lines of code.

Keeping tabs

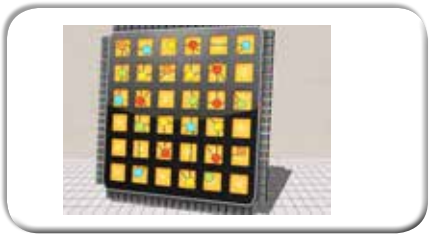
The hard work falls to the chip itself, which Sanchez designed in collaboration with Mark Jeffrey and Suvinay Subramanian, both MIT graduate students in electrical engineering and computer science; Cong Yan, who did her master’s as a member of Sanchez’s group and is now a PhD student at the University of Washington; and Joel Emer, a professor of the practice in MIT’s Department of Electrical Engineering and Computer Science, and a senior distinguished research scientist at the chip manufacturer NVidia.

The Swarm chip has extra circuitry to store and manage its queue of tasks. It also has a circuit that records the memory addresses of all the data its cores are currently working on. That circuit implements something called a Bloom filter, which crams data into a fixed allotment of space and answers yes/no questions about its contents. If too many addresses are loaded into the filter, it will occasionally yield false positives — indicating “yes, I’m storing that address” — but it will never yield false negatives.

The Bloom filter is one of several circuits that help Swarm identify memory access conflicts. The researchers were able to show that time-stamping makes synchronization between cores easier to enforce. For instance, each data item is labeled with the time stamp of the last task that updated it, so tasks with later time-stamps know they can read that data without bothering to determine who else is using it.

Finally, all the cores occasionally report the time stamps of the highest-priority tasks they’re still executing. If a core has finished tasks that have earlier time stamps than any of those reported by its fellows, it knows it can write its results to memory without courting any conflicts.

"I think their architecture has just the right aspects of past work on transactional memory and thread-level speculation," says Luis Ceze, an associate professor of computer science and engineering at the University of Washington. "'Transactional memory' refers to a mechanism to make sure that multiple processors working in parallel don't step on each other's toes. It guarantees that updates to shared memory locations occur in an orderly way. Thread-level speculation is a related technique that uses transactional-memory ideas for parallelization: Do it without being sure the task is parallel, and if it's not, undo and re-execute serially. Sanchez's architecture uses many good pieces of those ideas and technologies in a creative way."

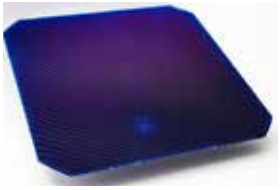


Imec Demonstrates Highly Efficient Bifacial Solar Cells with near 100% Bifaciality

Imec, the world-leading nano-electronics research center and partner in Energyville, will present at this week's Intersolar Europe/ EU PVSEC a highly efficient bifacial n-PERT (BiPERT) solar cell featuring a bifaciality value close to 100%. With a rear cell efficiency close to the efficiency measured from the front of the cell, imec's new achievement underscores the ability to strongly enhance the energy yield of photovoltaic (PV) modules made with this type of cell. Bifacial solar cells not only capture the light falling on the front side of the solar panel, but also the light that reaches the rear side of the panel, such as light that is reflected from the background, from clouds, diffuse light, and even direct light at sunrise or sunset. Bifacial modules can therefore generate more energy as compared to traditional monofacial modules. Published field tests have indicated that, depending on albedo values and bifaciality, bifacial gains from 10 – 40 percent are achievable. Bifacial cells can also be integrated into traditional glass-back sheet modules. In this configuration, they benefit from the scattering of infrared light at the back sheet to compensate for the lack of a rear metal reflector and from light reflection in the gaps between the cells.

Imec's bifacial n-PERT cells (BiPERT) feature very thin (< 5 µm) Ni/Ag plated contacts and no busbars on both sides of the cell, resulting in a symmetrical structure of high aesthetic value. The cells have the potential to deliver a very low Cost-of-Ownership (CoO), as they can profit from a bifacial gain, a low-cost metallization sequence, and the high efficiency potential of multi-wire interconnections that reduce optical shading and the required metal contact fraction.

The first experimental batch of BiPERT cells (n-type Cz-Si, size: 239cm2) resulted in very high bifaciality values. The current as measured from the rear (39.8 mA/cm2) was 97% of the one measured from the front (41.2 mA/cm2) (typical bifaciality values are around 80-90%). Moreover, imec's BiPERT cells with a rear emitter configuration reached excellent efficiencies up to 22.6% measured with a GridTOUCH system under Standard Test Conditions using only front side illumination and a non-reflective chuck. These efficiency measurements don't yet include the positive effect of the cells' bifaciality on the effective energy yield of the cell. Moreover, optimizations to the cell process and introducing a front emitter configuration are expected to further increase the cell efficiency and the energy yield. With these efficiency and bifaciality values, an effective efficiency of about 26% may be expected with a limited bifacial gain of only 15%".



Hallmark Envisions Real-Time Space Command and Control

Military commanders responsible for situational awareness and command and control of assets in space know all too well the challenge that comes from the vast size of the space domain. The volume of Earth's operational space domain is hundreds of thousands times larger than the Earth's oceans. It contains thousands of objects hurtling at

tens of thousands of miles per hour. The scales and speeds in this extreme environment are difficult enough to grasp conceptually, let alone operationally, as is required for commanders overseeing the nation's increasingly critical space assets.

Current space domain awareness tools and technologies were developed when there were many fewer objects in space. Only a few nations could even place satellites in orbit, and those orbits were easily predictable without advanced software tools. That situation has changed dramatically in the past decade with a developing space industry flooding once lonely orbits with volleys of satellite constellations. Despite this much more complex and chaotic environment, commanders with responsibility for space domain awareness often rely on outdated tools and processes—and thus incomplete information—as they plan, assess, and execute U.S. military operations in space.

To help address these technical and strategic challenges, DARPA is launching the first of two planned efforts under the Agency's new Hallmark program, which has the overarching goal to provide breakthrough capabilities in U.S. space command and control. This first effort, the Hallmark Software Testbed (Hallmark-ST), has as its primary goal the creation of an advanced enterprise software architecture for a testbed for tools that will integrate a full spectrum of real-time space-domain systems and capabilities. The testbed would be used to expedite the creation and assessment of a comprehensive set of new and improved tools and technologies that could be spun off into near-term operational use for the Defense Department's Joint Space Operations Center (JSpOC) and Joint Interagency Combined Space Operations Center (JICSpOC).

A Broad Agency Announcement (BAA) providing technical details about Hallmark-ST is available at http://go.usa.gov/xqqHm, and will be followed in the near future by a second BAA encompassing additional Hallmark goals.

"We envision a system that would fuse information from diverse sources and vastly reduce the overall time required to make and execute decisions and observe results," said Brad Tousley, director of DARPA's Tactical Technology Office (TTO), which oversees Hallmark. "For example, an intuitive user interface incorporating 3-D visualization technology would present complex information in novel ways and provide commanders with unprecedented awareness and comprehension. An advanced testbed featuring playback and simulation capabilities would significantly facilitate research and development activities, experiments, and exercises to evaluate new technologies for their impact on space command and control capabilities."

Specifically, Hallmark-ST seeks to design, develop, and maintain a state-of-the-art enterprise software architecture that would be flexible, scalable, secure, and capable of supporting tools and data from diverse sources. The architecture would need to support the ability to model current and future space situational awareness and command and control tools, capabilities, subsystems, and systems, as well as external capabilities and interfaces to support air, cyber, land, and maritime environments.

The enterprise architecture would be the backbone of a long-term testbed, the Hallmark Space Evaluation and Analysis Capability (SEAC), anticipated to be located in Northern Virginia. SEAC would provide for the effective development, integration, modeling and simulation, and realistic testing of software and decision-support processes relevant to space command and control. It would also eventually contribute to the rapid integration of technology into future space enterprise command and control systems. Furthermore, Hallmark personnel at SEAC would be integral to the actual integration of external space command and control tools, capabilities, and data, as well as execution of a number of anticipated tests and scenario-based exercises.

Questions about Hallmark-ST may be directed to the Hallmark BAA coordinator at DARPA-BAA-16-40@darpa.mil.

Image Caption: DARPA's new Hallmark program seeks to provide improved capabilities to rapidly plan, assess, and execute the full spectrum of U.S. military operations in space. Click below for high-resolution image."

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