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May 2016

About New-Tech Magazines Group

'New-Tech Magazines' A world leader in publishing high-tech and electronics, producing top quality publications read by tens of thousands professionals from all over the world especially from Europe, innovative electronics, IoT, microwave, homeland security, aerospace, automotive and technological industries.

Our specialized target audiences prefer New-Tech Europe because they know that our publications are a reliable source of the latest information in their respective fields. Our multidimensional editorials, news items, interviews and feature articles provide them with a full, well-rounded picture of the markets in which they operate - an essential asset for every technological leader striving to stay ahead, make the right decisions, and generate the next global innovation.

Moreover, as an attractive platform for advertisers from around the world, New-Tech Europe has become a hub for bustling international commercial activity. Here, through ads and other promotional materials, Israeli readers obtain crucial information about developers and manufacturers worldwide, finding the tools, instruments, systems and components they need to facilitate their innovative endeavors.

Targeting the needs of both the global and european industries and global advertisers, New-Tech Magazines Group constantly expands and upgrades its services. Over the years, the company has been able to formulate a remarkably effective, multi-medium mix of offerings, combining magazine publications with useful online activities, newsletters and special events and exhibitions.

Contents

Nokia completes the acquisition of Withings

Nokia announced that it has closed the acquisition of Withings S.A. earlier than had been expected. Through this acquisition, originally announced on April 26, 2016, Nokia Technologies has established a new Digital Health business unit led by Cédric Hutchings, formerly CEO of Withings, who reports to Ramzi Haidamus, president of Nokia Technologies.

The Digital Health business unit combines the talented employees from Withings and experts from the preventive health and patient care teams in Nokia Technologies. The new business unit builds on the pioneering work of Withings, offering a family of award-winning digital health products designed to fit seamlessly into people's lives, empowering them to make smarter decisions about the health and wellbeing of themselves and their families. The product line includes activity trackers, smart body analyzer scales, thermometers, blood pressure monitors, home and baby monitors and more, built on a sophisticated digital health platform. Together, under Cédric's leadership, the Digital Health team will continue to design smarter products for healthy living. "This is the beginning of an exciting new chapter in the history of Nokia Technologies as we extend our product portfolio to include a series of powerful digital health technologies," said Ramzi Haidamus, president, Nokia Technologies. "The Nokia brand is synonymous with innovation, connectivity and consumer technology and the acquisition of Withings puts us in a perfect position to capitalize on the huge opportunity in the health space. We're excited to welcome the Withings team to the Nokia family."

On June 9, Nokia Technologies will be hosting an invitation only event in San Francisco to share its vision for digital health and showcase its products, coinciding with the opening of its San Francisco office, in the heart of the Bay Area.

SIRIN LABS LAUNCHES SOLARIN: A MILITARY-GRADE SUPER SMART PHONE

SIRIN LABS announces the launch of SOLARIN - the world's first truly smart phone.

Privacy and mobile technology are the hot topics of today. As the value of digital information far eclipses that ever held under lock and key, we seek innovative encryption apps and secure technologies to protect ourselves. And yet no solution quite fits.

This is where SOLARIN comes in. Through a network of extraordinary partners, suppliers and passionate experts, and guided by the vision of our founders, SIRIN LABS has created a truly smart phone. Aimed at the international business person who carries a lot of sensitive information but doesn't want to compromise on usability, quality or design, SOLARIN combines advanced technology to make what we believe is the best mobile phone in the world. SOLARIN - Flat Front with Forcefield

Following over two years of R&D at bespoke facilities in Sweden and Tel Aviv, SOLARIN is made up of over 2,500 inner components within a meticulously designed exterior to achieve fast, seamless connectivity across any continent. Delivering tomorrow's technology, today, to the toughest audience with the most exacting requirements.

'We do not accept that price drives what's available in technology. With SOLARIN, we break the rules.' Moshe Hogeg, President and Co-founder, SIRIN LABS PRIVATE

SOLARIN features a carefully curated privacy package to keep your private information, private – unrivalled in terms of its sophistication and accessibility.

SOLARIN comes with Zimperium state-of-the-art mobile threat protection that thwarts the broadest array of advanced device, network and application mobile cyberattacks, without impairingusability or functionality of a top-of-the-range smartphone. In addition, SOLARIN incorporates the most advanced privacy technology, currently unavailable ➡

Redefining RF and Microwave Instrumentation

with open software and modular hardware
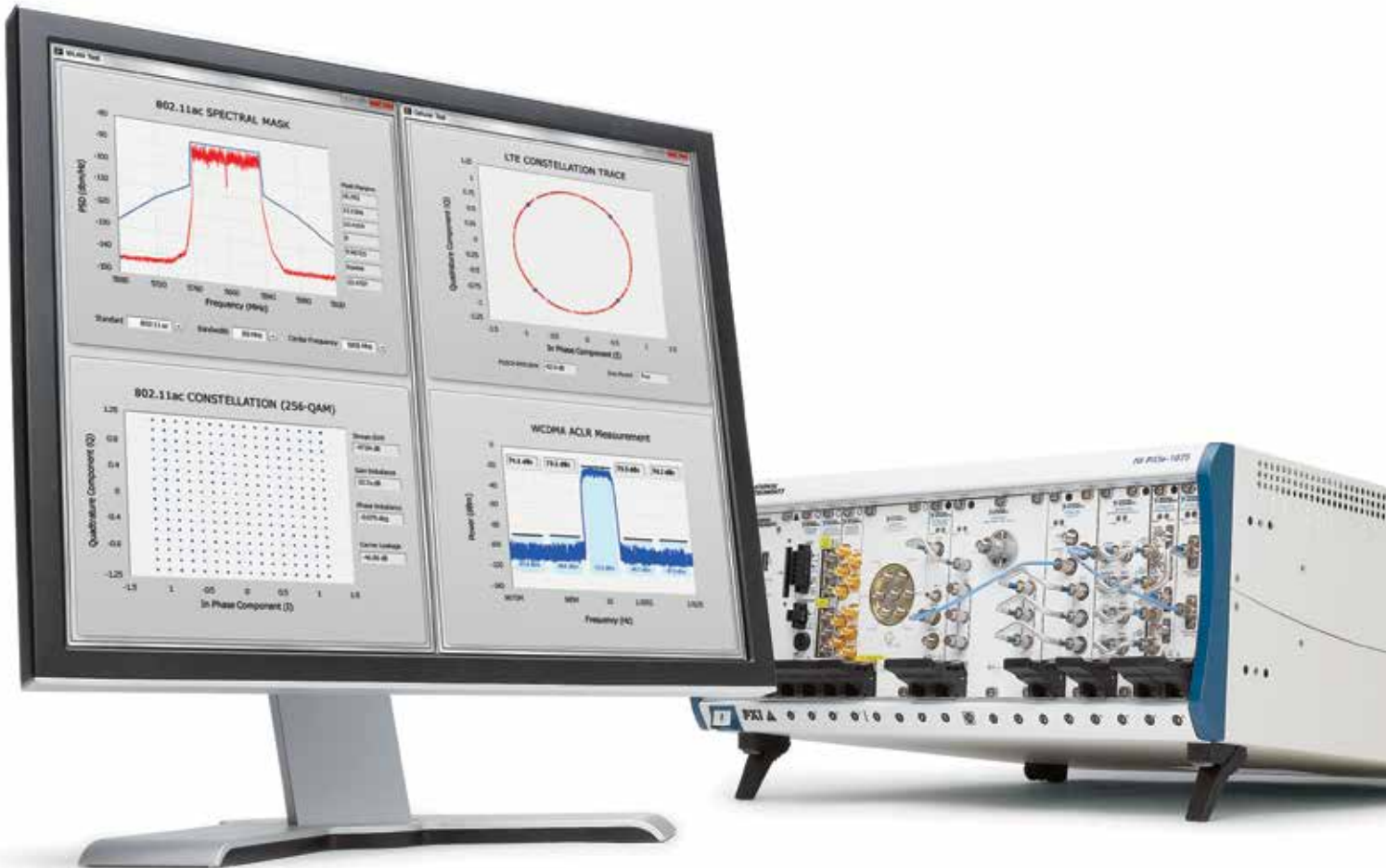
Achieve speed, accuracy, and flexibility in your RF and microwave test applications by combining National Instruments open software and modular hardware. Unlike rigid traditional instruments that quickly become obsolete by advancing technology, the system design software of NI LabVIEW coupled with NI PXI hardware puts the latest advances in PC buses, processors, and FPGAs at your fingertips.

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National Instruments supports a broad range of wireless standards including:

802.11a/b/g/n/ac	LTE
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NATIONAL INSTRUMENTS

→ outside the agency world. SIRIN LABS partnered with KoolSpan to integrate chip-to-chip 256-bit AES encryption, the same technology that militaries around the world use to protect their communications, offering the strongest possible mobile privacy protection worldwide. Activated by the unique Security Switch on the back of the handset, the phone enters a shielded mode, presenting an exclusive suite for fully encrypted calls and messages.

'Cyber-attacks are endemic across the globe. This trend is on the increase. Just one attack can severely harm reputations and finances. SOLARIN is pioneering new, uncompromising privacy measures to provide customers with greater confidence and the reassurance necessary to handle business-critical information.' Tal Cohen, CEO and Co-founder, SIRIN LABS

TRULY GLOBAL

SOLARIN is a truly global phone – offering faster data transfer and lasting performance.

SOLARIN is powered by a Qualcomm® Snapdragon™ 810 processor with X10 LTE and Wi-Fi, delivering high-performance connectivity. It offers up to 450 Mbps downlink and up to 150 Mbps uplink speeds, coupled with support for 24 bands LTE compatibility, setting a new benchmark in global usability. SOLARIN comes with far superior Wi-Fi™ connectivity than mainstream phones. It supports 802.11ac 2×2 MU-MIMO (multi user multiple input, multiple output) technology, offering up to three times the speed and capacity of conventional 1×1 configuration. In addition, SOLARIN incorporates revolutionary WiGig™ (802.11ad) multi-gigabit Wi-Fi technology. WiGig™ (802.11ad) offers speeds of up to 4.6Gbps, enabling near-instant cloud access, and synching of photos, videos and media, wire-equivalent docking and high-quality, low-latency video streaming, and more. Add to this the strongest battery in the premium and high end phone category, together with Qualcomm® Quick Charge™ for fast charging and power optimisation algorithms to create the essential travel companion. 'At every level, SOLARIN outperforms. Advanced carrier aggregation technology combines multiple LTE carriers for wider bandwidth, providing a faster, clearer connection. Using 802.11ac 2×2 MU-MIMO technology provides up to three times the bandwidth of a smartphone, and WiGig™ (802.11ad) pushes data transfer limits, allowing next generation features.' Fredrik Öijer, VP Product, SIRIN LABS

WATERFORD GETS A SELF-DRIVE CAR THANKS TO WIT ELECTRONIC ENGINEERING STUDENTS

Eight engineering students at WIT from across the South-East recently achieved a first for the Applied Robotics Lab with a Self-Driving Robotic Car. After just 12 weeks of working on the project students on the one-year BEng in Electronic Engineering, an add on course for the two-year Higher Certificate in Engineering in Electronic Engineering had a Toyota Corolla safely finish a test drive on the institute's Cork Road campus.

The students are part of the WIT School of Engineering Applied Electronics Stream, a study pathway that allows a student to get an honours degree in Applied Electronics

Pictured from left are: James Whelan, WIT Automotive Lecturer, Mark Ormsby, Castledermot, Co Kildare, Micheal Wall, Ballinamult, Co Waterford, Jenny Ball, Tramore, Adrian Cunningham, WIT Automotive Lecturer, Adrian Skowron, New Ross, Mark Dungan, Mullinavat, Mark MacManus, Waterford City, Shane Shortiss, Carrick on Suir, James Doughty, New Ross, Jason Berry, WIT Electronic Engineering Lecturer

without the prerequisite of Higher Level Maths.

The students were divided up into groups, the Vision team, the Acceleration Systems team, the braking team and the Steering Control Systems team. The Vision team was manned by James Doughty from New Ross and Shane Shortiss, Carrick-on-Suir. Students in the Acceleration Systems team were Adrian Skowron from New Ross and Mark Ormsby from Castledermot. The Braking team included students Mark McManus from Waterford city and Mark Dungan from Mullinavat. Micheal Wall, from Ballinamult was part of the Steering Control Systems team, along with Jenny Ball from Tramore.

→

"Achieving the 'White Board to Self-Drive Car' project in 12 weeks, eight WIT Electronic Engineering students have proven that anything is possible, if you keep moving forward. They have just completed a project never before attempted within WIT, in 12 weeks and it worked. One of the coolest sounds we have ever heard on a project was listening to the car increasing revs as its gets ready to go," said lecturer Jason Berry, the Lead Engineer in WIT's Applied Robotics Lab (ARL) lectures on the Higher Cert in Electronics, BEng in Electronics, BSc in Applied Computing, Masters in Electronic Engineering and Post Graduate Diploma in Business in Innovation Practice. "The project is the bread and butter of what any engineer is all about – figuring stuff out for yourself. Third year is a big transition for our students into the world of self =-learning."

Head of the School of Engineering at WIT, Ken Thomas outlined the prospects for students of electronic engineering. "Electronic Engineers are in high demand and short supply in Ireland. We in WIT want more Electronics students to equip them with the cutting-edge knowledge and skills that will allow them be very successful – and have great fun along the way with projects like Robo Car."

The team have since recorded a test drive for IrishTV's Waterford County Matters show and a video of the initial test drive is also available on www.wit.ie/selfdrivecar2016 and WIT social media accounts.

Berry's advice for school leavers and college applicants impressed by this project and who want to know if they would be suited a future in electronic engineering to get in contact with WIT staff.

"People can get in touch through the individual course pages. You can come in and have a look around at WIT, there is always a warm welcome in WIT Applied Robotics Lab."

There are also ways of learning about electronics from home. "Get yourself an arduino board and play with it right now, they are very cheap and there are loads of cool projects on the web. If you like the projects, who knows you might be onto something."

Previous graduates have been employed by Intel, Honeywell, Ericsson, Dell, Analog Devices, Bausch & Lomb, EMC.

Career opportunities for graduates of this course exist in various areas such as telecommunications, software and computer industry, research and development, electronic and IC design, production, test/maintenance, and control/automation departments.

ALMA Observatory pushing high Cisco technology

Located at 5,000 meter altitude at the Atacama Desert in Chile, ALMA, Atacama Large Millimeter/submillimeter Array, the world's largest radio observatory, is literally pushing Cisco® technology to the limits.

Having 66 antennas almost 15 meters tall – the eyes of ALMA – operating day and night to capture the signals of the universe to explain how stars and planets were formed is not an easy task. Low temperatures, high winds and snow, low humidity, dust, and a lack of oxygen are tough challenges that the ALMA staff and its network infrastructure have to endure.

To deal with one of the most extreme environments of the planet, it's required a robust and reliable digital network architecture to take all the data from the antennas to the brain of ALMA, a supercomputer capable of processing the information from the ALMA antennas in real-time and transforming it into one cohesive data stream.

Cisco solutions are deeply integrated within ALMA operations, making Cisco an end-to-end solution provider helping ALMA, the world's largest observatory, to fulfill its mission: unveiling the mysteries of the Universe.

"ALMA is, in simple words, a factory that produces scientific data and delivers them to the astronomical community, but for this supply chain to work, we need a reliable backbone, where we can support this process, and that is where Cisco plays a fundamental role", said Jorge Ibsen, Director of the Computing Department of ALMA. "For over 10 years we've been working with Cisco solutions and have always given us cutting edge technology, which is what ALMA needs to generate large amounts of reusable scientific data. We currently produce about 200 terabyte (TB) TB per year, and that volume of data is expected to increase significantly over the following years in operations".

"For a unique operation such as Alma to work, it is essential that the infrastructure operates in extreme conditions, but with the same advanced features and capabilities as if they were in a traditional office environment. One of the secrets to Cisco's success is our ability to customize our solutions to meet the needs in various industries, their special requirements and unique conditions", explained Mariana Portela, account manager at Cisco Chile.

Unveiling the Mysteries of the Universe

For that purpose, ALMA is using Cisco Catalyst 6500 Core ➡

→ switches capable of working at high altitude allowing great reliability in this extreme environment, and advanced functionalities. This critical equipment is installed in a data center located inside of the Array Operations Site Technical Building located at 5000m altitude. The building has oxygen injection, precise cooling systems and power lines to ensure optimal operational conditions, making it the highest data center in the world.

The antennas produce hundreds of gigabits (GB) of data every day, which are processed in the ALMA supercomputer – the Correlator – and then sent to the Operations Support Facility (OSF) at 2.900m altitude, located at 28Km from San Pedro de Atacama in the middle of the desert, through dedicated fiber optics links. The OSF hosts a data center, state-of-the-art labs, offices and dormitories allowing more than 200 persons to work every day, with reliable Internet access, Wi-Fi connections, video conferencing, telephone and presence services through Cisco network equipment, providing critical services given the remote nature of the facilities.

It's at the control room in the OSF, the decision-making neurons of ALMA, where astronomers and operators command all the antennas to observe the universe and where the captured data is stored, essentially acting as the short term memory of ALMA. To do that, a set of servers, storage units and very specialized software is needed to control the 66 antennas. However, a great challenge was presented to maximize the operation throughput of the onservatory, groups of antennas needed to be controlled and operated independently from others and to act as parallel production lines. But duplicating the control hardware and software was too expensive, and the workload for reconfiguring them and to change all the required optic cabling to properly connect each single antenna was overwhelming.

The New Intel® Core™ i7 Processor Extreme Edition: Intel's Most Powerful Desktop Processor Ever

Ultimate Platform for Gaming and Content Creation

Designed for the extreme performance needs of enthusiasts, the Intel® Core™ i7 processor Extreme Edition delivers with up to 10 cores and 20 threads, 40 PCIe* lanes, and a new Intel® Turbo Boost Max Technology 3.0 to tame the most demanding workloads. When game and content creators need incredible performance, they turn to Extreme Edition. Gamers today do more than just gameplay; they're playing in 4K, they live-stream, record, edit and upload their highlights online, and communicate in real time with their eSports team or competitors. We call this mega-tasking, when simultaneous, compute-intensive, multithreaded workloads are needed. The Intel Core i7 processor Extreme Edition has up to 35 percent better 3D rendering performance1 for vivid 4K gameplay while accomplishing other compute-intensive tasks in the background. A new era in virtual reality has also begun and achieving the premium VR experiences delivered by the leading headmounted displays on the market requires powerful PCs for both consuming and creating VR content.i7core

Content creators also mega-task: They are editing, creating visual effects and composing music simultaneously. Creators also want to see the end result as they're in the process of creating it, so with the ability to support multiple 4K displays along with the threads and performance to handle all of the simultaneous applications, Intel Core i7 processor Extreme Edition helps people spend more of their time creating and less time waiting.

Intel Core i7 processor Extreme Edition opens up new levels of performance and capability enthusiasts never thought possible. Forty PCIe lanes connected directly into the CPU allow for system expansion with fast SSDs, up to four discrete GFX cards and ultra-fast Thunderbolt™ 3.0 technology. Massive Intel® Smart Cache of up to 25MB and quad-channel memory improves responsiveness and decreases startup time when working with large files and applications. The new Intel® Turbo Boost Max Technology 3.0 steers applications to the highest-performing core, improving single-threaded performance by up to 15 percent2 . The Intel® Core™ i7-69xx/68xx processor family is also unlocked, an important feature for enthusiasts who want the extra headroom and tools to push their system to the limit3 . With this revolution in performance and flexibility, Intel's first ever 10-core desktop consumer processor delivers the cores and threads to handle the mega-tasking workloads of today's gamers and creators.

Qualcomm Extends Industry-Leading Snapdragon Wear Lineup with New Processor, Platforms and Support for Targeted-Purpose Wearables

Qualcomm Incorporated (NASDAQ: QCOM) today announced at COMPUTEX 2016 that its subsidiary, Qualcomm Technologies, Inc., is introducing the new Qualcomm® Snapdragon™ Wear 1100 processor for the fast growing targeted-purpose wearables segments such as connected kid and elderly watches, fitness trackers, smart headsets, and wearable accessories. The Snapdragon Wear 1100 processor complements theSnapdragon Wear 2100 processor, which is designed for multi-purpose wearables, and joins the Snapdragon Wear product family.

Snapdragon Wear 1100: Designed for Targeted-purpose Wearable Devices

Snapdragon Wear 1100 is designed for the next generation of targeted-purpose wearable segments where consumers are demanding a smaller size, longer battery life, smarter sensing, secure location, and an always connected experience. This processor excels in meeting these requirements with low power features such as Power Save Mode (PSM), industry leading compact packages, and next gen Cat 1 modem with LTE/3G global band support.

The Snapdragon Wear 1100 also features an integrated applications processor for Linux-based applications and scales to support voice, Wi-Fi®, and Bluetooth®, thus supporting a seamlessly connected experience. Additionally, the Snapdragon Wear 1100 incorporates the Qualcomm® iZat™ integrated location engine to offer enhanced accuracy and power optimization through such features as multi-GNSS, cell-ID positioning, and ability to support applications that utilize geo-fencing for safety monitoring. Integrated in the chipset are the hardware cryptographic engine, HW random number generator, and TrustZone, which supports a highly secure environment for consumers. Snapdragon Wear 1100 is commercially available and shipping today.

OEM Products Bring Innovative Experiences to Consumers

In addition to the platform announcements, a number of OEMs launched connected kid watches at the event:

Anda Technologies announced plans to launch its kid watch, based on the Borqs reference design, for the Latin America region. "As a father of two young children, I conceived the original idea of creating a symbol-based communications product out of my own need to stay emotionally connected to them throughout the day," said Jose Delmar, chief executive officer, Anda Technologies. "Our Android-based connected wearable, based on the Qualcomm Snapdragon Wear 2100 processor, offers a plethora of unique functions, innovative design, and top of the line materials, making it unlike any other children's wearable product available in the marketplace."

Imec and its Solliance Partners Present First Semi-Transparent Perovskite Modules

Nanoelectronics research center imec, partner in Solliance, presented the first-ever semi-transparent perovskite PV-module, achieving power conversion efficiencies up to 12%. The technology enables for semi-transparent PV-windows which are a key towards Zero-Energy Buildings. Moreover, combining these semitransparent perovskite modules with Si solar cells, an unprecedented 20.2% in power conversion efficiency for a perovskite/Si stacked solar module was achieved.

Stand-alone perovskite solar modules feature excellent power conversion efficiencies and can be manufactured with simple fabrication technologies, such as coating and printing. Perovskites can also be manipulated to be realized on flexible (plastic films or metal foils) as well as rigid (glass, metal) carriers. Optical and electrical properties of the perovskite solar cells can be varied by tuning the composition of the material components and thereby adjusting color and transparency. The semi-transparent perovskite modules of imec realized by scalable coating techniques showed efficiencies of 12% on sizes as large as 4 cm2 and 10 % on sizes as large as 16cm2, a world-best achievement in this domain. The combination of perovskite solar modules on top of silicon solar modules bears the exciting potential of achieving power conversion efficiencies greater than 30 percent, ➡️

➡️ thereby surpassing the efficiencies of the best single junction Si solar cells. Imec's novel stacked module concept features a highly transparent perovskite solar module stacked on top of interdigitated back contacted (IBC) silicon solar cells. All devices had the same area and the semi-transparent perovskite top module shows a 70 percent transmission of light towards the crystalline Si solar cell. An unprecedented power conversion efficiency of 20.2 percent was reached for the resulting stacked perovskite/Si solar module of relevant sizes of 4 cm2. Moreover, a power conversion efficiency of 17.2% was achieved for larger areas of up to 16cm2, employing a Si bottom solar module of 4 interconnected IBC cells, also representing a record result for

this size.

Tom Aernouts, Thin Film PV Technology Manager at imec commented "We are proud about these results as they show we have excellent control over the performance as well as the upscaling capabilities of this technology. Our future work will continue in increasing module sizes and optimizing the perovskite solar cell technology." Ulrich Paetzold, researcher at the Thin Film PV group at imec added: "With a mm-size perovskite solar cell stacked on our IBC solar cell even efficiency as high as 22% has been obtained. But advancement of the perovskite/Si stacked solar module technology relies on demonstrators of realistic sizes."

New concept turns battery technology upside-down Pump-free design for flow battery could offer advantages in cost and simplicity

A new approach to the design of a liquid battery, using a passive, gravity-fed arrangement similar to an old-fashioned hourglass, could offer great advantages due to the system's low cost and the simplicity of its design and operation, says a team of MIT researchers who have made a demonstration version of the new battery.

Liquid flow batteries — in which the positive and negative electrodes are each in liquid form and separated by a membrane — are not a new concept, and some members of this research team unveiled an earlier concept three years ago. The basic technology can use a variety of chemical formulations, including the same chemical compounds found in today's lithium-ion batteries. In this case, key components are not solid slabs that remain in place for the life of the battery, but rather tiny particles that can be carried along in a liquid slurry. Increasing storage capacity simply requires bigger tanks to hold the slurry. But all previous versions of liquid batteries have relied on complex systems of tanks, valves, and pumps, adding to the cost and providing multiple opportunities for possible leaks and failures.

The new version, which substitutes a simple gravity feed for the pump system, eliminates that complexity. The rate of energy production can be adjusted simply by changing the angle of the device, thus speeding up or slowing down the rate of flow.
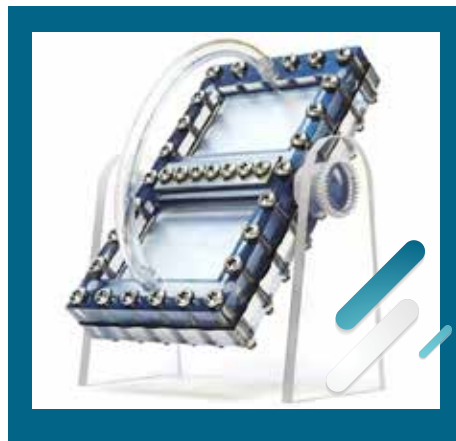
The concept is described in a paper in the journal Energy and Environmental Science, co-authored by Kyocera Professor of Ceramics Yet-Ming Chiang, Pappalardo Professor of Mechanical Engineering Alexander Slocum, School of Engineering Professor of Teaching Innovation Gareth McKinley, and POSCO Professor of Materials Science and Engineering W. Craig Carter, as well as postdoc Xinwei Chen, graduate student Brandon Hopkins, and four others.

Chiang describes the new approach as something like a "concept car" — a design that is not expected to go into production as it is but that demonstrates some new ideas that can ultimately lead to a real product.

The original concept for flow batteries dates back to the 1970s, but the early versions used materials that had very low energy-density — that is, they had a low capacity for storing energy in proportion to their weight. A major new step in the development of flow batteries came with the introduction of high-energy-density versions a few years ago, including one developed by members of this MIT team, that used the same chemical compounds as conventional lithium-ion batteries. That version had many advantages but shared with other flow batteries the disadvantage of complexity in its plumbing systems.

The new version replaces all that plumbing with a simple, gravity-fed system. In principle, it functions like an old hourglass or egg timer, with particles flowing through a narrow opening ➡️

from one tank to another. The flow can then be reversed by turning the device over. In this case, the overall shape looks more like a rectangular window frame, with a narrow slot at the place where two sashes would meet in the middle.

In the proof-of-concept version the team built, only one of the two sides of the battery is composed of flowing liquid, while the other side — a sheet of lithium — is in solid form. The team decided to try out the concept in a simpler form before making their ultimate goal, a version where both sides (the positive and negative electrodes) are liquid and flow side by side through an opening while separated by a membrane.

Solid batteries and liquid batteries each have advantages, depending on their specific applications, Chiang says, but "the concept here shows that you don't need to be confined by these two extremes. This is an example of hybrid devices that fall somewhere in the middle."

The new design should make possible simpler and more compact battery systems, which could be inexpensive and modular, allowing for gradual expansion of grid-connected storage systems to meet growing demand, Chiang says. Such storage systems will be critical for scaling up the use of intermittent power sources such as wind and solar.

While a conventional, all-solid battery requires electrical connectors for each of the cells that make up a large battery system, in the flow battery only the small region at the center — the "neck" of the hourglass — requires these contacts, greatly simplifying the mechanical assembly of the system, Chiang says. The components are simple enough that they could be made through injection molding or even 3-D printing, he says.

In addition, the basic concept of the flow battery makes it possible to choose independently the two main characteristics of a desired battery system: its energy density (how much energy it can deliver at a given moment) and its power density (how much total power can be stored in the system). For the new liquid battery, the power density is determined by the size of the "stack," the contacts where the battery particles flow through, while the energy density is determined by the size of its storage tanks. "In a conventional battery, the power and energy are highly interdependent," Chiang says.

The trickiest part of the design process, he says, was controlling the characteristics of the liquid slurry to control the flow rates. The thick liquids behave a bit like ketchup in a bottle — it's hard to get it flowing in the first place, but then once it starts, the flow can be too sudden. Getting the flow just right required a long process of fine-tuning both the liquid mixture and the design of the mechanical structures.

The rate of flow can be controlled by adjusting the angle of the device, Chiang says, and the team found that at a very shallow angle, close to horizontal, "the device would operate most efficiently, at a very steady but low flow rate." The basic concept should work with many different chemical compositions for the different parts of the battery, he says, but "we chose to demonstrate it with one particular chemistry, one that we understood from previous work. We're not proposing this particular chemistry as the end game."

Venkat Viswanathan, a research scientist at Lawrence Berkeley National Laboratory who was not involved in this work, says: "The authors have been able to build a bridge between the usually disparate fields of fluid mechanics and electrochemistry," and in so doing developed a promising new approach to battery storage. The work was supported by the Joint Center for Energy Storage Research, funded by the U.S. Department of Energy. The team also included graduate students Ahmed Helal and Frank Fan, and postdocs Kyle Smith and Zheng Li.

Microsoft announces streamlining of smartphone hardware business

Microsoft Corp. announced plans to streamline the company's smartphone hardware business, which will impact up to 1,850 jobs. As a result, the company will record an impairment and restructuring charge of approximately $950 million, of which approximately $200 million will relate to severance payments.

"We are focusing our phone efforts where we have differentiation — with enterprises that value security, manageability and our Continuum capability, and consumers who value the same," said Satya Nadella, chief executive officer of Microsoft. "We will continue to innovate across devices and on our cloud services across all mobile platforms."

Microsoft anticipates this will result in the reduction of up to 1,350 jobs at Microsoft Mobile Oy in Finland, as well as up to 500 additional jobs globally. Employees working for Microsoft Oy, a separate Microsoft sales subsidiary based in Espoo, are not in scope for the planned reductions.

As a result of the action, Microsoft will record a charge in the fourth quarter of fiscal 2016 for the impairment of assets in its More Personal Computing segment, related to these phone decisions.

Sensifree Secures $5M in Series A Financing Led by TransLink Capital

Sensifree, the pioneer in low power, contact free, electromagnetic sensors that accurately collect a range of continuous biometric data without the need to touch the human body, today announced it has completed a $5.0 million Series A round of financing. TransLink Capital led the investment round with participation from existing and new investors, including UMC Capital, a subsidiary of United Microelectronics Corp. (NYSE: UMC) and an undisclosed strategic investor. The investment adds to seed investment made by Samsung's Catalyst fund and brings Sensifree's total funding since launching its revolutionary RF-based biometric sensor technology to $7 million. The funding
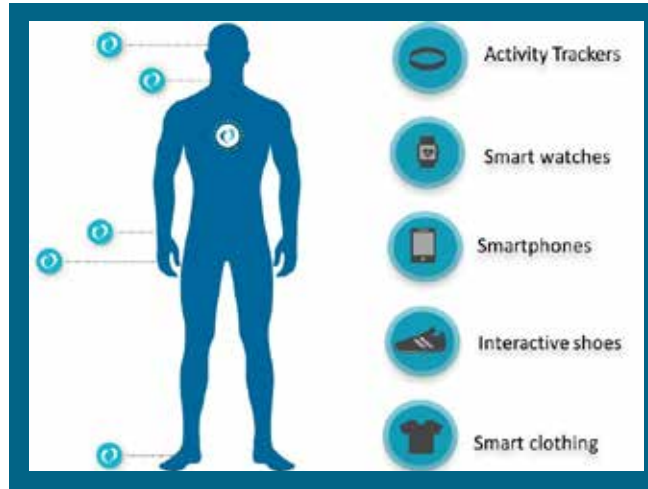
will help the company aggressively expand its engineering and product development teams, and accelerate its business development efforts. TransLink Capital Venture Partner and Senior Advisor, Eric Hsia, will join the Sensifree Board of Directors.

Sensifree brings a technology breakthrough to the fast growing wearable and digital health markets, aiming to provide a better alternative to decades-old sensor technologies, with its patent pending RF-based technology. The Company's first product is a contactless heart rate sensor for wearable devices for applications such as traditional watches, fitness trackers and smart clothing.

A new treatment room design model for future hospitals

In the EVICURES project a design model for future intensive and intermediate care facilities was developed at Seinäjoki Central Hospital. The results of research conducted by VTT Technical Research Centre of Finland Ltd on evidence-based design (EBD) and user-orientation were applied to the design work. The project will be realised when Finland's first single-patient intensive and intermediate care and cardiac unit designed in accordance with the model becomes operational in 2018.

The need for intensive and intermediate care will increase, and hospitals must be developed to meet future needs. "The international trend is that the need for intermediate care in particular is increasing. More and more demanding methods are being used for treating patients, and the share of elderly patients is increasing," says Kari Saarinen, Project Manager of the EVICURES project and Chief Physician at ICU, Hospital District of South Ostrobothnia.

The EVICURES project developed a new design model on the basis of Seinäjoki Central Hospital's needs for intensive and intermediate care facilities using evidence based design (EBD), which is built upon evidence, research results or strong practical experience. An additional goal was to improve the quality and effectiveness of operations, and to increase both patient and staff satisfaction.

There are currently no ICUs with single patient rooms in Finland.

Seinäjoki Central Hospital's new intensive and intermediate care unit will feature 24 single patient rooms. "The operations will be more cost-efficient and of higher quality, when the equipment and nursing staff are concentrated into one place. We also expect the solution to have remarkable effects on patient healing," Saarinen emphasizes.

Nursing staff's experiences and views used as a basis for development work

The hospital staff, management, patients and their families, the hospital district, and other cooperation partners participated in the design work. "VTT produced the technical research data, which was combined with medical knowledge, practices and future visions contributed by the hospital. This enabled transforming theory into practice," Saarinen notes.

When the project was launched in 2014, questionnaires were conducted extensively among hospital staff and patients in order to survey views on such issues as architecture, indoor conditions, durability, functionality, safety, accessibility and usability.

"A user-oriented approach was an essential foundation for the whole project. This way we can all together make the major change about to happen easier, when the nursing staff is moving from facilities for multiple patients to working alone in single rooms," says Tiina Yli-Karhu, Design Coordinator, Hospital District of South Ostrobothnia.

Increasing Production Line Performance and Reducing Operations Costs with IoT Technologies

> Advantech-Intel

Executive Summary

Equipment maintenance personnel are tasked with keeping the production line running at peak performance while minimizing operations costs. This is made more difficult by the need for specialized skill sets to support a wide range of factory devices that use different communications protocols, data formats, and device management tools, etc. Greatly simplifying this task, it is possible to seamlessly link factory floor devices and processes using technologies from the Internet of Things (IoT), thus enabling remote equipment monitoring and management from a centralized dashboard.

Providing such a solution, the SUSIAccess* remote management system from Advantech* allows maintenance personnel to perform equipment status and maintenance checks from a web browser at any time, from anywhere, and with any connected device. The factory automation solution uses an Intel® processor-based gateway running an Advantech client-side agent to transparently handle protocol and data conversion, and acts as a conduit between manufacturing equipment and the Advantech server-side software. This solution can interoperate with high-level applications such as data analytics and machine learning. This paper details the benefits and the key ingredients of the solution.

Key Business Objectives

Increase production line performance and reduce operations costs without sacrificing quality.

Business Challenge

Although large manufacturers have been using statistical process control and statistical data analysis to optimize production for years, the extreme complexity of today's data provides opportunities to deploy new approaches, infrastructure, and tools. The challenge is figuring out how to cost-effectively unify device management, control, and data analytics.

In addition, manufacturers need a real-time device management platform that enables them to address maintenance issues on a timely basis. Today, there are many disparate manufacturing systems with their own management tools, which makes maintenance cumbersome and time consuming.

Solution Beneits

Revolutionizing factory equipment management in the IoT era, the Advantech SUSIAccess remote management system delivers the following advantages:

● **Reduced Total Cost of Ownership (TCO):** Saving time for maintenance personnel, centralized remote monitoring continuously checks factory floor devices and sends alerts to their mobile devices as needed. Power usage may be lowered by automatically powering systems on/ of according to a preset schedule.

●**Improved Production Line Performance:** Machine data aggregated by the SUSIAccess server is processed by big data analytics to uncover ways to increase product yields, improve predictive maintenance, and identify manufacturing problems more quickly.

● **Easy Integration:** The solution provides a comprehensive, seamless, device monitoring and control system that
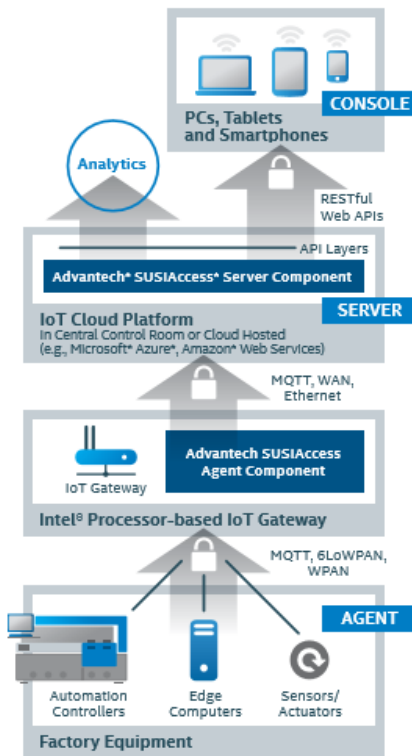
Figure 1. High-Level Structure of Factory Automation Solution

includes both hardware and software.

● **Higher Equipment Availability:** If a system fails, the keyboard-video- mouse (KVM) feature enables remote diagnosis and recovery for most software issues, enabling factory devices to be brought on line much faster and at lower cost than sending a technician onsite.

Solutions can be tailored to meet the specific requirements of different factory environments given Advantech's comprehensive system integration experience. Founded in 1983, Advantech is a leader in providing trusted, innovative hardware and software products, services, and global logistics support.

Solution Overview

Advantech has taken its turnkey solutions for factory automation to a new level by incorporating IoT technologies as the foundation for a cloud-based platform running data analytics, remote management, and a wide range of third-party applications. This is done with a cloud management framework consisting

Figure 2. Centralized Remote Monitoring

of three layers - web-based Console, Server, and Agent - as illustrated in Figure 1.

1.   Agent: SUSIAccess client-side software runs on Advantech IoT gateways or IoT devices (e.g., automation controller, edge computer, and sensors/actuators) on the factory floor.

2.   Server: A central control room or a cloud-based service, such as Microsoft* Azure* and Amazon* Web Services, runs SUSIAcess server-side software that is in direct contact with agents.

3.   Console: A web-based interface that communicates with Agents via the Server, presenting IoT device status and configuration data.

Solution Capabilities

The Advantech Smart Production Line solution provides a range of powerful features to monitor factory devices and perform remote operations.

1.   Centralized   Remote Management The Advantech Console-Server- Agent structure allows administrators to perform device status and maintenance checks - at anytime and from anywhere - via the web browser-based SUSIAccess console. Administrators can easily manage all of their devices by simply using their PCs, smartphones, and tablets. The solution also provides a distributed connectivity structure, which solves the challenges brought on by large-

scale or multi-site device management.

2.   Hardware   and   Software Monitoring SUSIAccess ensures Advantech device stability by actively monitoring temperatures, fan speeds, voltages, hard disk states, and other hardware elements, as shown in Figure 2. Active alerts are sent out if any abnormalities are observed, which can trigger user-defined actions, like stopping or restarting processes.

Available out of the box, device- side software uses a SUSIAccess API to send device status data to SUSIAccess.

In addition to the hardware monitoring functions, SUSIAccess also performs software monitoring by continually checking program status. Real-time alerts are sent out if any abnormalities are observed. Active management of both hardware and software can prevent serious damage to devices, thus avoiding costly repairs and effectively reducing the cost of ownership.

3. User Friendly Map-view Interface Maintenance personnel can more easily locate and manage their devices using the map-view interface on SUSIAccess. In addition to the maps, building diagrams are provided to help pinpoint device locations in offices, factories, or wherever.

4.   Data Analytics The SUSIAccess Server software runs on a variety of cloud

Figure 3. UTX-3115 IoT Gateway

Figure 4. Key SUSIAcess* Functions

computing platforms, including Microsoft Azure and Amazon Web Services. These platforms typically include application support for data analytics, machine learning, video recognition, SCADA, business intelligence, and more.

5. Secure Interfaces The Server-Agent connection is based on the MQTT communication protocol, which offers secure and stable communications and decreases SUSIAccess integration time. The connection is also protected by OpenSSL.

6. Cost Savings[1] SUSIAccess Server software is provided free, and SUSIAcess Agent software is preloaded on all Advantech solutions. In addition, SUSIAccess will open the Agent source code and RESTful API document to non-Advantech platforms.

Customers can save up to 30 percent on deployment costs with worry-free compatibility and zero integrated software license fees. Maintenance costs can be reduced by up to 50 percent with the remote diagnosis and recovery capabilities. Real-time remote monitoring and proactive alarm notifications can bring down the time required for trouble shooting by as much as 70 percent.

Technology

This section describes the technology ingredients available to deploy a manufacturing solution like the one previously described.

IoT Devices Advantech is a global leader in remote I/O modules, offering complete, stand-alone data acquisition modules, which are broadly used in IoT or other industrial applications, such as facility monitoring, environment monitoring, and industrial process control. Advantech distributed remote I/O modules are categorized into two families, Ethernet I/O (ADAM-6000 series) and RS-485 I/O (ADAM-4000 series), which are subdivided into Analog I/O and Digital I/O modules. Advantech also offers a complete range of embedded automation computers with each series coming in three sizes – palm, small, and regular – all of them providing fanless, industrial-proven, application-ready control platforms.
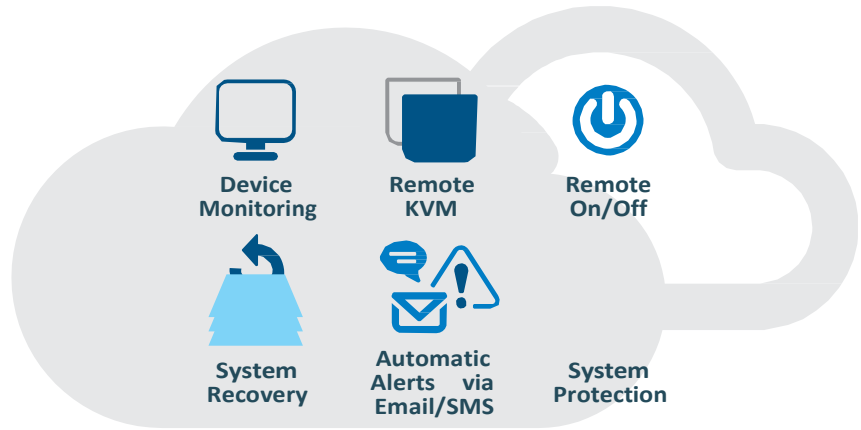
IoT Gateway
Pictured in Figure 3, the UTX-3115 is a member of the Advantech Embedded IoT Gateway series, designed for efficient, stable, and 24/7 operation. Equipped with a dual-core Intel® Atom™ processor E3826, the gateway is built with extremely reliable hardware and is easy to integrate with back-end maintenance and operating systems.

The UTX-3115 is based the Intel® IoT Gateway, which is a proven, application-ready platform with pre-validated, industry-leading software. Integrated and validated components provide maximum flexibility, and fast application development and field deployment. The Intel IoT Gateway is built on open architecture to ensure interoperability between systems, enable wide application development, and simplify services deployment.

The UTX-3115 IoT gateway includes Wind River* Intelligent Device Platform (IDP), which is a complete software development environment used for building IoT applications and devices that communicate with the cloud. It provides building blocks components to secure, manage, and connect IoT gateways to the cloud and is based on Wind River industry-leading operating systems, which are standards- compliant and fully tested. SUSIAcess*

SUSIAccess Server software delivers IoT Cloud capabilities that provide real-time hardware and software monitoring and maintenance with key features shown in Figure 4 and described in the following:

• System Backup and Recovery: Powered by Acronis* Backup and Recovery technology, this feature performs regular, automated backups with dynamic scheduling, hot backup without interrupting current tasks, and differential backup used to save precious storage space.

• Remote Monitoring: Administrators can monitor remote device status, including hard disk temperature, hard drive health, network connection, system/CPU temperature, system/ CPU fan speed, and system voltages.

• System Protection: McAfee Embedded Control security software maintains the integrity of the Advantech embedded systems by only allowing authorized code to run and only authorized changes to be made. It automatically creates a whitelist of the authorized code on the system. Once the whitelist is created and enabled, the system is locked down to the known good baseline, no program or code outside

the authorized set can run, and no unauthorized changes can be made.

• Remote Keyboard-Video-Mouse (KVM): Administrators can use their consoles to control and display the graphical user interface (GUI) of an IoT device on the factory loor using Keyboard-Video-Mouse (KVM) redirection. No additional hardware is required. Administrators can control a device as if they were sitting right in front of it. Remote KVM is a feature in Intel® Active Management Technology (Intel® AMT),2 which also enables administrators to diagnose and repair devices remotely, thereby significantly lowering support costs.

For instance, it is possible to remotely remediate and recover systems after an operating system or driver failure.

• Remote On/Of: Administrators can switch IoT devices on/of based on a preset schedule.

• Automatic Alerts by Email/SMS: SUSIAccess actively sends alerts so administrators can receive real-time notifications of IoT device status through email or smartphone.

IoT Tenets

The Advantech SUSIAccess remote management system is designed to provide security and interoperability from edge to control center or cloud in keeping with five key tenets defined by Intel:

• World-class security as the foundation

- The solution implements robust hardware and software-level protection that secures data between IoT-based factory devices and the cloud.

• Automated discovery and provisioning of edge devices to ease deployment

- SUSIAccess discovers and provisions Advantech devices on the factory floor.

• Data normalization through protocol abstraction to improve interoperability

- The Advantech IoT Gateway supports and abstracts a wide range of protocols, including MQTT, TR- 069, OMA, OSGi, Wi-Fi, and ZigBee*.

• Broad analytics infrastructure from edge to cloud to realize customer value

- The web-based Console-Server-

Agent structure of the Advantech solution enables users to aggregate and move data from factory loor to analytic applications.

• Infrastructure to monetize hardware, software, and data management from edge to cloud

- This cloud-based solution provides the tools needed to realize substantial improvements in manufacturing performance.

Summary

Bringing the power of IoT to factory automation, Advantech's SUSIAccess solution is able to help manufacturers improve the production line performance and lower operations costs by connecting factory devices to the cloud. The solution is made up of client-side agent software and server-side management software that enables seamless device interconnection and easy-to-use management interface. Using this tool set, customers can save time when resolving device maintenance issues and, most importantly, reduce the total cost of ownership (TCO) of factory equipment.

The solution features a streamlined interface designed to offer a smooth, intuitive experience, making it easier for administrators to get up to speed right away. As a result, equipment maintenance personnel will find it much easier to use big data analytics to improve manufacturing performance and remote device monitoring to reduce support costs. Advantech, working with Intel, is incorporating IoT technology to enable new opportunities on the factory floor.

Resources

Intel® Internet of Things Solutions Alliance Members of the Intel® Internet of Things Solutions Alliance provide the hardware, software, firmware, tools, and systems integration that developers need to take a leading role in IoT.
Intel® Gateway Solutions for the Internet of Things Development Kits
Intel Gateway Solutions for the Internet of Things development kits enable solution providers to quickly develop, prototype, and deploy intelligent gateways. Available for purchase from several vendors, the kits also maintain interoperability between new intelligent infrastructure and legacy systems, including sensors and data center servers.

M12 connectors become more reliable, easier to fit and reduce installer injuries

> Michael Meckl, Molex

The M8 and M12 sealed connector systems are the most common method of cable termination for sensors in harsh environment industrial and control applications. 2015 is the 30th anniversary of the introduction of the M12 interconnects, and was initially launched with 3 and 4-pin versions. Originally targeted at the automotive manufacturing market, the screw-type, dust proof, water tight connectors found favour in many other industries, including food and beverage, textile and machine building.

The need for increased productivity and Digital Industry 4.0 has increased the demand for higher data rates. Production lines and manufacturing systems are no longer stand-alone, but are digitally interconnected, "talking" to each other to deliver instantaneous decision critical data. Coding options for M8 and M12 connectors have expanded from the original A-code (analogue) used for sensors and actuators, to B-code (fieldbus) and now includes D-code (100 MB Ethernet Cat5) and high speed X-code (Gigabit Ethernet Cat6) types. This in turn has led to higher expectations for secure connections even under extremely harsh conditions. In addition to IP67 (Ingress Protection - dust tight and 1m water immersion), M12 connectors are also offered with IP65, IP68 and IP69K (high pressure and high temperature spray) ratings.

Compounding the challenge is the sheer number of connectors that are now being used. Their locations, often in very restricted places, can make installation difficult. Equipment upgrades to cope with the higher data rates can become very time consuming and complex. Molex, as a manufacturer of high-quality connectors, has set itself the task of simplifying and speeding up installation while improving communication integrity.

The traditional mainstream M12 connector utilises a screw thread that has three disadvantages. The hand applied torque during installation is a relatively uncontrolled process. Insufficient tightening can result in a poor connection, but too much will result in a compromise of the seal. Secondly, the time to fit a connector is quite long and thirdly is that of potential repetitive motion injury to the installer.

With its patented Brad® Ultra-Lock® connection system, Molex has brought to the market an entire portfolio of M12 connectors with Push-Pull functionality. This breakthrough thread-less design combines innovative engineering and advanced ergonomics, while still meeting the mechanical and electrical requirements of IEC Standard 61076-

2-101.

The connector is simply pushed into place and an automatic locking mechanism ensures a secure mate, even under the stress of machine vibration and accidental cable pulls. This quick and easy operation is highly repeatable, regardless of the worker completing the task. Labour savings of up to 75% are achieved compared to the traditional screw type. The loss of concentration and fatigue involved with such a monotonous, repetitive task is also reduced. This is especially the case when assembly needs to be done in confined spaces and in crowded device junction boxes. At first glance the connector head appears larger, but actually saves room as no additional space needs to be reserved laterally for hand or tool tightening of the screw thread.

An integrated radial seal replaces the commonly used axial type resulting in a guarantee that every connection, even without assembly aids, provides compliance to even the most rigorous IP69K standard.

Molex has also introduced the spark-free Brad Ultra-Lock (M12) EX Connection System, designed for industrial automation use in Class I, Division 2 and Zone 2 hazardous areas.

In cases where a machine possesses a high number of connections, where a worker has to screw/unscrew hundreds of connectors, the push on Ultra-Lock connection system dramatically reduces potential repetitive motion injuries. Globally this is a major concern. US based industry research estimates the cost of cumulative stress trauma exceeds $20 billion a year in worker's compensation. It cites manufacturing companies as one of the industries having high incident rates for occupational injuries. The National Institute for Occupational Safety and Health estimates that 20 million workers on assembly lines are at risk of developing injuries such as carpal tunnel syndrome. The National Safety Council reports that repeated trauma disorders have the highest incidence rates of all occupational illnesses, with manufacturing workers constituting 72% of these disorders.

In summary, the Molex Brad Ultra-Lock connector is quickly becoming the preferred solution for M12 connector systems:

• A repeatable fast, secure and sealed connection via the push-to-lock principle
• A 75% reduction in assembly times
• Reduced workload and injury risks to installers

From connectors which can be freely assembled, to over-moulded connectors, shielded connectors, distributors and distribution boxes - the Molex Brad Ultra-Lock spans the entire range of products needed for a machine's cabling solution.

Compression Seal / **Radial Seal**

Too loose — Moisture can enter
Too tight — Seal can be damaged
Just right — Optimal seal against moisture
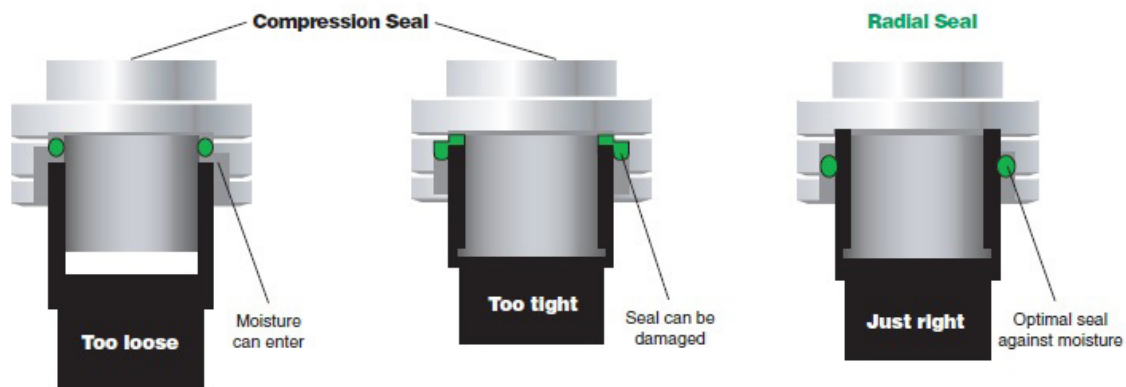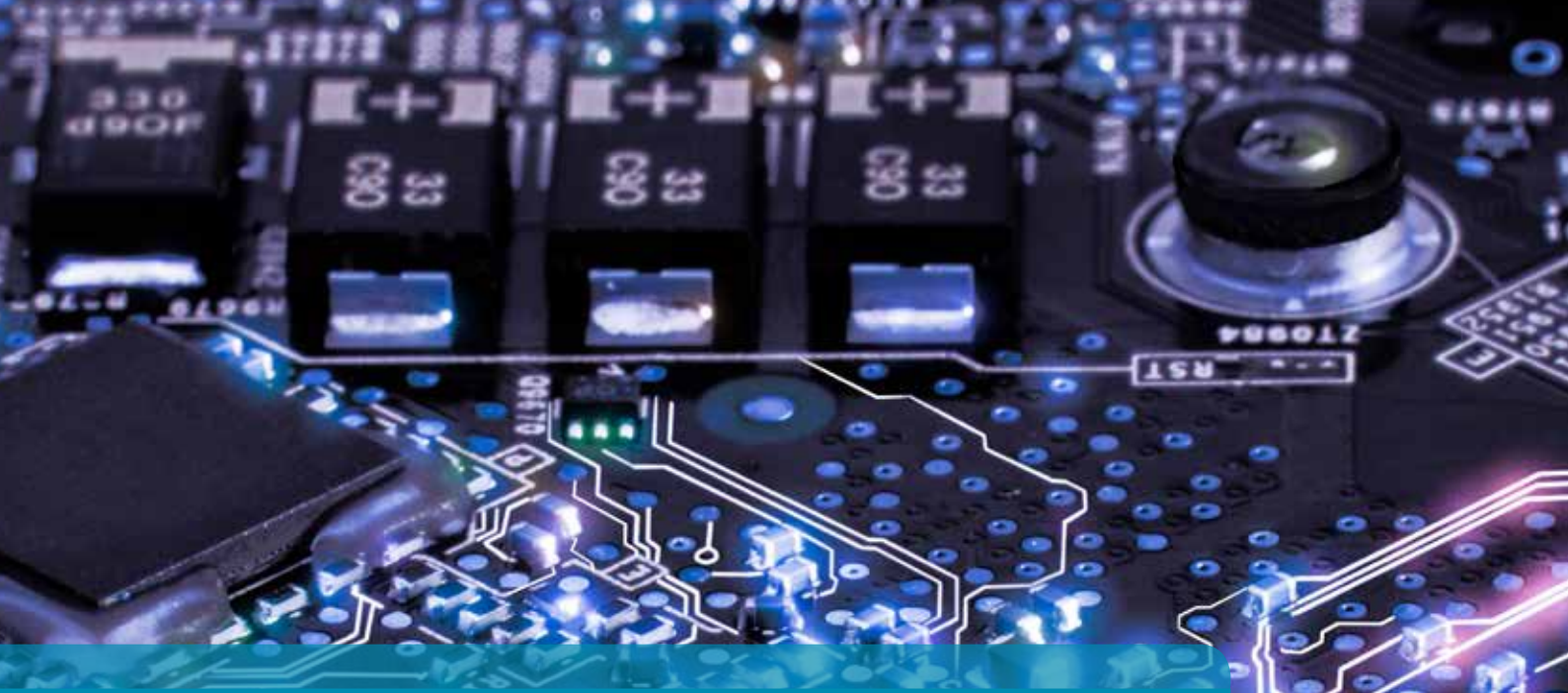
Design an optimized circuit for HART-enabled 4- to 20-mA inputs

› DERRICK HARTMANN & MICHAL BRYCHTA, ANALOG DEVICES

The advantages over traditional circuits include less board space and lower cost.

The highway addressable remote transducer (HART) protocol allows for bi-directional 1.2/2.2-kHz frequency shift keying (FSK) modulated digital communication over traditional analog 4- to 20-mA current loops. This allows for interrogation of the sensor/actuator, and provides significant advantages during equipment installation, monitoring and maintenance. HART provides benefits to maintenance crews using a portable secondary device to interrogate the sensor/actuator. But to fully realize all the benefits HART can bring, the sensor/actuator must be connected to a control system with HART enabled current inputs or outputs.

Let's focus on the HART FSK transmit circuitry. Figure 1 shows a traditional approach. Rsense converts the 4- to 20-mA signal to a 1- to 5-V signal to be read by an ADC. The HART FSK transmit circuitry AC couples ±500-mV HART FSK signals to the 4- to 20-mA loop via C1. These signals are either sinusoidal or trapezoidal waveforms.

A good buffer with enough drive strength is required at the HART modem's output as the Rsense represents a low impedance and there may also be significant capacitance on the current loop cabling. When the HART isn't transmitting, the buffer output would present a low impedance to the loop which could compromise the 4- to 20-mA signaling. For this reason the switch, SW1, is used in series with the buffer output to provide a high impedance when not transmitting.

The 4- to 20-mA loop can swing between 1 and 5 V while SW1 is open. As this change is AC coupled to SW1, the switch could see up to ±4 V at its input. Hence, a bi-polar supply of ±5 V or more would be required for the switch, or alternately an opto-switch could be used. A tri-state buffer is another option, though again this buffer would require bi-polar supplies. Another option is to use transformer isolation. Given the HART signal frequencies, an audio transformer would be required which is likely to be bulky and consume a large amount of board area.

Figure 2 shows an improved HART FSK transmit circuitry design, which reduces space and cost. In this circuit, the AD5700 HART modem has enough drive strength to drive the ±500 mV FSK signals directly onto the current loop without the need for an external buffer. When the modem isn't transmitting, the AD5700's FSK output is biased to 0.75V with a 70-kΩ impedance. R2, R3 provide a stronger 0.75-V bias, with AC impedance of R2||R3 = 1.7 kΩ. The high-pass filter formed by the this 1.7 kΩ and C1 ensures that the worst case 4- to 20-mA input signal, which is ±16 mA at 25 Hz across the 200-Ω Rsense, only results in the HART modems FSK output being drive to between 0 and 1.5 V. This means that the whole input
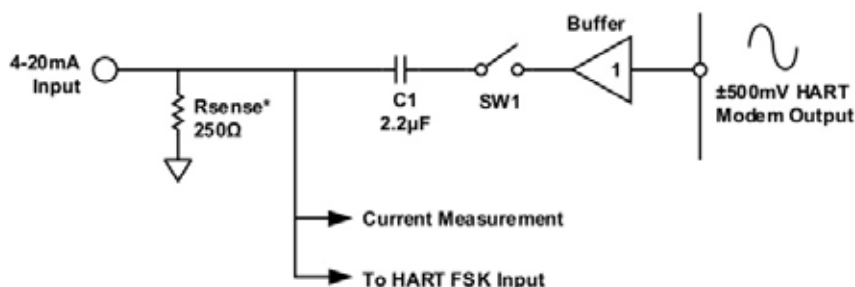
Figure 1: Traditional HART FSK transmit circuit.
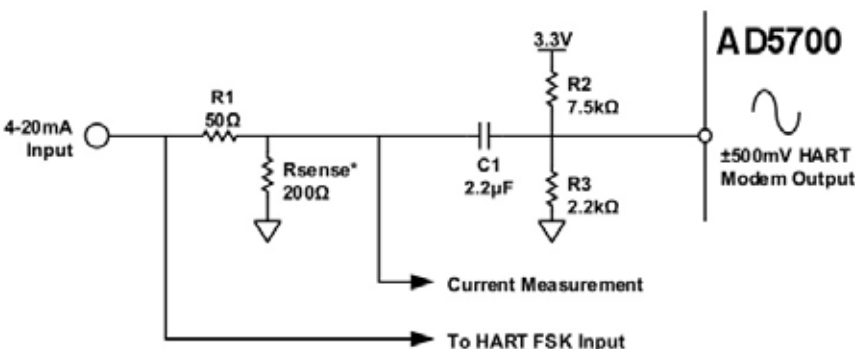
Figure 2: Improved HART FSK transmit circuitry.

Figure 3: HART FSK input.

can be run from unipolar supplies as low as 1.62 V (the minimum supply for the HART modem).
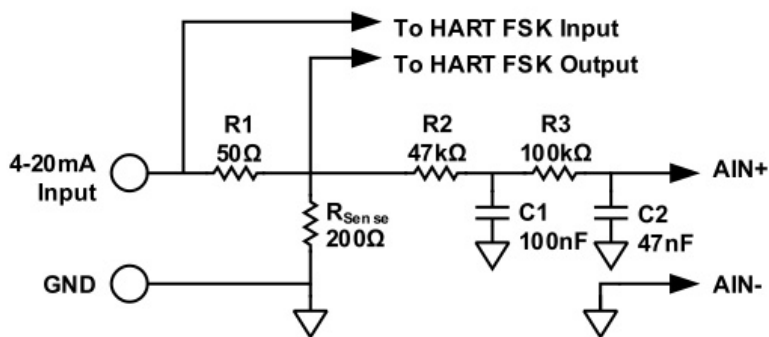
Another consideration is the input impedance, which should be greater than 230 Ω. The 250-Ω input resistor is split into 50 and 200 Ω to ensure a large enough input impedance. The AC input impedance is R1 + (Rsense || R2 || R3) ≈ 230 Ω. If needed, this impedance can be increased by raising the values of the 0.75 bias resistors, R2 and R3. The additional 50 Ω in the FSK transmit path will attenuate the FSK signals somewhat, but the voltages will still meet the HART spec requirements.

As the current loop is slewing, there will be some current flow through C1, R2, R3. Ensure that this won't significantly affect the 4- to 20-mA analog signal. Considering < 0.1% as an acceptable error contribution equates to seven time constants (τ). So $7\tau = 7*R*C = 7*(R2||R3)*C1 = 30$ ms. The 4- to 20-mA analog signaling is limited to 25 Hz, which corresponds to a 40-ms period. As this is longer than seven time constants, the additional current measurement error will always be < 0.1 percent.

This improved circuit (in Figure 2) has eliminated the need for a buffer and a switch, as well as the need for a bi-polar power supply. These three factors provide significant space and cost savings for a system over the traditional HART FSK transmit circuitry.

Circuitry for the HART FSK input is shown in Figure 3, where a bandpass filter rejects the low-frequency analog signaling and provides immunity from higher frequency interferers. The filter shown is specifically tailored for the AD5700 and will vary for different HART modems. One feature of this bandpass filter is the 150-kΩ input impedance provided by R1, which provides an inherent high level of protection from transient events.

Circuitry for the 4- to 20-mA current measurement is shown in Figure 4. The 200-Ω precision Rsense resistor converts the 4- to 20-mA signals to a 0.8- to 4-V signal to be converted by the ADC. This is followed by a double poll low-pass filter R2, C1, R3, C2 to reject the HART FSK signals.
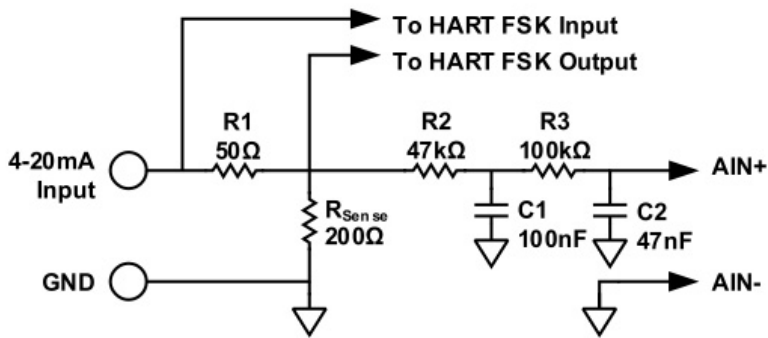
Figure 4: Current measurement circuitry.

This signal is then fed to an ADC for conversion.

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Michal Brychta is senior staff system applications engineer with focus on industrial automation. He also works for Analog Devices' Industrial Automation group, and is based in Limerick, Ireland. Michal holds Master's degree in electronic engineering from Technical University in Brno, Czech Republic.

Expanding Frequency Range in High-Power Splitter/Combiners by Minimizing Resistor Capacitance

> WeiPing Zheng and Brandon Kaplan, Mini-Circuits

Mini-Circuits' ZACS242-100W+ is a coaxial high-power, 2-way 0° splitter/combiner capable of handling up to 100W RF input power as a splitter. Its power handling capability makes this model a useful building block for signal distribution in high-power systems from 500 to 2400 MHz. However, at frequencies above 2400 MHz, the component's insertion loss performance degrades, hampering the splitter's usability in higher-frequency applications.

This article will present a design modification of ZACS242-100W, which achieves a 50% bandwidth increase by reducing signal loss due to the capacitance of the chip resistors in the circuit. The modification will be shown in a new model, ZACS362-100W+ which exhibits comparable power handling capability to that of its predecessor, but with low insertion loss up to 3600 MHz. The same technique has been used to expand the frequency range of other high-power splitter models in Mini-Circuits line to support high-power applications at higher frequencies.

Bandwidth Constraint: Power Handling vs. Resistor Capacitance

The power handling capability of a power splitter is essentially determined by the power handling of the internal resistors. The power handling of a resistor is proportional to its size; the higher the power, the larger the resistor. Therefore, the resistors used in a 100W splitter/combiner will be relatively large. This is important to consider in regard to the effect of resistor capacitance on insertion loss.

ZACS242-100W+ utilizes four 100W chip resistors configured in as shown in Figure 1. The conductive metallization the bottom of each resistor creates a capacitance to the PCB which can be expressed by the equation for the capacitance between two parallel plates:

$$C = \frac{\varepsilon_0 A}{d}$$

Where ε_0 = the permeability of the material between the two plates
A= the overlapping surface area of the plates, and
d= the distance between the plates
In other words, assuming constant ε_0 and constant d, the greater the area of conductive material on the bottom of the resistor overlapping the PCB, the greater the capacitance from the resistor. The capacitance of the resistors shown in Figure 1 adds to the overall insertion loss through the circuit, especially at higher frequencies, and this is primarily what constrains the bandwidth in ZACS242-

Figure 1: Board layout of ZACS242-100W+ with 4 100W chip resistors.

100W+.

Expanding Bandwidth by Minimizing Resistor Capacitance

To support high power requirements at higher frequencies, a design goal was set to extend the frequency range of ZACS242-100W+ while maintaining low insertion loss and comparable performance overall. One way to achieve this would be to reduce the capacitance from the resistors. We know that capacitance is a function of the overlapping area of conductive surfaces on the bottom of the resistor and on the PCB. Note that the resistors in Figure 1 sit face-down, with the entire conductive surface flat against the PCB. While we cannot reduce the size of the resistor or the area of the conductive surface itself, we can reorient the resistor to the PCB to minimize the overlapping area of the parallel plates.

The splitter/combiner was thus rebuilt with the resistors oriented 90° to the PCB as shown in Figure 2. Reorienting the resistors this way effectively reduces the resistor capacitance by more than 10 fold, which in turn significantly reduces the overall insertion loss at higher frequencies.

Test data for insertion loss swept over frequency verifies the improvement between ZACS242-100W+ in which the resistors are positioned flat against the PCB, and ZACS363-100W+ in which the resistors are positioned vertically, orthogonal to the PCB. Figure 3 shows a comparison of insertion loss versus frequency for the old and new designs.

While insertion loss for ZACS242-100W+ degrades above 2400 MHz, the modified design in ZACS362-100W+ achieves low insertion loss up to 3600 MHz, amounting to a 50% expansion in operating bandwidth. Both models provide 100W power handling as splitters, although whereas ZACS242-100W+ handles up to 40W RF power as a combiner, new model ZACS362-100W+ can handle up to 5W as a combiner. In all other respects, ZACS362-100W+ provides comparable performance to that of ZACS242-100W+ up to 3600 MHz with high isolation (22 dB typ.), and low phase and amplitude unbalance (1° and 0.15 dB, respectively).

Conclusion

The design technique presented in this article takes advantage of a basic principle of parallel plate capacitance to minimize the capacitance of resistors in a splitter/combiner circuit,
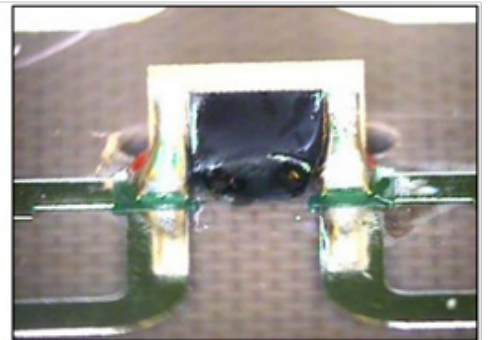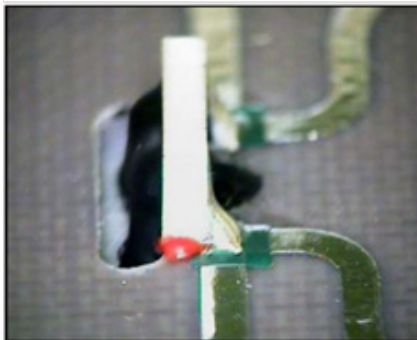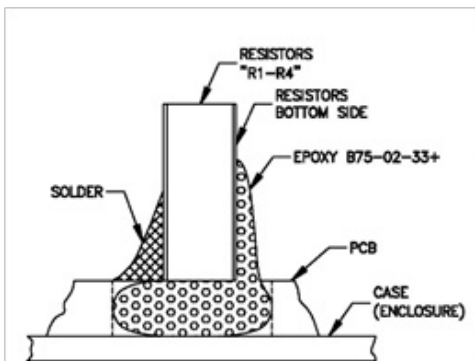
Figure 2: 100W Chip resistor oriented with conductive surface perpendicular to the PCB.

ZACS242-100W+
(Resistors Flat)
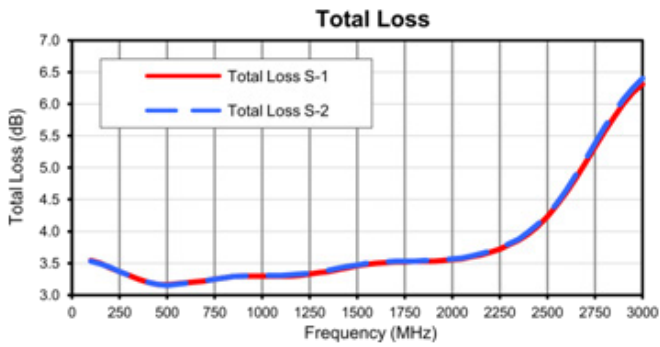
ZACS362-100W+
(Resistors Oriented Vertically)
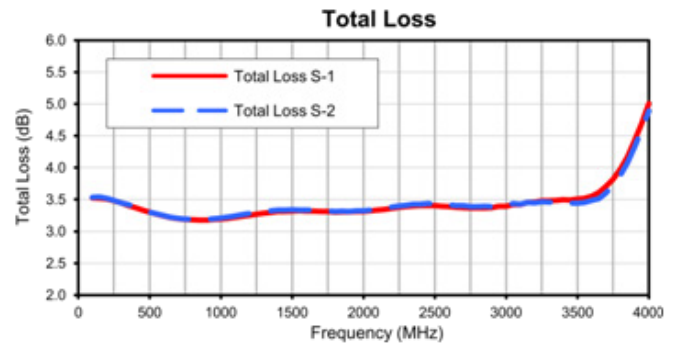
Figure 3: Comparison of insertion loss vs. frequency for old and new splitter/combiner designs. Orienting the resistors vertically to the PCB achieves a 50% increase in rated operating bandwidth.

thereby significantly improving insertion loss performance at higher frequency. The same technique has been used to expand the frequency of other high-power splitter/combiner designs in Mini-Circuits' line, and new designs are now in development to offer similar high-power capability up to 6 GHz.

ASICs allow cost-effective IP protection for technology inventions

> IC-LINK'S PHILL CHRISTIE

If you are a technology innovator, you'll want your efforts and inventions to be protected from copying. Patents are a first line of defense, but enforcing them though litigation may be expensive and time-consuming. A more preemptive approach is to implement your IP as a package that is all but impossible to copy, e.g. as a dedicated application specific integrated circuit (ASIC). Due to the long-term trend of price reductions for advanced (but not necessarily leading-edge) foundry technologies, it has become an attractive and cost-effective option for innovative SME's to design such an ASIC.

Patents are your first line of protection, but can you enforce them?

The origin of patents may be traced back in time to Queen Elizabeth I of England who granted monopoly privileges to businesses by means of letters patent, meaning public documents. These ultimately enabled investors to form business ventures to explore business opportunities in the New World.

Starting out as a royal permission for the exclusive commercialization of land, patents have since evolved to become legally enforceable rights that provide exclusive control over the production and sale of Intellectual Property (IP), otherwise known as inventions.

A company who implements an invention without the permission of the patent holder is said to have infringed the patent. But it is up to the owner of the patent to discover the infringement and initiate court proceedings. For some technology companies, especially startups and SME's, this may place an important burden on their efforts to bring their innovative products to market. For one, as an innovator, you often have financial constraints, especially because you investment costs – particularly R&D – are incurred before they have any prospect of revenues.

Your PCBs will be reverse engineered, fast

At some point, intellectual property in the technology domain has to be physically implemented and manufactured. This still often takes the form of a PCB (printed circuit board) comprised of a variety of mounted discrete components, which may include a power supply, Bluetooth functionality and a microcontroller.

The problem with this widely-used approach is illustrated by an internet search query for the phrase "PCB reverse engineering". This returns over 20,000 hits and clearly represents

Target Applications

- Intelligent edge access
- NFV solutions
- Wireless access point control
- Virtual CPE
- iNIC offload processing
- Industrial

Software Toolkit

Freescale has significant and increasing global investment in software for the embedded marketplace. The Freescale software development kit (SDK) delivers foundational technologies (user space, fast path, virtualization) that are continuously 'upstreamed' to support the networking portfolio. With 13+ years experience of commercial ARM software tooling, operating system development and delivery, Freescale continues to be a strong supporter of open source and industry software consortia, including Linaro and the Linux Foundation.

QorIQ LS1 Processor Family

QorIQ LS1088A and LS1048A Communications Processors

Overview

The QorIQ LS10x8A family of multicore communications processors combine up to eight ARM® Cortex®-A53 cores with the advanced, high-performance datapath and network peripheral interfaces required for wireless access points, networking infrastructure, intelligent edge access, including virtual customer premise equipment (vCPE), and high-performance industrial applications.

The QorIQ LS10x8A processors include Freescale's second generation datapath acceleration architecture (DPAA2). DPAA2 provides the infrastructure required to support simplified and secure networking interface and accelerator sharing by multiple general purpose CPU cores, while also providing a range of powerful acceleration engines to off-load software running on the CPUs.

The ARM® general purpose processors and DPAA2 are supported by a powerful software toolkit that provides a higher level of hardware abstraction and makes software development quick and simple. This combination balances ease-of-use with high-performance processing in a Linux® environment that is familiar to any software programmer. Customers can fully exploit the underlying hardware and easily adapt to network changes for real-time 'soft' control over the network.

QorIQ LS1088A Processor Block Diagram
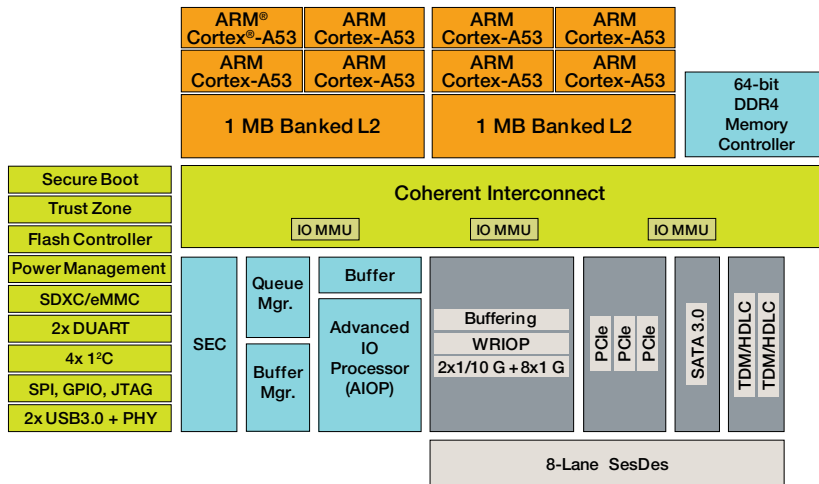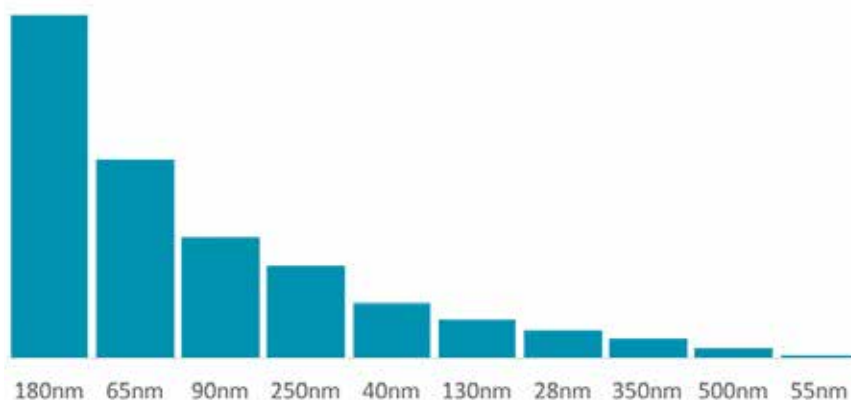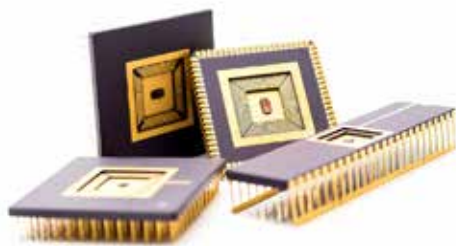
Number of ASIC projects as a function of technology node. Source imec IC-link database.

an established international industry. The copying process begins by stripping all the parts off the board to identify parts. The PCBs can then be delaminated into their individual layers and imaged in order to reconstruct a schematic diagram of the board. This reverse engineering industry also includes companies that offer to extract the code from your microcontrollers; so not even the firmware running on the boards is safe from cloning.

ASICs, at least modern ones, turn out to be your best safeguard

These issues have led technology companies to revert to ASICs (Application Specific Integrated Circuits) as a means of physically implementing and protecting their IP. But in older IC technologies, meaning those with one or two metal layers and 1um-2um critical dimensions, this still didn't prove secure. After package removal (also known as "depotting") all features could easily be seen using optical imaging equipment to take high resolution images. The cloning process could then proceed using similar methods as PCB cloning.

With more recent foundry fabrication technologies using critical dimensions of 180nm and less, this is much, much more difficult. This is not only due to the difficulties of imaging these sub-wavelength dimensions using optical,

wide-field microscopes, there are also many more metal interconnect layers, larger numbers of logics gates, plus analog blocks, Radio Frequency (RF) blocks, memory, MEMs, inductors and other devices integrated on-chip. All these factors combine to make ASIC cloning extremely time consuming and ultimately uneconomic for all but the biggest companies.

A typical example of a fast-innovating technology company is Belgium-based Van de Wiele, a global leader in advanced equipment and specialized services for the textile manufacturing industry. Van de Wiele has repeatedly suffered from reverse engineering of the boards used to control yarn systems. R&D manager Hans Desmet admits that "the first machine we released that used ASIC controllers was the first one that was not copied". The IoT offers a huge opportunity for nimble, fast-moving innovation

The accelerating trend of technology innovators to use ASICs for IP protection has been driven by the recent confluence of three key drivers. First, there has been an explosion

in applications for what has been loosely grouped under the heading of the Internet of Things (IoT). This has enabled companies with leaner decision making cycles and closer connections to the latest trends to move more rapidly to market than larger companies.

Second, while the volume of chips needed to address the IoT market is huge, the fragmentation of the market into a large number of potential IoT applications means that the production volumes of individual designs will be relatively small. This makes it difficult for large companies to compete on their ability to ramp large production volumes. In many ways large companies have outsourced innovation to technology SMEs.

Finally, and perhaps most importantly, one of the key characteristics of IoT applications is that they require advanced but not necessarily leading-edge silicon technology. This is primarily due to the fact that some form of wireless communication is required and the corresponding

analog circuit blocks to implement this functionality do not benefit very much from aggressive feature size scaling. The costs for implementing production prototypes with such foundry technologies are extremely low. Using imec IC-link's multi-project wafer (MPW) service, a company can produce a prototype run of a 25mm2 ASIC in the extremely popular 180nm technology with 45 samples for as little as $16,000.

Number of ASIC projects as a function of technology node. Source imec IC-link database.

Here comes substream innovation

The use of ASICs coupled with low-cost foundry technologies is giving rise to a new wave of technology-based innovation. But this would not be possible if the ASICs would not protect the IP. Together, accessible low-cost technologies and IP protection have enabled SMEs with great ideas to gain access to lucrative, high growth, global markets. We refer to this as substream innovation and like to think it would be easily recognizable to those earlier business adventurers looking for opportunities in the New World.

Phill Christie is a Principal Scientist and leads the Business & Technology Strategy Group at imec IC-link.

A Recipe for Embedded Systems

> ## Adam Taylor, e2v

Engineers never lose sight of the need to deliver projects that hit the quality, schedule and budget targets. You can apply the lessons learned by the community of embedded system developers over the years to ensure that your next embedded system project achieves those goals. Let's explore some important lessons that have led to best practices for embedded development.

THINK SYSTEMATICALLY

Systems engineering is a broad discipline covering development of everything from aircraft carriers and satellites, for example, to the embedded systems that enable their performance. We can apply a systems engineering approach to manage the embedded systems engineering life cycle from concept to end-of-life disposal. The first stage in a systems engineering approach is not, as one might think, to establish the system requirements, but to create a systems engineering management plan. This plan defines the engineering life cycle for the system and the design reviews that the development team will perform, along with expected inputs and outputs from those reviews. The plan sets a clear definition for the project management, engineering and customer communities as to the sequence of engineering events and the prerequisites at each stage. In short, it lays out the expectations and deliverables. With a clear understanding of the engineering life cycle, the next step of thinking systematically is to establish the requirements for the embedded system under development. A good requirement set will address three areas. Functional requirements define how the embedded system performs. Nonfunctional requirements define such aspects as regulatory compliance and reliability. Environmental requirements define such aspects as the operational temperature and shock and vibration requirements, along with the electrical environment (for example, EMI and EMC). Within a larger development effort, those requirements will be flowed down and traceable from a higher-level specification, such as a system or sub-system specification (Figure 1). If there is no higher-level specification, we must engage with stakeholders in the development to establish a clear set of stakeholder requirements and then use those to establish the embedded system requirements.

Generating a good requirement set requires that we put considerable thought into each requirement to ensure that it meets these standards:

1.   It is necessary. Our project cannot achieve success without the requirement.

2.   It is verifiable. We must ensure that the requirement can be implemented via inspection, test, analysis or demonstration.
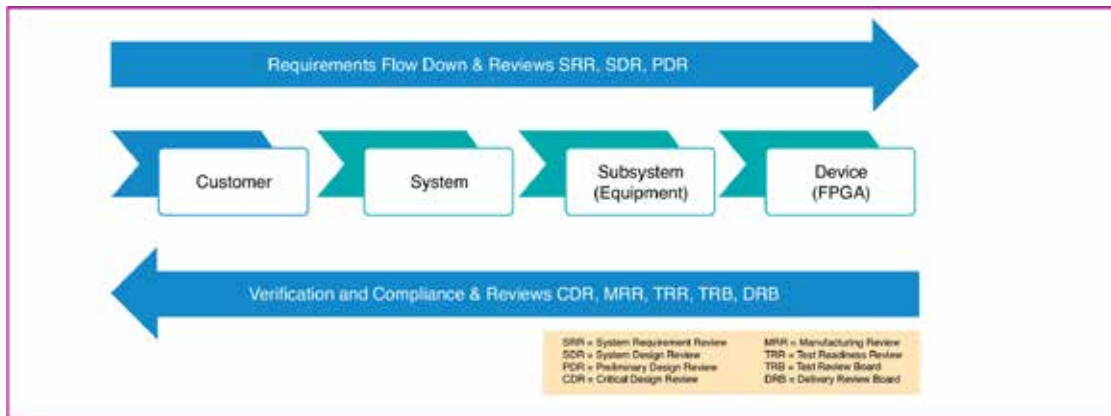
Figure 1 - Dynamic current dominates with higher operating voltage
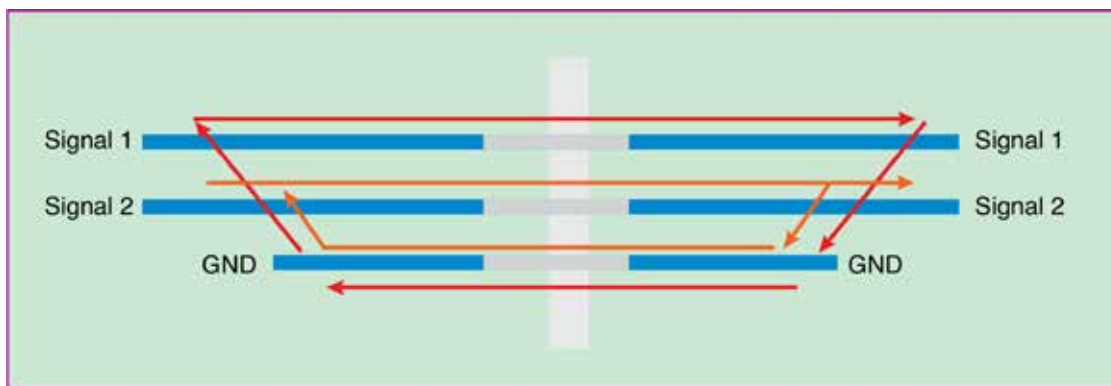
Figure 1 - Dynamic current dominates with higher operating voltage

3. It is achievable. The requirement is technically possible, given the constraints.

4. It is traceable. The requirement can be traced from lower-level requirements and can trace to higher-level requirements.

5. It is unique. This standard prevents contraction between requirements.

6. It is simple and clear. Each requirement specifies one function.

It is also common to use specific language when defining requirements to demonstrate intention. Typically, we use SHALL for a mandatory requirement and SHOULD for a nonmandatory requirement. Nonmandatory requirements let us express desired system attributes. After we have established our requirements baseline, best practice is to create a compliance matrix, stating compliance for each requirement. We can also start establishing our verification strategy by assigning a verification method for each requirement. These methods are generally Test, Analysis, Inspection, Demonstration and Read Across. Creating the requirements along with the compliance and verification matrices enables us to:
• Clearly understand the system behavior.
• Demonstrate the verification methods to both internal test teams and external customers. This identifies any difficult test methods early on in the development and allows us to determine the resources required. • Identify technical performance metrics. These spring from the compliance matrix and comprise requirements that are at risk of not achieving compliance.

ASSIGN ENGINEERING BUDGETS

Every engineering project encompasses a number of budgets, which we should allocate to solutions identified within the architecture. Budget allocation ensures that the project achieves the overall requirement and that the design lead for each module understands the module's allocation in order to create an
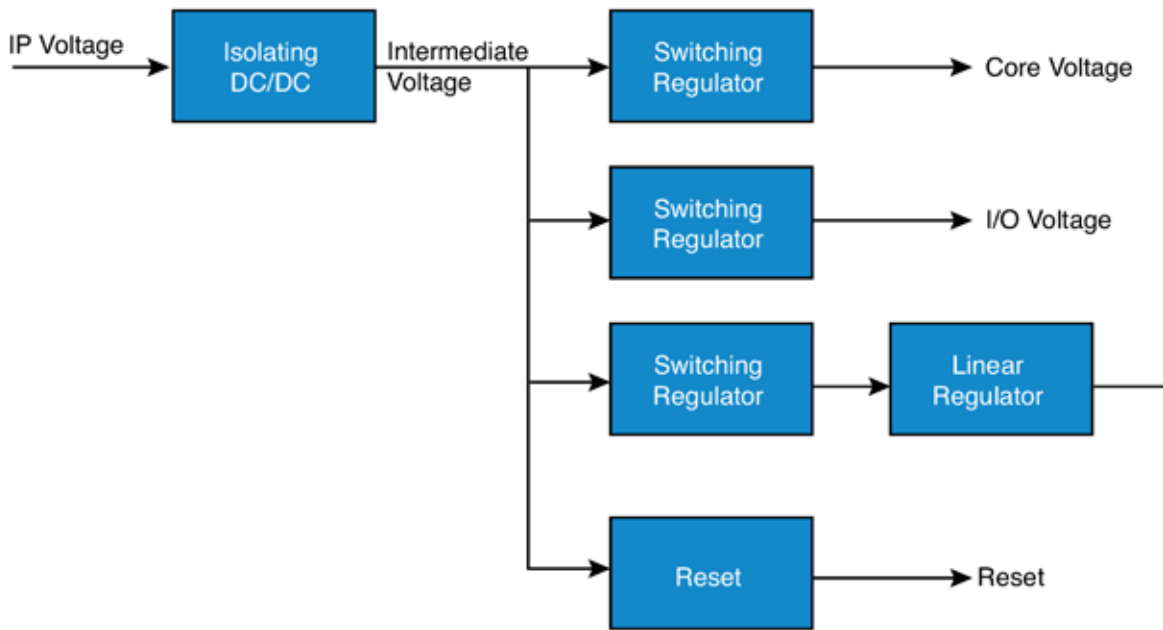
Figure 4 - Sub-threshold circuits are exponentially sensitive to temperature

appropriate solution. Typical areas for which we allocate budgets are the total mass for the function; the total power consumption for the function; reliability, defined as either mean time between failures or probability of success; and the allowable crosstalk between signal types within a design (generally a common set of rules applicable across a number of functions). One of the most important aspects of establishing the engineering budgets is to ensure that we have a sufficient contingency allocation. We must defeat the desire to pile contingency upon contingency, however, as this becomes a significant technical driver that will affect schedule and cost.

MANAGE TECHNICAL RISK

From the generation of the compliance matrix and the engineering budgets, we should be able to identify the technically challenging requirements. Each of these at-risk requirements

should have a clear mitigation plan that demonstrates how we will achieve the requirement. One of the best ways to demonstrate this is to use technology readiness levels (TRLs). There are nine TRL levels, describing the progression of the maturity of the design from its basic principles observed (TRL 1) to full function and field deployment (TRL 9). Assigning a TRL to each of the technologies used in our architecture, in conjunction with the compliance matrix, lets us determine where the technical risks reside. We can then effect a TRL development plan to ensure that as the project proceeds, the low TRL areas increase to the desired TRL. The plan could involve ensuring that we implement and test the correct functionality as the project progresses, or performing functional or environmental/dynamic testing during the project's progression.

CREATE THE ARCHITECTURES

Once we understand the required

behavior of the embedded system, we need to create an architecture for the solution. The architecture will comprise the requirements grouped into functional blocks. For instance, if the embedded system must process an analog input or output, then the architecture would contain an analog I/O block. Other blocks may be more obvious, such as power conditioning, clocks and reset generation. The architecture should not be limited to the hardware (electrical) solution, but should include the architecture of the FPGA/SoC and associated software. Of course, the key to modular design is good documentation of the interfaces to the module and the functional behavior. One key aspect of the architecture is to show how the system is to be created at a high level so that the engineering teams can easily understand how it will be implemented. This step is also key for supporting the system during its operational lifetime. When determining our architecture, we

need to consider a modular approach that not only allows reuse on the current project but also enables reuse in future projects. Modularity requires that we consider potential reuse from day one and that we document each module as a standalone unit. In the case of internal FPGA/SoC modules, a common interface standard such as the ARM® AMBA® Advanced Extensible Interface (AXI) facilitates reuse. An important benefit of modular design is the potential ability to use commercial off-the-shelf modules for some requirements. COTS modules let us develop systems faster, as we can focus our efforts on those aspects of the project that can best benefit from the added value of our expertise. The system power architecture is one area that can require considerable thought. Many embedded systems will require an isolating AC/DC or DC/DC converter to ensure that failure of the embedded system cannot propagate. Figure 2 provides an example of a power archi tecture. The output rails from this module will require subregulation to provide voltages for the processing core and conversion devices. We must take care to guard against significant degradation of switching losses and efficiency in these stages. As we decrease efficiency, we increase the system thermal dissipation, which can affect the unit reliability if not correctly addressed. We must also take care to understand the behavior of the linear regulators used and the requirements for further filtering on the power lines. This need arises as devices such as FPGAs and processors switch at far higher frequencies than a linear regulator's control loop can address. As the noise increases in frequency, the noise rejection of the linear regulator decreases, resulting in the need for additional filtering and decoupling. Failure to understand this relationship has caused issues in mixed-signal equipment. Another important consideration is the clock and reset architecture, especially if

there are several boards that require synchronization. At the architectural level, we must consider the clock distribution network: Are we fanning out a single oscillator across multiple boards or using multiple oscillators of the same frequency? To ensure the clock distribution is robust, we must consider:

• Oscillator startup time. We must ensure that the   reset is asserted throughout that period if required.

• Oscillator skew. If we are fanning out the oscillator across several boards, is timing critical? If so, we need to consider skew both on the circuit cards (introduced by the connectors) and skew introduced by the buffer devices themselves.

• Oscillator jitter. If we are developing a mixed-signal design, we need to ensure a low-jitter clock source because increases in jitter reduce the mixed-signal converter's signal-to-noise ratio. This is also the case when we use multigigabit serial links, as we require a low-jitter source to obtain a good bit error rate over the link.

We must also pay attention to the reset architecture, ensuring that we only apply the reset where it is actually required. SRAM-based FPGAs, for example, typically do not need a reset. If we are using an asynchronous assertion of the reset, we need to ensure that its removal cannot result in a metastability issue.

CLEARLY DEFINE INTERFACES

Formal documentation of both internal and external interfaces provides clear definition of the interfaces at the mechanical, physical and electrical levels, along with protocol and control flows. These formal documents are often called interface control documents (ICDs). Of course, it is best practice to use standard communication interfaces wherever possible. One of the most important areas of interface definition is the "connectorization" of the external interfaces. This process

takes into account the pinout of the required connector, the power rating of the connector pins and the number of mating cycles required, along with any requirements for shielding. As we consider connector types for our system, we should ensure that there cannot be inadvertent cross connection due to the use of the same connector type within the subsystem. We can avoid the possibility of cross connection by using different connector types or by employing different connector keying, if supported.

Connectorization is one of the first areas in which we begin to use aspects of the previously developed budgets. In particular, we can use the crosstalk budget to guide us in defining the pinout. The example in Figure 3 illustrates the importance of this process. Rearranging the pinout to place the ground reference voltage (GND) pin between Signal 1 and Signal 2 would reduce the mutual inductance and hence the crosstalk. The ICD must also define the grounding of the system, particularly when the project requires external EMC. In this case, we must take care not to radiate the noisy signal ground. Engineers and project managers have a number of strategies at their disposal to ensure they deliver embedded systems that meet the quality, cost and schedule requirements. When a project encounters difficulties, however, we can be assured that its past performance will be a good indicator of its future performance, without significant change on the project.

FURTHER READING

 1. Nuts and Bolts of Designing an FPGA into Your Hardware. Xcell Journal, 82, 42-49. 2. A Pain-Free Way to Bring Up Your Hardware Design. Xcell Journal, 85, 48-51. 3. Design Reliability: MTBF Is Just the Beginning. Xcell Journal, 88, 38-43.

Connector selection crucial for high performance industrial applications

> ## Harwin

T he industrial connector space has in the past sometimes been defined more by what it isn't – communications, computing, consumer, aero/space/defence, transportation etc - rather than what it is. However, this is changing, for a couple of reasons: firstly certain areas such as robotics and industrial automation with the advent of the Smart Factory (sometimes called Industry 4.0) are becoming 'bigger news'; and second because in some segments, - oil and gas, industrial vehicles, even medical which is sometimes included under 'industrial' - the increasing use of electronics systems has been a driver in connector development.

Industrial applications are often also termed 'hi-rel' - that is, any activity where the connector cannot fail - and usually involves applications in environments that are subject to harsh operating conditions, usually resulting from shock, vibration and temperature variation. Industrial sectors which require very high performance connectors include:

Robotics
Industrial & Factory Automation (Smart Factory/Industry 4.0)
Industrial vehicles (off-road)
Oil & Gas
Marine & Undersea
Scientific Equipment
Test & Measurement
Metering

There is significant growth in all the above sub-sectors. This is due to a number of factors including the increased use of electronic systems that are being used for monitoring and control, and also the emergence of sophisticated robotics and metering systems. Quite simple, electronic systems are all-pervasive and almost every piece of equipment used today relies on them. This in turn means that the components used must be rugged and reliable.

Influencing factors

Connectors used in the industrial market share many similar drivers with other markets – size, weight, cost are always important – but industrial applications also tend to put more stress on all types electronic components that are used, and this is especially true of connectors. This is because as well as having an electrical function (carrying the power or signal) they also often make a physical connection. Often, too, they must be capable of being mated and unmated many times. This is why, for so long, some industrial users refused to specify surface mount connectors. Even today, hi-rel connector maker Harwin offers through hole and surface mount variations of its Datamate, Gecko and M300 Hi-Rel connector families, and also includes different locking mechanisms for extra security.

Size; Weight; Signal Density

Looking more closely at the evolving connector requirement we can identify three common factors: size, weight

and signal density – all markets want 'smaller, lighter'. The industrial market has responded and connector pitches have shrunk down to 2 and 1.25 mm. A good example of this is Harwin's 1.25mm pitch Gecko family. Another way of maximising space utilisation is to combine the functionality of connectors, for example by combining signal and power, and sometimes coax and even opto in the same package. Mix-Tek Datamate from Harwin is an example of a connector family that can mix signal (to 3A), power (to 40A) and coax (to 6GHz) in a variety of configurations all within one common, lightweight, space-saving modular body shell.

Of course, as sizes reduce and densities increase, there is the issue of EMI and crosstalk. This is a system wide issue so connector design is a significant issue.

Cost

In the past, industrial applications, especially on the factory floor, often relied on connectors developed for military and defence applications, where cost was a (sometimes distant) secondary concern. For industrial users, as connector usage proliferates to service the exponential requirement for localised yet widespread sensing and monitoring required by factory automation programs such as Smart Factory or Industry 4.0, cost is very much an issue. (And even military programs are subject to stringent cost analysis due to budget cuts!) So alternatives had to be found. Harwin's hi-rel product range – chiefly comprising the Datamate, Gecko and M300 families – offer high performance, surviving extremes of shock, vibration and temperature, yet are much lower cost than military products.

For lower cost industrial applications that still require high quality and small size, Harwin's Archer 1.27mm pitch connector M50/M52 range is several percentage points more cost-effective than other manufacturers' products.

High-performance

The interconnect system chosen must be suitable for the application. Therefore, while it may be tempting to go for an ultra-small, cheap device developed perhaps for use in consumer goods, such devices are not suitable for most industrial applications as they are not rugged enough to survive extremes of shock, vibration and temperature; neither are they designed for repeated mating and demating cycles. Operating conditions must be considered very carefully before a connector is specified.

If we combine all these factors, ideally industrial connectors need to be small, lightweight, cost-effective and high-performance. To achieve such a challenging order, special contact technology – the heart of any hi-rel connector - has been developed. In Harwin's case, we use special beryllium copper clip contacts which ensure that signal integrity is maintained even in harsh environments. Body material is important too: plastics used must be highly robust but also may be required to be fire-resistant, exhibit no outgassing and of course be RoHS-compliant, made environmentally friendly materials, ideally eliminating harmful chemicals even before they are added to restricted substances lists for system future-proofing.

A recent example which illustrates this combination of factors is Harwin's M300 high density power connectors that can handle currents up to 10A. Based on a 3mm pitch, the connectors are designed for rugged environments and withstand twice the number of operations as older generation products. M300 connectors feature a 4-fingered Beryllium Copper female contact which delivers excellent electrical and mechanical performance. Devices suit 18 to 22AWG applications and are designed for use in temperatures of between -65 and +175degC and are rated for 1000 operations. They pass shock (EIA-364-27: 100g 6ms No Discontinuity >1μs and vibration (EIA-364-28 10g No Discontinuity >1μs)

testing. Jackscrews are available for extra security.

Design Flexibility

Design engineers are very creative people, possibly because they are continuously being pushed to deliver more functionality, whilst – as we have mentioned before – reducing size and cost. Therefore it is important that connector manufacturers respond with solutions that are flexible. One example from Harwin is the introduction of a horizontal mounting style for its 1.25mm pitch, hi-rel Gecko product family. G125 series connectors offer high performance in a miniature package. The 1.25mm pin spacing results in a 35% space saving over other high-performance connectors such as Micro-D. Connectors can handle 2A per contact and function within a wide temperature range (-65 to +150degC) and under extreme vibration (Z axis 100g 6m/s). Other features common to the Gecko connector family include polarization points that prevent mis-mating, easy identification of the No 1 position for fast visual inspection and optional latches that allow simple and fast de-latching. Optional special tooling is available for use in confined applications. The horizontal style connectors feature a new mechanical hold-down latching system for additional connection security.

The new horizontal versions reduce stacking height of PCBs to just 5.6mm. Available in the standard eight positions - 6, 10, 12, 16, 20, 26, 34 and 50 – the new style also facilitates mother & daughter board configurations.

Above all, when determining which interconnect system to employ, always consider the application and the demands that the environment and usage pattern will place on the connectors. Over-specing a connector may cause financial problems, underspecing it most certainly will!

Intelligent Gateways Make a Factory Smarter

> ## Armando Astarloa, System-on-Chip engineering S.L

An intelligent gateway powered by the Zynq SoC enhances productivity in a state-of-the-art manufacturing plant.

The Industrial Internet of Things-the idea that all systems should be connected on a global scale in order to share information-is quickly becoming a reality. Today, a growing number of companies, especially in the industrial equipment markets, are taking IIoT one step further by creating complex systems that integrate sensors, processing and communications to form intelligent factories, smart energy grids and even smart cities. These developments increase productivity and profitability, as well as enrich lives. New technology implemented on a Xilinx® Zynq®-7000 All Programmable SoC is helping to bring intelligent systems into the manufacturing sector of the IIoT. The smart gateway, designed by System-

on-Chip engineering S.L. (SoC-e), streamlines productivity and helps companies like Microdeco become more reliably connected and secure. To maximize profitability, factories seek more flexibility in their layouts, more information about the process and manufactured products, more intelligence in the processing of this data and an effective integration of the human experience/interaction. However, as new technology is introduced into the factory sector, those creating it need to respect some rules. The first and most important is that production cannot stop. New technologies must be compatible with old systems and interoperability among vendors should be facilitated. Furthermore, the solutions should provide a means of taking the next step in automation, leading to more autonomous or decentralized analytics.

In order to achieve what many are calling the "fourth industrial revolution," factories need infrastructure and systems to use the IT and electronics for automated production. Although many factories automated in the third industrialization wave, in many scenarios it is necessary to implement both steps simultaneously: the third and fourth evolutions of automation. This situation offers a good opportunity to integrate IT infrastructures that will fit with new requirements for smart factories but are compatible with the third era production-scheduling and automation systems. Figure 1 depicts the typical production system widely used in industry that helps adapt and optimize production to demand. The enterprise resource-planning (ERP) software consists of tools that support the commercial database. It defines what to fabricate. Meanwhile,
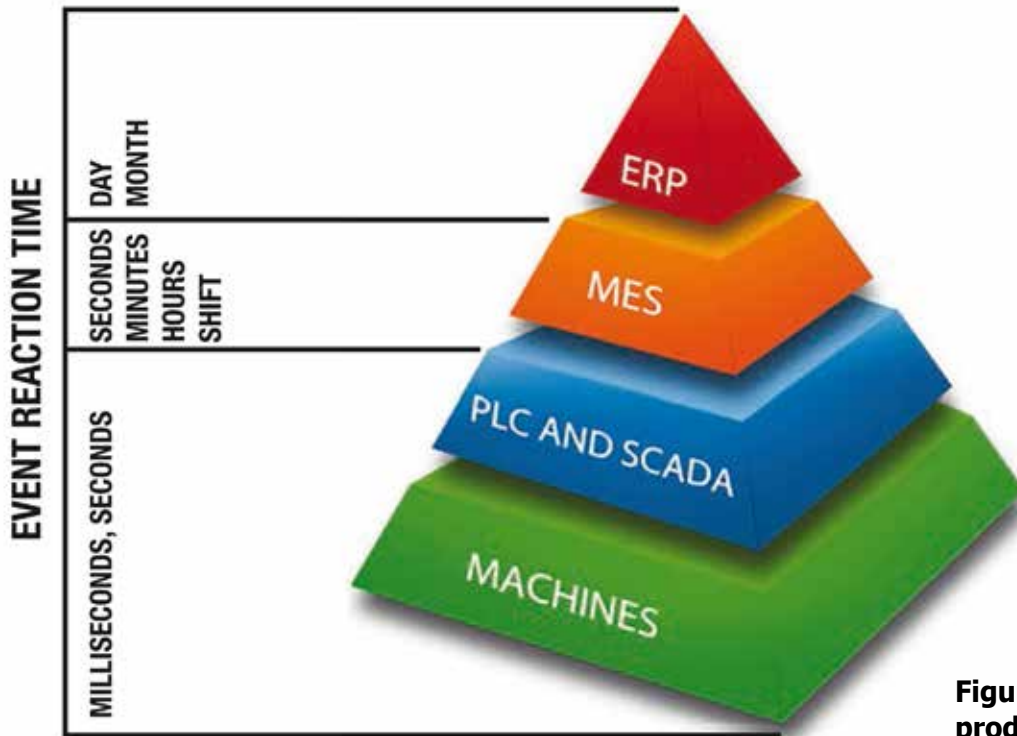
Figure 1 – Scheduling the production via ERP/MES

the manufacturing enterprise system (MES) focuses on the scheduling of production. It uses the ERP outputs, communicates with the production plant equipment and tells the equipment what to do.

NETWORKING, PROCESSING AND SENSING IN THE SMART FACTORY

With many companies offering different types of factory equipment and many generations of that equipment coexisting, connecting equipment from different vendors and different time periods that conforms to different standards can be quite challenging. It's further complicated by the fact that this factory equipment must also communicate with a company's IT network (enterprise and/or Internet); combinations of PCbased systems; gateways, black boxes and industrial switches built around multiple protocols. As such,

a factory can quickly turn into a heterogeneous nightmare, lacking the simplicity and flexibility that a "plug-and-work" operation demands. Intelligent gateways like the CPPS-Gate40 from SoC-e (Figure 2) will play a vital role in offering secure and transparent operation between both worlds (machine and IT). Microdeco is a company that manufactures small metal parts for the automotive sector. The company is always looking for ways to enhance productivity and is at the forefront of using intelligent systems. In the company's pilot plant, located in Ermua, Spain, Microdeco has built a networking infrastruc ture around the concept of smart gateways that combine in the same system networking, processing and sensing. One of the top challenges in creating a smart factory lies in connecting the various systems. The factory includes high-speed optical links that interconnect the various cyber physical production system

(CPPS) areas-that is, each production group of machines, sensors and actuators. The intelligent gateway is in charge of all the communication infrastructure. This includes, the highspeed switching for the fiber links and flexible, trispeed Ethernet ports to implement regular Ethernet or Industrial Ethernet protocols in each cell, along with serial ports to implement widely

used industrial protocols such as Modbus and Profibus. Figure 3 shows how each smart gateway installed in each machine (CPPS area) is tied to the next one using a single fiber-optic link. The infrastructure is completed by connecting all the devices in a single ring that implements the High-Availability Seamless Redundancy (HSR) protocol. This nonproprietary (IEC 62439-3 Clause 5) Ethernet "zero-delay recovery time" solution allows operators to disconnect any equipment from the ring without adversely affecting other nodes or

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ZVE-3W-183+	5900-18000	35	2	3	1295
ZHL-4W-422+	500-4200	25	3	4	1160
ZHL-5W-422+	500-4200	25	3	5	1670
ZHL-5W-2G+	800-2000	45	5	5	995
ZHL-10W-2G+	800-2000	43	10	12	1295
• ZHL-16W-43+	1800-4000	45	12	16	1595
• ZHL-20W-13+	20-1000	50	13	20	1395
• ZHL-20W-13SW+	20-1000	50	13	20	1445
LZY-22+	0.1-200	43	16	30	1495
ZHL-30W-262+	2300-2550	50	20	32	1995
ZHL-30W-252+	700-2500	50	25	40	2995
LZY-2+	500-1000	47	32	38	2195
LZY-1+	20-512	42	50	50	1995
• ZHL-50W-52+	50-500	50	63	63	1395
• ZHL-100W-52+	50-500	50	63	79	1995
• ZHL-100W-GAN+	20-500	42	79	100	2395
ZHL-100W-13+	800-1000	50	79	100	2195
ZHL-100W-352+	3000-3500	50	100	100	3595
ZHL-100W-43+	3500-4000	50	100	100	3595

Listed performance data typical, see minicircuits.com for more details.
• _Protected under U.S. Patent 7,348,854_
* _Price Includes Heatsink_

Mini-Circuits®

Figure 2 – The CPPS-Gate40 smart gateway from SoC-e

equipment in the factory. This real plug-and-work operation facilitates plant layout modifications. Furthermore, HSR supports the redundant IEEE 1588v2 submicrosecond synchronization protocol, which simplifies the synchronization of the system to perform precise reconstruction of the sampled sensor data or the implementation of control tasks. In order to provide seamless redundancy, each HSR node sends the Ethernet frames through both directions of the ring. This approach allows "hot" cable or equipment plugging and unplugging. Each node is in charge of forwarding both frames, and the IEEE 1588v2 support corrects the residence and link delay times to ensure timing accuracy in the entire network. Thus, frame hardware processing is mandatory to ensure low and constant latency times in every node. Indeed, the IEC standard recom

mends a "cut-through" approach for forwarding the frames in the ring. To avoid circulating frames, for unicast communications the node that receives the frames is in charge of removing them from the ring. For multicast and broadcast traffic, the sender removes the frames when it sees them again in the redundant port. Additional rules regarding circulating frames (such as corrupted frames) are applied to ensure network stability.

HSR, combined in many cases with the Parallel Redundancy Protocol (PRP), is the recommended High-Availability Ethernet protocol in the standard for the automation of one of the most critical sectors worldwide: power sub stations. Other sectors, such as military and aerospace, are also adopting these Layer 2 solutions. Smart gateways provide hardware switching from the Ethernet and serial ports to the HSR infrastructure ring. There are two smart gateways, represented in the left and in the right of Figure 3, that connect the HSR ring with the Ethernet-based enterprise network working as a redundancy box (RedBox). Functionally, the access point represented on the right is optional, as it can be used to avoid the single point of failure that would appear in the case of a network using only one RedBox. We recommend implementing the dual-box setup in cases where high availability is needed, or when it is necessary to manage PRP frames (IEC 62439-3 Clause 5) in the critical nodes in the enterprise network. Additionally, there are internal networking ports in the gateway to the processing elements of the SoC device. In most cases, a "dumb" switching approach is useless to join plant and IT worlds. The heterogeneity in the data and network formats makes straightforward connections difficult.

What's needed is a powerful integrated processing system able to talk with local, enterprise or cloud databases. In addition, such a system would be in charge of translating protocols, managing HMI systems, supporting MES systems and even running soft PLCs for real-time control. But that is not all. The customer also expects such a system to perform complex sensor data preprocessing and filtering in the equipment, and of course, advanced cybersecurity operations.

The cybersecurity requirements in these kinds of advanced manufacturing facilities vary widely. Advanced security is necessary to protect the status of the production itself, avoiding any malicious or accidental interruption generated by any cyber infrastructure (device, network, software or hardware). It is also necessary to authenticate users and devices that are accessing information or any critical operation. Furthermore, this information and the control protocols need to be protected in terms of authentication and privacy, because factory networks are connected to larger IT networks in an enterprise and outside of it. These challenges can only be addressed with a layered cybersecurity approach that takes into account each plant implementation. A common element in all the projects is the need to support secure boot and storage with encryption and authentication. This feature will make credible the implementation of secure software and secure net

works. The trusted embedded system is more and more difficult to protect due to the increasing number of devices and their heterogeneity. For authentication and for networking security, these systems can directly
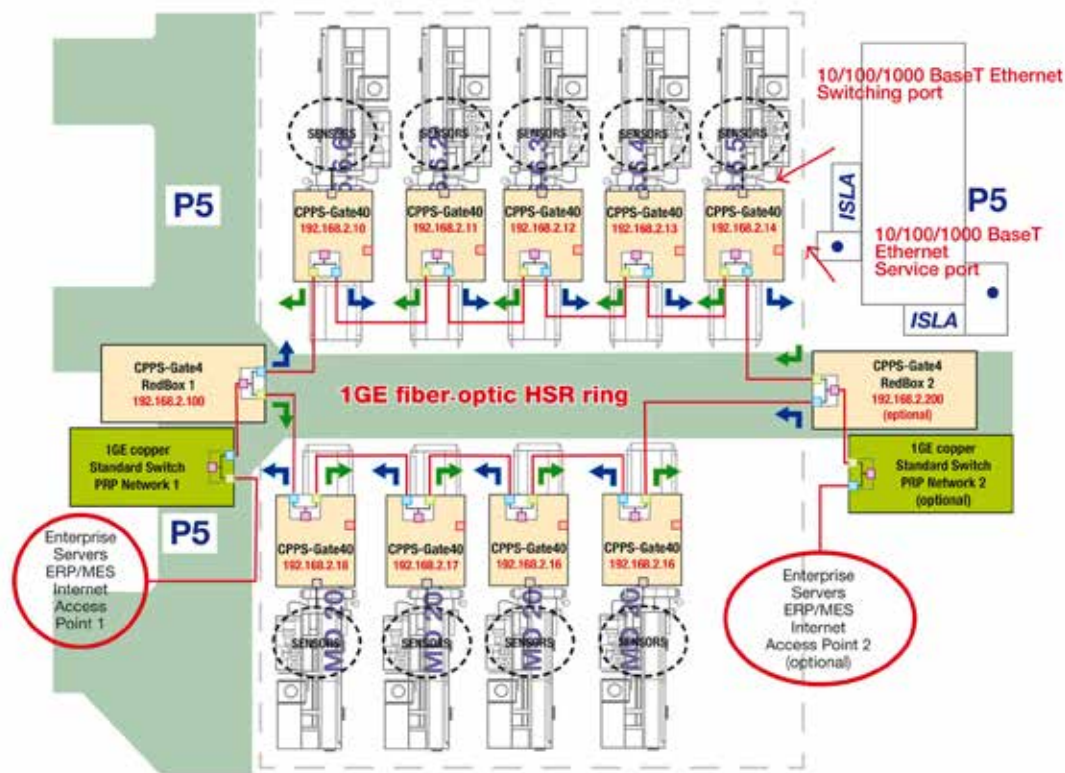
Figure 3 – Lathes section in the Microdeco factory

use many of the solutions present in the IT world today. Well-known authentication mechanisms like IEEE 802.1X combined with RADIUS are a good example. Many embedded systems with high-level operating systems can run cryptographic libraries (such as OpenSSL) to support all the secure Layer 3 protocols and applications useful for secure data interchange. However, a big challenge arises when it is necessary to secure Layer 2 industrial protocols with strict real-time requirements. The analysis of these scenarios shows that the software approach of protecting these frames by applying cryptographic algorithms, even using crypto accelerators, is not straightforward, and in many cases custom hardware processing is required.

In the presented topology, from the network and user point of view, it is necessary to secure three network links—the redundant HSR/PRP, the 10/100/1G switching port and the service ports—with authentication mechanisms. Furthermore, due to all the plant traffic passing through the intelligent gateway, the three links will play a vital role in monitoring traffic for potential threats. A final concept is the integration of a sensor interface suite. As discussed, the advances in the technology should help us to simplify the installations, not make them more complex. To fulfill this demand, we integrated all the standard digital and analog interfaces in the gateway. Additionally, we also included high-end interfaces for advanced vibration sensors and high-speed data acquisition interfaces with direct access to the Zynq SoC device.

HOW SOC PROGRAMMABLE PLATFORMS DRIVE THE CHANGE

The "magic" of merging high-end networking, powerful processing and sensing capabilities has been obtained thanks to SoC programmable platforms. Our product, named CPPSGate40, embeds a Xilinx Zynq-7000 All Programmable SoC device implemented on the SoC-e SMARTzynq OEM module. The dual-core ARM® Cortex™-A9 MPCore™ on the device is complemented with different memory resources (DDR3, flash, massive storage units, etc.) and hardware to support multiple high-speed networking links. This infrastructure offers a huge level of freedom to partition hardware and software processing in order to face the
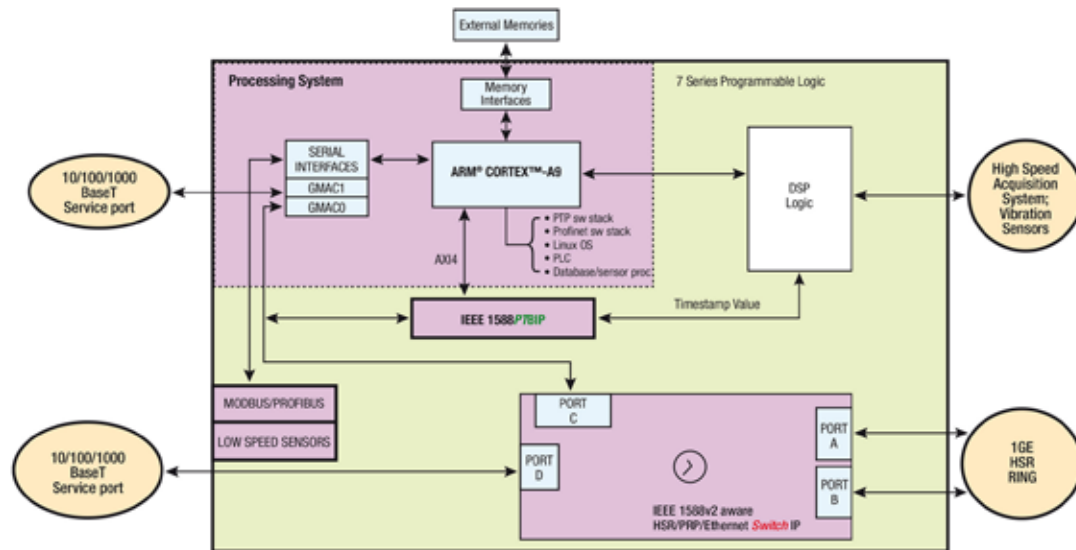
Figure 4 – Block diagram of Zynq SoC implementation
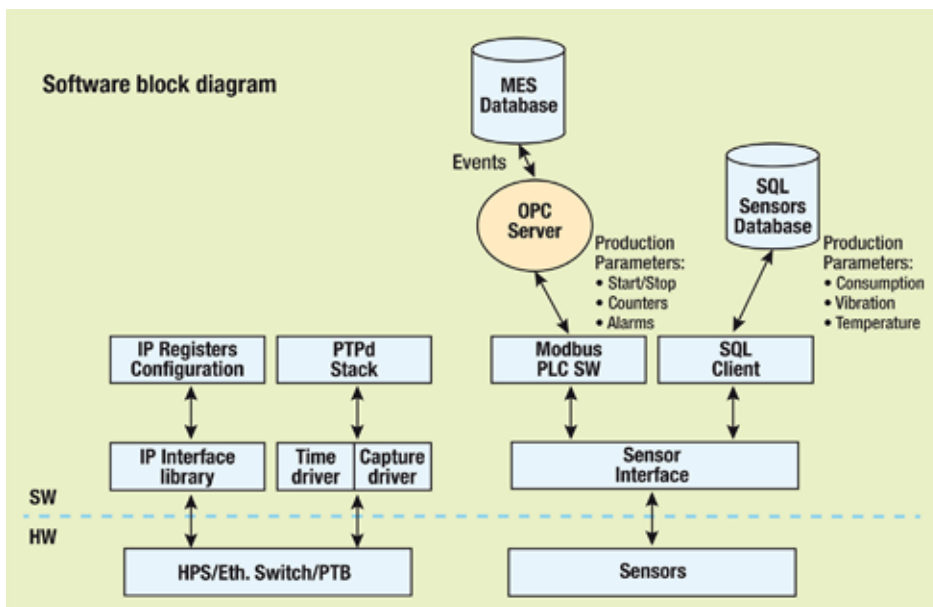
Figure 5 – Software infrastructure for the smart-factory network

challenges these applications present. From the hardware perspective, the Zynq SoC's programmable logic is the perfect candidate to implement the low-latency networking tasks combined with the IEEE 1588v2 hardware support units. Figure 4 is a block diagram of the SoC implementation for the CPPSGate40 in the Microdeco implementation. The network's switching infrastructure is coordinated by the SoC-e HSR/ PRP/ Ethernet switch (HPS) IP core, which ensures a constant forwarding time of 550 nanoseconds in each node of the ring and integrates internal and external trispeed Ethernet ports. The internal port is sniffed and time-stamped by the Precise Time Basic (PTB) IP core, providing support for the PTP stack. This IEEE 1588v2 infrastructure allows the smart gateway to work as master, slave, transparent clock and boundary clock. Thus, at the end, in each piece of equipment a synchronized 64-bit timer can be used for time-stamping, synchronization, control and as a common time reference to implement Time-Sensitive Networking (TSN) networks. These networking cores implemented on the FPGA section of the Zynq SoC are also ready to support cybersecurity features such as IEEE 802.1X authentication. This mechanism, combined with an external authentication server, protects nonauthorized connections to the network ports. The Zynq SoC's programmable logic also plays a vital role in securing Layer

2 control-related frames on the fly, like the authentication needed in the IEEE 1588v2 transparent clock operation. The cybersecurity is further enhanced by the Zynq SoC's secure boot. All the external software and bitstreams external from the device, even the bootloader and OS, are stored, AES-256 encrypted and HMAC authenticated. This feature, combined with other hardware security protections included in the device, ensures that data throughout the cyber infrastructure comes from trusted origins. Additionally, a SIEM agent installed in each CPPS-Gate40 runs (among others) the following security-related tasks: surveilance of new connections, authentication attempts, SSH connections and access to analytics tools; virus/malware detection; network attacks identification; and ARP traffic analysis. The sensor interfaces are also implemented on the programmable logic section (high-speed data acquisition, digital filtering and FFT) and via some of the standard communication channels present on the Zynq SoC's processing system (UART, I2C, SPI). The software infrastructure implemented on this equipment benefits from the seamless integration of Linux OS Ubuntu's distribution on the device. The list of features that Linux supports is extensive. For Microdeco's specific implementation, Figure 5 summarizes the most relevant software services implemented on top of the Linux OS. A Python-based PLC emulator has been developed as the key piece to map sensor interfaces in a well-known Modbus TCP scheme. This approach simplifies the communication with the third-party MES

software. In parallel, a SQL client transfers raw and preprocessed sensor data packets to a remote SQL server. Specific alarms and selected data are directly published in a cloud-based couchDB database. The data analysis can be performed remotely in the enterprise or cloud server and even locally on the smart gateway. For this last purpose, the product includes a temporal database that can predict failures or other defined behaviors in the production and act locally. Big-data analysis software provided by Juxt.io is in charge of performing the predictive analytics related to machine behavior. Network management is supported via SNMP thanks to SoC-e's Portable Tools API. The cybersecurity infrastructure is built around the hardware support of SoC-e IP and the integrated SIEM agent for network and user activity surveillance.

INCREASING PROFITS THROUGH TECHNOLOGY

Germany's Fraunhofer Institute for Industrial Engineering and Automation forecasts that Industry 4.0 may lead to a leap in productivity of 20 to 30 percent by 2025. However, the industrial sector needs progressive changes and friendly technologies and solutions. The Microdeco plant, for example, benefits from high-end technologies to integrate flexible and computationally powerful networking and processing infrastructures in its production lines. The drivers of this approach are the adoption of open standards for networking and for the data formats; the use of extensible and repartitionable SoC reconfigurable devices; and the selection of software frameworks that offer a high level of productivity (like Python over embedded Linux). Furthermore, manufacturers can drastically reduce their time-to-market in addressing this new market by means of the readyto-use, value-added hardware IP now available. And of course, the system must also come with the highest levels of cybersecurity at the device, software and networking levels. For more information on SoC-e's IIoT IP portfolio, visit our site.

Manage the IoT on an Energy Budget part 1

> ## Silicon Labs

You might not think about it, but, on average, you utilize hundreds of microcontrollers (MCU) in a day. Everything from your toothbrush to your car has one or more MCUs inside them. And the number of MCUs you rely on is growing with the rapid adoption of the Internet of Things (IoT) movement.

So, what is this MCU inside everything? Like the name implies, a microcontroller is a small chip that controls something. It does this by processing a recipe, known as the program, which someone has written specifically for a product and stored inside the memory of the MCU. Because it is the program inside that decides how the MCU controls a product, one microcontroller can be used in two completely different products. We will discuss the reason for this later.

Historically, users wanted MCUs because they could process data and solve problems faster than a human could. MCUs also help make products more convenient and consistent in behavior. The microcontroller speed or frequency indicates how fast data is processed and problems are solved. Speed is generally not a big problem anymore. The challenge now is that the MCU needs to be able to solve more complex problems while it is being put on a power diet.

Let's face it. We all get a little worried and start looking for power outlets when our computer or smart phone battery gets close to zero. Imagine if all your battery-powered products required daily charging. To prevent this, we need to put our devices on a budget. They need to become energy efficient.

In this paper, we'll discuss how to use the Silicon Labs' 32-bit microcontroller family (EFM32 Gecko) to maximize energy efficiency in your embedded applications.

What is inside embedded applications?

At a high level, all embedded applications are strikingly similar. Everything from industrial products, like water meters and security sensors, to personal items, including smart wearables, are built from a number of components. These components are connected to each other to solve specific tasks. A typical application includes many building blocks. Here is a list of categories and some common components and functions:

Power management - Battery, regulators, energy harvesting, energy storage

Microcontroller - The brain

MCU support - Extra MCUs/co-processors, memories, external RTCs

Sensors/input - PIR, light, HRM, IMU, GPS, rotation count, capacitive touch

Actuators/output - Display, LED, audio, motor control
Wired connectivity - USB, UART, I2C, Ethernet, CAN, PLC
Wireless connectivity - Radio/RF, Bluetooth Smart, ZigBee, Thread, Proprietary, NFC
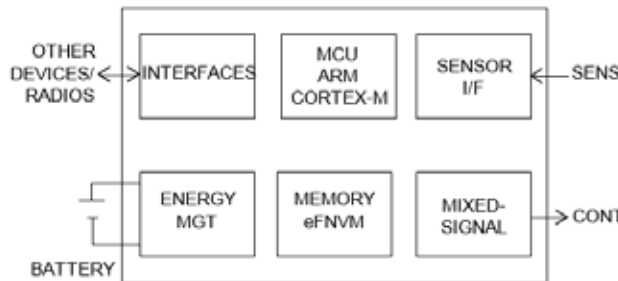
All of these components consume energy from your power source. So when building an energy-efficient system, logic dictates that you should choose components within your budget that are inherently energy efficient. This is sometimes difficult because many of the items listed above are highly integrated and combine functionalities. For example, in Silicon Labs Bluetooth Smart MCU, the Blue Gecko, both the bluetooth radio device and the MCU are combined, so the user only needs one device.

PHONE   EXAMPLE WATCH WITH BLUETOOTH SMART AND HRM
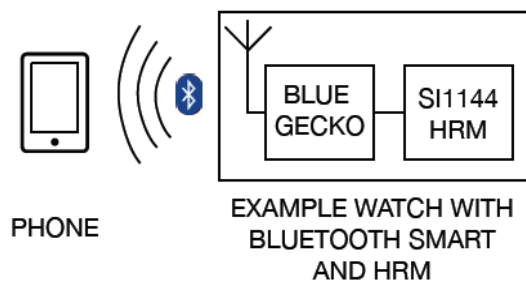
Almost always on?

Besides integration, you should also understand the components' various modes of operation. Most of them have an on mode and an off mode, but there may also be intermediate modes. Let's explore two analog voltage sensors for a moment. Both the Analog-to-Digital Converter (ADC) and Analog Comparator (ACMP), which are built in to the EFM32 products, can be used to monitor analog voltages in a system. Sensors in a system often produce analog voltages as their sensor output. The ADC is highly accurate and fast, with a 12-bit accuracy and 1 million samples per second. It also has a fast startup time. The ADC is a typical on/off peripheral, even though sample speed and accuracy can be varied.

The ACMP continuously compares the analog voltage against a pre-set threshold instead of taking individual samples. Startup time is not as important here because it is always running, and accuracy can be traded for current consumption. This allows it to monitor analog voltages all the way down to 100 nA of current consumption.

Which one of the ACMP or ADC is better depends solely on the needs of your application.

Energy Sources

There are many types of energy sources for embedded applications:

1. Wired Power - 110 V - 240 V AC, 12 V DC, energy "leeching"
2. Batteries - Coin cell, Li-Poly, Li-Ion, alkaline, Super-cap
3. Energy harvesting - Light, vibration, thermal, RF
4. Wireless Power - Light, magnetic, RF

A single application might use multiple power sources, but common across these energy sources, beyond the wired option, is that minimizing current consumption is key. For example, if you're building a wired home automation system, you may include a backup battery in case there is a power outage. This helps ensure that not all functionality is lost in an emergency.

The following are topics to think about when choosing an energy source for your application:

Mobility - Can the device move? Does it need to be near a socket?

Lifetime - For how long can the device live before it needs maintenance?

Cost - How expensive is this energy source?

Form factor - What size restrictions does my product have?

Designing with batteries

Let's say you're a designer and the specification states that the product or application needs to last for at least three years. You've decided to use batteries as the energy source. Now you need to make a tradeoff between lifetime, form factor, and cost.

Let's consider these two coin cell options:

Option A - CR1616, which comes in a 16 mm x 1.6 mm package with 55 mAh capacity.

Option B - Common CR2032, which has 20 mm x 3.2 mm dimensions with 210 mAh of capacity.

CR2032
20 mm x 3.2 mm
210 mAh
8 µA - max current draw
to achieve 3 year operation

CR1616
16 mm x 1.6 mm
55 mAh
2 µA - max current draw
to achieve 3 year operation
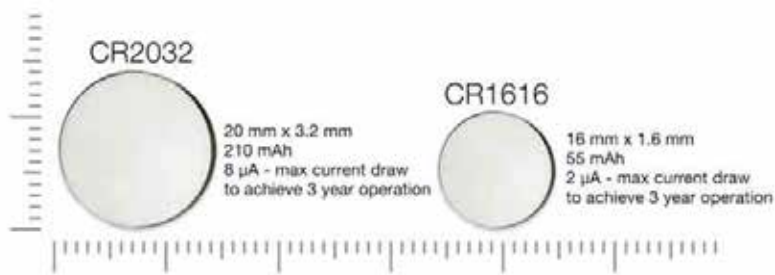
Coin Cell Battery Size Compare

With the CR2032, the average current consumption of your application needs to stay below 8 µA in order to get the desired lifetime of three years. If you go with the CR1616, the application must consume less than 2 µA to achieve the same lifetime. By making your application consume less than 2 µA, you go for the smaller battery, and thus get to a smaller form factor for the product.

Surprisingly, the smaller battery in this case actually has a higher cost than the larger one, so the current consumption reduction does not give a cost improvement when switching from the larger battery to the smaller. However, imagine switching from two of the CR2032 batteries to a single CR2032. That gives both a form factor and a cost improvement. Whether a single smaller battery has lower cost than a bigger one can depend on multiple factors, including product demand and availability.

If your application is a wearable or other rechargable accessory, you may want to bypass coin cell altogether and explore the lithium polymer batteries.

In general, energy harvesting looks like a very attractive solution. You just use the surroundings to generate the energy you need. But, as with batteries, energy harvesting has tradeoffs to consider. Is the power source reliable? Is your power converter efficient enough? Let's consider the sun, which is a pretty reliable and sustainable power source. Solar harvesting panels must be in a bright location, and they need to have a given surface area. They might be able to generate 10 mW/cm^2 under direct sunlight, but can drop to 10 µW/cm^2 when indoors. That is 1000 times less energy to play with! To support nighttime operation, a rechargeable battery is needed as well, which increases cost and penalizes form factor.

Designing with wireless power

Wireless power delivery, also known as remote power delivery, is similar to energy harvesting in that your application picks up energy from its surroundings. The difference is that in this case, energy is not assumed to be present, in the form of light, vibration, or other natural energy source. A power transmitter generates the energy the application is supposed to pick up.

The challenges with remote power delivery are somewhat similar to those of energy harvesting. For inductive power delivery, the transmitter is generating an alternating magnetic field, and the receiver uses a coil to capture the energy. In this scenario, the maximum distance between the transmitter and the receiver, and also the amount of power that can be delivered, are based on the size of the coil. This puts constraints on form factor and flexibility. Qi and A4WP are two emerging standards for inductive wireless charging, which is currently being used in a number of smart phones and weareables. These require the receiver and transmitter to be in very close proximity, and allow very little mobility. They are thus really only suitable for applications such as wireless charging.

Another method of remote power delivery is based on radio frequencies. By outputting a strong radio signal, and using beamforming techniques, a transmitter can send a signal carrying sufficient energy to a receiving antenna. Challenges with this technology currently include transmission efficiency.

Deciding which energy source to choose for an application depends on the properties of the application itself. The rest of this discussion will dig into applications that operate from constrained energy sources.

Energy Efficiency - The Big Picture

Sensors are the eyes and ears of an application. Table 1 below contains a list of sample sensors and their basic specifications. (see table 1 on next page)

When working with a sensor in an application, the straightforward approach is to leave the sensor on all the time, as shown in case A of Figure 1. With this approach, the MCU can read the voltage across the variable resistor at any time, and calculate the current temperature based on the voltage.

This option is the easiest way to control the sensor, but it's also the method that consumes the most energy. Now, 33 µA might not seem like much, but when a solar cell that small only produces 10 µW of current, we quickly see the problem. A better setup is shown in case B of Figure 1, where the MCU is able to control the power of the sensor directly, turning it on only when needed.

Two ways of powering a sensor
Figure 1 - Two ways of powering a sensor, in this case a variable resistor,

ENERGY MODE	ASSOCIATED NAME	EXAMPLE BASE CURRENT CONSUMPTION	CPU	HIGH-FREQUENCY PERIPHERALS	LOW-FREQUENCY PERIPHERALS	ASYNCHRONOUS PERIPHERALS	IO STATE AND WAKEUP
EM0	Run	114 µA/MHz	Y	Y	Y	Y	Y
EM1	Sleep	48 µA/MHz	-	Y	Y	Y	Y
EM2	Deep sleep	0.9 µA	-	(some)	Y	Y	Y
EM3	Stop	0.5 µA	-	(some)	(some)	Y	Y
EM4	Shutoff	20 nA	-	-	(some)	(some)	Y

Table 1 - Example component properties. Note that values will vary greatly depending on the chosen components.
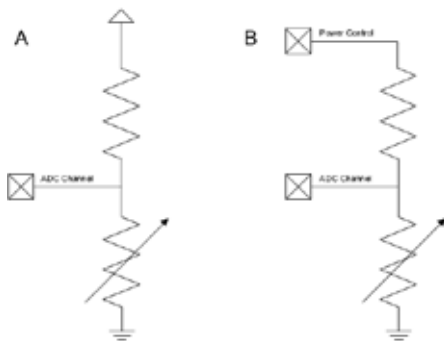
Figure 1 - Two ways of powering a sensor, in this case a variable resistor, which could be a thermistor.
In (A), current is always flowing through the resistors.
(B) is much more efficient, only drawing current whenever a measurement is needed.
The boxes in the drawing are MCU pins that can be driven high or low by the MCU to control the circuit.

which could be a thermistor. In (A), current is always flowing through the resistors. (B) is much more efficient, only drawing current whenever a measurement is needed. The boxes in the drawing are MCU pins that can be driven high or low by the MCU to control the circuit.

For an application that only needs to measure temperature once per second, the current consumption of the thermistor is now reduced to 0.165 nA. Assuming that you keep it on for 5 µs in order to sample it once every second, this approach gives you a 200,000x improvement in current consumption.

When controlling the supply of external components through a pin on the MCU, you have to clearly define the default state of these circuits. On EFM32 products, all pins are floating when the device comes out of reset, which, in this scenario, is not an issue. For a device with default-low IO, you want to connect the sensor as shown in case B of Figure 1. But if the IO comes out as default-high, you should connect the other end of the resistor divider to VDD (supply) instead of ground. This will prevent current consumption through the sensor during MCU reset.

An application can consist of a number of components, and you have to make a decision on how to control each component in the most efficient way. Note that designing for energy efficiency actually has a cost. In the thermistor example above, an extra MCU pin is required to control the power to the thermistor. Additional attention to efficiency also has to be given during software development.

Designing for energy efficiency can in some ways be harder than designing a system that does not care about efficiency. But in energy-constrained systems, it is well worth the investment.

What about the MCU?

We discussed that the application components must be duty-cycled in order to maximize efficiency. The same is true for the MCU itself. Because they are more sophisticated components, MCUs almost always have more than just an on/off button. MCUs have multiple energy modes, where each mode allows a set of capabilities with an associated current consumption overhead.

Table 2 shows an overview of the energy modes of the EFM32 MCUs. MCU energy modes will vary somewhat between MCU.

As seen in Table 2, the Run mode (EM0) has all functionality available. As the MCU goes to deeper energy modes, less functionality is available, but drastically lower current consumption can result. There are two key takeaways from this table:

1. The CPU is only available in the highest energy mode

In order to reap maximum benefits, the CPU must be turned off whenever it is not needed. The system must aim to sleep as much as possible.

2. The system should sleep as deeply as possible whenever it's sleeping

With deeper sleep, less functionality is available. Thus, the right modes have to be chosen to allow the system to sleep as much and as deeply as possible.

ENERGY MODE	ASSOCIATED NAME	EXAMPLE BASE CURRENT CONSUMPTION	CPU	HIGH-FREQUENCY PERIPHERALS	LOW-FREQUENCY PERIPHERALS	ASYNCHRONOUS PERIPHERALS	IO STATE AND WAKEUP
EM0	Run	114 µA/MHz	Y	Y	Y	Y	Y
EM1	Sleep	48 µA/MHz	-	Y	Y	Y	Y
EM2	Deep sleep	0.9 µA	-	(some)	Y	Y	Y
EM3	Stop	0.5 µA	-	(some)	(some)	Y	Y
EM4	Shutoff	20 nA	-	-	(some)	(some)	Y

Table 2 - Overview of energy modes on EFM32 Gecko MCUs.


```
TRADITIONAL CODE

//Program starts here
int main() {
    //Initialize sensor
sensor_init();

    while (1) {
        //Get current sensor value
int v = sensor_read();

        //Depending on sensor value
        //turn fan on or off. Note
        //that we also added a bit
        //of hysteresis here
if (v > threshold) {
fan_enable();
        }
        else if (v < threshold - 5) {
            fan_disable();
        }
    }
}
```

```
EVENT-DRIVEN CODE

//This interrupt handler is executed
//whenever the sensor tells us
//that temperature has crossed
//a threshold void
IRQ_Sensor() {
    //Get the current sensor value
int v = sensor_read();

    if (v > threshold) {
fan_enable();

        //We are currently at high
        //temp. Get interrupt
//again if temp falls
sensor_neg_threshold(v-5);
    }
else {
        fan_disable();

        //We are currently at low
        //temp. Get interrupt again
        //if temp rises
sensor_pos_threshold(v);
    }
}

//Program starts here
void main() {
    //Initialise sensor
sensor_init();

    //Set sensor to give interrupt
    //whenever above threshold
sensor_pos_threshold(threshold);

    while (1) {
        //Go to the deepest energy
        //mode where hardware can
        //still monitor temperature
goto_sleep();
    }
}
```

Sleep Mode
A system is said to be sleeping when its main coordinating function is powered down. For a microcontroller, sleep would mean that the CPU has stopped executing code. Since executing code consumes energy, sleeping conserves energy. With deeper levels of sleep, larger parts of the system is sleeping, giving higher energy savings, but with deeper sleep also comes the downside of less functionality available and longer wakeup times.

The EFM32 MCUs are designed to maximize the amount of time that can be spent in sleep modes, also known as energy modes. This is achieved by providing a broad amount of functionality in sleep modes, combined with fast wakeup times.

By requiring the CPU to be off as much as possible in order to save energy, the CPU tasks must be offloaded to the hardware in the MCU. Instead of being in a paradigm where software running on the CPU does everything, software development should focus on setting up hardware to do the heavy lifting and only intervene when hardware needs assistance. In other words, hardware should be the main driver of the application.

This takes the system to an event-driven architecture, allowing massive energy savings. Table 3 shows the sample code of an application that measures temperature using a thermistor, enabling a fan when temperature crosses a determined threshold. This example code assumes that the MCU has hardware that allows it to autonomously monitor the sensor and give an interrupt whenever the sensor crosses a threshold. In the "traditional" approach, this autonomous hardware is used, while in the "event-driven" approach, it is fully leveraged.

As you can see in the example (table 3), the event-driven code is more complex than the traditional code, but it has some significant advantages:

Massive energy savings
A system using the traditional approach running at 10 MHz would consume more than 1.1 mA, while a system using the event-driven

approach would consume as little as ~0.9 – 1.3 µA, depending on the sensor and sample rate. This is almost a three-orders-of-magnitude difference. More importantly, it's the difference between a day and multiple years of battery life.

Multi-tasking

With the traditional approach, the CPU does everything, and can only manage a limited number of functions. With the event-driven approach, the CPU is freed up because hardware does the bulk of the work. With this method, an MCU can drive sophisticated applications.

On an MCU with minimal flash and RAM resources, this is how you should write code. With this kind of multi-tasking you can get the absolute most out of the hardware in the MCU, both in terms of performance and energy savings. We call this "coding down to the metal."

Spending some of the MCU resources on an embedded operating system provides a level of abstraction that makes building sophisticated, event-driven applications easier, but potentially less efficient. For applications running on MCUs with 512 KB flash or more, the memory overhead can be negligible, making this an easy choice. On MCUs with 32 KB flash or less, there are still operating systems that can do the job, but the percentage of the MCU resources used by the OS increases drastically. A minimal configuration of FreeRTOS requires between 5 KB and 10 KB flash and a minimal amount of RAM.

For complex applications, an operating system might actually make the system more efficient than coding to the metal. This approach gives software developers a framework
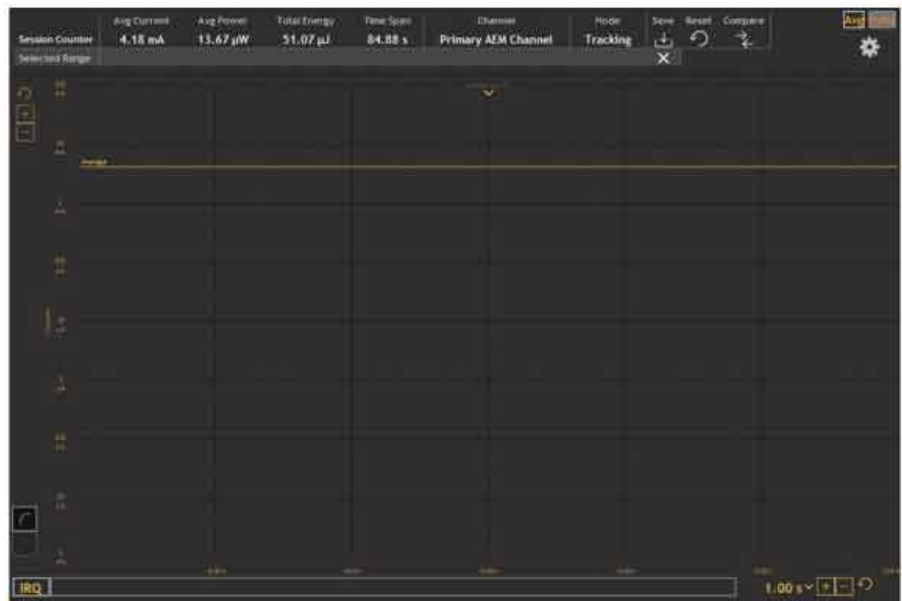
Figure 2 - Wonder Gecko traditional implementation sampling ADC @ 128Hz.

for how to write code to use energy modes in the most efficient way.

A couple of operating systems or ecosystems to check out are listed below. They all provide tick-less sleep modes, meaning that unlike normal PC operating systems that always waste energy by waking up every 1 ms or 10 ms, these operating systems only wake up when they are needed:

ARM mbed OS
FreeRTOS
RTX

Doing it in your sleep

In the previous section, we talked about the CPU letting hardware do the bulk of the work. While the CPU is sleeping and no software is running, the MCU should autonomously carry out the CPU's orders. There are two things to focus on here:

Sleep as deeply as possible
Wake up as seldom as possible

Looking back at the thermistor example, there are multiple ways of achieving this with varying amounts of sleep.

1. The traditional way

CPU uses ADC to continuously sample the thermistor.

This approach forces the CPU to be awake at all times, causing the highest current consumption. A traditional implementation of this, run on the EFM32 Wonder Gecko, results in the following current consumptions:

a. Wonder Gecko, sampling ADC @ 1 Hz: 4.18 mA

b. Wonder Gecko, sampling ADC @ 128 Hz: 4.18 mA

Figure 2 shows the system current consumption using the Advanced Energy Monitor (AEM) capability offered by Simplicity Studio, a combination of free tools provided by Silicon Labs. The current consumption is measured in real-time using hardware available on all EFM32 development kits. In this scenario, current consumption is dominated by the CPU, and very little variation can be seen from the ADC activity.

2. Improved

RTC wakes up the CPU periodically. On wakeup, the CPU uses the ADC to

sample the thermistor.

With the improved method, the CPU configures the RTC to provide a periodic wakeup. Since the RTC works all the way down to EM2 Deep Sleep, the MCU consumes only 0.9-1.4 µA while waiting for wakeup. On period wakeup, the CPU uses the ADC to take a sample, then potentially performs an action based on the result before going back to sleep. With this approach, the system can see a significant improvement in energy consumption.

RESPONSE TIME

Response time is the length of time taken by a system to react to a given stimulus or event. Faster response times often come at the expense of power consumption, because the event has to be checked for more frequently, and because once the event has been detected, the system needs to be able to respond in time, which could involve waking up from sleep, and the deeper sleep modes require longer wakeup times.

This scenario also brings up the notion of response time. The longer we can wait between samples, the more energy we can save. In a house where temperature changes slowly, the system can wake up to take a sample every 10 seconds. However, this also causes a 10-second reaction time to any temperature change event. In most systems, reaction time is a critical component and will vary with sensor type. Required sample-rate depends on what is being measured. For a heart-rate measurement system, one might want to measure the system 25 times a second. For a rotation-based water meter, up to a thousand times a second.

Figure 3 - Wonder Gecko, EM2 interrupt driven, sampling ADC @ 1 Hz.

Power gating also becomes critical in this scenario. Since we are now approaching system current consumptions around 1 µA, the 33 µA, current consumption of the thermistor becomes dominant unless the CPU makes sure the thermistor is powered only when it is being sampled.

Figure 3 shows the current consumption over time for the 1 Hz scenario. The Wonder Gecko consumes 0.95 µA in deep sleep mode, and the periodic wakeups to EM0 can clearly be seen. Note that the current consumption includes excitation of the external thermistor.

Using this approach, an application can get to the following current consumptions, which is considerably better than the first approach.

a. Wonder Gecko, sampling ADC @ 1 Hz: 1.30 µA

b. Wonder Gecko, sampling ADC @ 16 Hz: 2.43 µA

c. Wonder Gecko, sampling ADC @ 128 Hz: 10.46 µA

d. Wonder Gecko, sampling ADC @ 1024 Hz: 72.48 µA

3. Optimal

MCU autonomously monitors the thermistor, only waking the CPU when the threshold is crossed.

If an MCU supports autonomous external sensor monitoring while also duty-cycling them, this is by far the most efficient option. Low Energy Sense (LESENSE), available on devices in the EFM32 portfolio, is able to autonomously monitor up to 16 external resistive, capacitive, or inductive sensors, while also properly turning off the sensor when not in use.

With this approach, the CPU does not wake up around every sample, as in the second option. It wakes up only when a sample is outside of a set threshold. This concept is demonstrated in Figure 4, where the system is able to stay in EM2 continuously.

For a very slowly sampled system, using the ADC as in the second option is better because LESENSE uses some current to operate. But for higher frequency systems, LESENSE definitely has a benefit. It reduces the current consumption by more than

10X in the system sampled at 1024 Hz:

a. Wonder Gecko, LESENSE @ 1 Hz: 1.49 µA

b. Wonder Gecko, LESENSE @ 16 Hz: 1.57 µA

c. Wonder Gecko, LESENSE @ 128 Hz: 2.06 µA

d. Wonder Gecko, LESENSE @ 1024 Hz: 5.92 µA

LESENSE can also simplify software development by treating measurements as its own autonomous system, freeing up the ADC for other tasks.

to be continued in our next magazine...
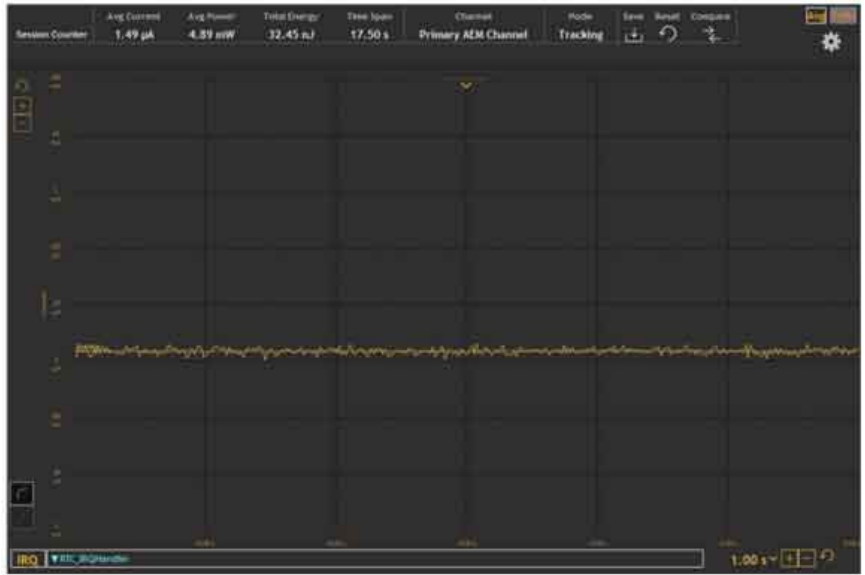
Figure 4 - Wonder Gecko, Wonder Gecko, LESENSE, sampling @ 1 Hz.

Researchers Teaching Robots to Feel and React to Pain

One of the most useful things about robots is that they don't feel pain. Because of this, we have no problem putting them to work in dangerous environments or having them perform tasks that range between slightly unpleasant and definitely fatal to a human. And yet, a pair of German researchers believes that, in some cases, feeling and reacting to pain might be a good capability for robots to have.

The researchers, from Leibniz University of Hannover, are developing an "artificial robot nervous system to teach robots how to feel pain" and quickly respond in order to avoid potential damage to their motors, gears, and electronics. They described the project last week at the IEEE International Conference on Robotics and Automation (ICRA) in Stockholm, Sweden, and we were there to ask them what in the name of Asimov they were thinking when they came up with this concept.

Why is it a good idea for robots to feel pain? The same reason why it's a good idea for humans to feel pain, said Johannes Kuehn, one of the researchers. "Pain is a system that protects us," he told us. "When we evade from the source of pain, it helps us not get hurt." Humans that don't have the ability to feel pain get injured far more often, because their bodies don't instinctively react to things that hurt them.

Kuehn, who worked on the project with Professor Sami Haddadin, one of the world's foremost experts in physical human-robot interaction and safety, argues that by protecting robots from damage, their system will be protecting humans as well. That's because a growing number of robots will be operating in close proximity to human workers, and undetected damages in robotic equipment can lead to accidents. Kuehn and Haddadin reasoned that, if our biological mechanisms to sense and respond to pain are so effective, why not devise a bio-inspired robot controller that mimics those mechanisms? Such a controller would reflexively react to protect the robot from potentially damaging interactions.

The idea of a reflex controller for robots isn't a new one. Torsten Kroeger and colleagues at Stanford and the University of Rome–La Sapienza developed one half a decade ago that helped a robot arm avoid collisions with people:

As you can see, this controller does collision avoidance, and it's very concerned with not running into that human, but not at all concerned with its own safety, except as a byproduct. Indeed, an artificial robot nervous system designed to feel pain and react to it is completely different, and based on how humans deal with painful tactile sensations, as Kuehn and Haddadin write in their ICRA paper:

A robot needs to be able to detect and classify unforeseen physical

Out Of the box

states and disturbances, rate the potential damage they may cause to it, and initiate appropriate countermeasures, i.e., reflexes. In order to tackle this demanding requirement, the human antetype shall serve as our inspiration, meaning that human pain–reflex movements are used for designing according robot pain sensation models and reaction controls. We focus on the formalization of robot pain, based on insights from human pain research, as an interpretation of tactile sensation.

This video shows a prototype of the controller running on a Kuka arm equipped with a BioTac tactile fingertip sensor (it can sense pressure and also temperature). I find that it helps if you

imagine the robot saying "Ouch!" louder and louder each time: The robot's tactile system is using a "nervous robot-tissue model that is inspired by the human skin structure" to decide how much pain they should feel for a given amount of force. Just like human neurons, the model transmits pain information in repetitive spikes if the force exceeds a certain threshold, and the pain controller reacts after classifying the information into light, moderate, or severe pain.

In the [light] pain class, such contacts occur that may harm the robot or prevent it from performing the task. The robot "feels" uncomfortable and shall smoothly retract until the contact event is over and return thereafter. Strong collisions are covered in the [moderate] pain class. The robot "feels" moderate pain, shall quickly retract, and more distant until the contact event is over. Then, it may move back. The [severe] pain class covers all contacts in which the robot may be damaged and thus needs some sort of "help". In order to prevent making the damage worse, the robot switches to gravity compensation with additional damping for dissipation, improving the safety of the robot and the environment by its strictly passive behavior.

In terms of both bio-inspiration and control, this paper is just the first step towards a pain-based reflex controller for robots, but as sinister as it sounds, it's something that most robots could get a lot of use out of, especially given the overall increase in robot autonomy and collaboration with human workers. Keeping robots from hurting people is certainly a top priority, but even Asimov would agree that keeping robots from hurting themselves is also important if we want to have them around us.

"An Artificial Robot Nervous System to Teach Robots How to Feel Pain and Reflexively React to Potentially Damaging Contacts," by Johannes Kuehn and Sami Haddadin from Leibniz University in Hannover, was presented last week at ICRA 2016 in Stockholm, Sweden.

Leibniz University of Hannover Evan Ackerman

STMicroelectronics and SAG Cooperate to Deliver High-Performance, Tiny NFC Tags for IoT Applications

STMicroelectronics (NYSE: STM), a global semiconductor leader serving customers across the spectrum of electronics applications, and Securitag Assembly Group (SAG), a leading supplier of RFID transponders announced a tiny NFC Ferrite Tag that uses STMicroelectronics' ST25 NFC tag IC for IoT (Internet of Things) data-transmission applications.

Small, light, and thin, the NFC Ferrite Tag can be surface–mounted during production through the metal pad that can be directly soldered to the PCB surface. In addition, the NFC Ferrite tag can function when placed on metal products because of its anti-metallic interference characteristics. These features make it highly attractive for IoT data-transmission applications in consumer electronics, wearable devices, and smart healthcare products. The tiny NFC Ferrite Tag perfectly suits the need for smaller, thinner, and lighter design for wearable products where compactness is critical.

Along with its small dimensions (4.9 x 3.0 x 2.5 mm), the NFC Ferrite Tag with an embedded antenna demonstrates outstanding RF performance, benefiting from ST's state-of-the-art ST25TA02K NFC Forum Type 4 tag IC with built-in NDEF (NFC Data Exchange Format) message support. This allows the NDEF data to be directly executed through an Android NFC phone without any dedicated application software. In addition to NDEF support, the ST25TA02K features a 20-bit counter and 128-bit password to protect read / write access to the 2Kbit EEPROM memory.

Manufacturers will ship as many as 2.2 billion NFC-enabled smartphones by 2020 according to IHS Technology (Market Insight, NFC-enabled Handset Shipments to Reach Three-Quarters of a Billion in 2015, June 2015). The growing momentum for NFC is expected to drive new IoT and wireless applications in the Smart Home, Smart Healthcare/ Medical, Smart City, and Smart Factory. With ST's global reach and semiconductor leadership, combined with SAG's professional manufacturing of RFID tags, the two companies aim to accelerate innovation and new product development that strengthens the competitiveness of their customers' final products.

Two-Channel, Bi-Directional Digital Isolators Reduce Space and System Complexity for Designers

Designers can save space and achieve more flexible designs with theMAX14933 and MAX14937 two-channel, bi-directional digital isolators from Maxim Integrated Products, Inc. (NASDAQ: MXIM). They transfer digital signals between circuits in both directions and provide complete galvanic isolation between two power domains, all while using fewer components to save board space.

More information about the MAX14933 ›
More information about the MAX14937 ›
A schematic is available for download ›
A hi-res image is available for download ›

The MAX14933 and MAX14937 are the newest additions to Maxim's recently introduced ultra-robust portfolio of quad-channel digital isolators, which include MAX14930–MAX14932 and MAX14934–MAX14936. These devices provide best-in-class speed, propagation delay, skew, and jitter for timing sensitive applications while maintaining an extremely robust isolation barrier between two power domains.

Digital isolators are replacing optocouplers in many applications because they offer the same isolation capabilities while using less board space and consuming less power. The MAX14933 and MAX14937 provide high voltage isolation of 2.75kVRMS or 5kVRMS, respectively. They support data rates from DC up to 1.7MHz and can be used in isolated I2C busses with or without clock stretching. Both products feature independent 2.25V to 5.5V supplies on each side of the isolator, and provide open-drain channels for applications that require data to be transmitted in

both directions on the same line. Applications include power supplies, battery management systems, instrumentation, and interfaces for I2C, SMBus, or PMBus.

Key Advantages

Space savings: Lowers component count and system complexity

Flexible interface: Interfaces with most microcontrollers and FPGAs running at various supply voltages

Robust galvanic isolation: More than 30 years lifetime at rated working voltage

Commentary

"These I2C, two-channel, bi-directional digital isolators provide a solution for designers who want to lower component count and system complexity," said Tony Partow, Executive Business Manager at Maxim Integrated.

Availability and Pricing

The MAX14933 is available in both a 16-pin wide-body (10.3mm x 7.5mm) and narrow-body (9.9mm x 3.9mm) SOIC package. The MAX14937 is available in a 16-pin wide-body (10.3mm x 7.5mm) SOIC package.

Pricing starts at $1.80 for the MAX14933ASE and $2 for the MAX14933AWE (1000-up, FOB USA). Pricing starts at $3.29 for the MAX14937AWE (1000-up, FOB USA).

Both products are specified over the -40°C to +125°C temperature range.

An evaluation kit is available for both products: MAX14933WEVKIT# and MAX14937WEVKIT#.

For more information about the family of products, visit http://bit.ly/Maxim_Digital_Isolators.

Latest ARM Premium Mobile Technology to Drive Immersive Experiences

ARM premium IP will redefine virtual reality (VR) and augmented reality (AR) experiences on 2017 flagship mobile devices

The ARM® Mali™-G71 graphics processor offers advanced efficiency and performance gains from the new Bifrost architecture

The ARM Cortex®-A73 addresses the most demanding use cases with impressive increases in sustained performance and efficiency

Products are optimized for the latest 10nm FinFET process technology.

Cambridge, UK, May 30, 2016 – ARM has announced a suite of premium mobile processor technologies to redefine flagship devices from 2017. The ARM Cortex-A73 processor and the ARM Mali-G71 graphics processor offer sustained performance and efficiency gains that will lead to new products with enhanced contextual and visual capabilities. This will allow devices to run high resolution content for longer periods while staying within strict mobile power budgets.

"The smartphone is the world's most ubiquitous compute device, offering experiences that improve with each new product generation," said Pete Hutton, executive vice president and president, product groups, ARM. "In 2017, we will see devices with the Cortex-A73 and Mali-G71 processors that stand out thanks to their impressive and sustained performance, and even more stunning visuals. This technology can make engaging with 4K video, virtual reality and augmented reality an everyday experience on a mobile device."

Mali-G71: A Step Change in ARM Mali GPU Performance

The Mali-G71 graphics processor unit (GPU) increases the momentum for ARM Mali products, now the industry's number one shipping graphics processor technology. The new core enables a 50 percent increase in graphics performance, a 20 percent increase in power-efficiency and 40 percent more performance per mm2.

The Mali-G71 scales efficiently up to 32 shader cores, twice as many as the previous generation premium IP GPU – the Mali-T880. The uplift means the Mali-G71 surpasses the performance of many discrete GPUs found in today's mid-range laptops. The product is also fully coherent, helping to simplify software development and efficiency. It is ideally suited to power immersive VR and AR experiences on mobile devices and leading silicon providers including HiSilicon, MediaTek and Samsung Electronics have already taken licenses.

Bifrost, the third-generation ARM GPU architecture, is the foundation

of the Mali-G71. The architecture is optimized for Vulkan and other industry-standard APIs, building on innovations from the previous Utgard and Midgard architectures.

"VR is one of the most important technological breakthroughs for the gaming industry in a generation," said Niklas Smedberg, technical director, platform partnerships, Epic Games. "The ability to deliver a compelling VR experience on all platforms, but especially mobile, is critical for the industry's continued growth and advancement. To enable a great mobile VR experience, devices need to be the highest performing and most energy efficient available."

"It's basic math – the sheer number of smartphones in the world is already double PCs and rising, which makes it the single most important device for accelerating VR gaming adoption," said Clive Downie, CMO Unity Technologies. "ARM is making smart investments that move the mobile VR and AR ecosystems forward. By creating more efficient and powerful technology solutions for mobile they are helping push the boundaries of what is possible in the virtual world and everyone will benefit."

Cortex-A73: More Efficiency and Performance for Mobile SoCs

At under 0.65mm2 per core (on a 10nm FinFET process technology) the Cortex-A73 is the smallest and most efficient 'big' ARMv8-A core. Its advanced mobile microarchitecture enables a 30 percent uplift in sustained performance and power efficiency over the Cortex-A72.

Size and efficiency improvements enhance the ability of silicon providers to use the Cortex-A73 in ARM big.LITTLE™ configurations. These improvements create further opportunities for designers to scale big cores along with the GPU and other IP in a single SoC. Ten partners have licensed the Cortex-A73 so far, including HiSilicon, Marvell and Mediatek.

"In order to deliver more quality and excellent smartphone experiences to consumers, Huawei will continue enhancing the integrated performance of our premium smartphones," said Kevin Ho, President, handset business, Huawei consumer business group. "The system-level approach that ARM takes in developing its IP is a vital element in ensuring our design teams are able to maximize efficiency and performance across the entire device."

In addition to smartphones, ARM's latest premium IP suite offers the increased performance density and throughput required for other consumer electronics applications such as large-screen compute devices, industrial gateways, in vehicle infotainment and smart TVs..
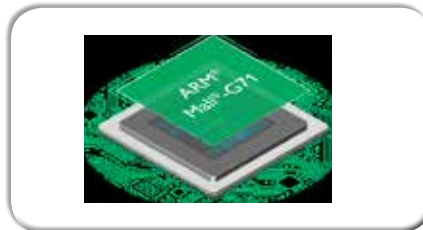
16-Bit, 5Msps SAR ADC with Wide Input Common Mode Range Simplifies Analog Front-End Circuitry

Linear Technology Corporation introduces the LTC2311-16, a 16-bit, 5Msps successive approximation register (SAR) analog-to-digital converter (ADC) with a wide rail-to-rail input common mode range. The LTC2311-16 features a flexible differential input that accepts analog signals up to the Nyquist frequency. This provides direct conversion of a variety of signal types while maintaining a good signal-to-noise ratio (SNR) of 81.6dB with a 2.2MHz input signal, and achieving a high common mode rejection ratio (CMRR) of 85dB for the same high speed input signal.

Instrumentation and medical applications that require channel-to-channel isolation often use single-channel ADCs to individually isolate front-end circuitry. Each of the ADC channels then requires its own signal conditioning circuitry along with an isolated power source. This circuit is replicated on all channels, so any simplification in the circuit has a profound effect on the complexity of the system. The flexible differential inputs and wide input common mode range of the LTC2311-16 simplify the input signal conditioning design, significantly lowering the required component count, reducing system cost, power consumption and circuit board space.

The LTC2311-16 leads a pin-compatible family of 16-, 14- and 12-bit SAR ADCs with sample rates of 5Msps and 2Msps. These devices integrate a precision internal reference with low drift, guaranteeing 20ppm/°C maximum temperature coefficient to simplify

system design. This family can be powered from either a 3.3V or 5V supply, and consumes 30mW with a 3.3V supply and 50mW at 5V. The high speed SPI-compatible CMOS or LVDS serial interface is ideal for highly integrated high speed systems.

The LTC2311-16 is available today in commercial, industrial and automotive (-40°C to 125°C) temperature grades. Other devices in the family will be releasing through 2016. Pricing begins at $9.95 each in 1,000-piece quantities. Samples and demo boards may be requested LTC2311-16, or by contacting your local Linear Technology sales office.

Summary of Features: LTC2311-16

5Msps (LTC2311) or 2Msps (LTC2310) Throughput Rate

8Vp-p Differential Input with Wide Input Common Mode

81.6dB SNR, -90dB THD at fIN = 2.2MHz (16 Bits)

±3LSB INL (Typ), ±8LSB INL (Max)

Low Drift (20ppm/°C Max), 2.048V or 4.096V Internal Reference

Single 3.3V or 5V Supply

No Cycle Latency (LTC2310)

Low Power Dissipation of 30mW (3.3V) or 50mW (5V)

CMOS or LVDS SPI-Compatible Serial I/O

Guaranteed Operation from -40°C to 125°C

Small 16-Lead 4mm x 5mm MSOP Package

16-Bit 5Msps SAR ADC with

Wide Input Common Mode Range

Intersil's 5A and 3A Power Modules Offer Industry-Leading Power Density and Efficiency

Intersil Corporation (NASDAQ: ISIL), a leading provider of innovative power management and precision analog solutions, today announced two new single-channel DC/DC step-down power modules that deliver high power density and up to 95% efficiency in a compact 4.5mm x 7.5mm x 1.85mm footprint. The pin-compatible 5A ISL8205M and 3A ISL8202M provide point-of-load (POL) conversions for FPGAs, DSPs and MCUs in a wide range of home networking and high-end consumer products, as well as portable industrial equipment that use Li-ion batteries. The modules are complete power supplies that include a controller, MOSFETs, inductor and passive components inside an encapsulated module, simplifying system design.

With a height of 1.85mm, the ISL8205M and ISL8202M can be directly mounted on the backside of a PCB, freeing up valuable space for topside mounted components. Both devices support input voltages from 2.6V to 5.5V and offer adjustable output voltages as low as 0.6V. The pin compatibility allows engineers to start with a 3A power module and later migrate to the higher 5A output current, or design a power tree with multiple POL output rails. For battery-operated applications, the ISL8205M and ISL8202M offer unique efficiency and power saving features to extend battery life and support Energy Star® compliant

products. Selectable light load efficiency, 100% duty cycle modes and 50µA quiescent current enable better efficiency and lower power consumption at light load.

Both power modules leverage Intersil's patented technology and advanced packaging to offer high power density and superior thermal dissipation performance. A copper lead-frame structure allows the modules to operate at full load over a wide temperature range with no airflow or heatsinks. The ISL8205M and ISL8202M also provide several protection features that ensure safe operations under abnormal operating conditions, further enhancing their robustness and reliability.

"The ISL8202M and ISL8205M analog power modules speed time to market and provide the industry's best combination of power density and performance," said Mark Downing, senior vice president of Infrastructure and Industrial Power Products at Intersil. "Their size, light load efficiency and 100% duty cycle performance gives customers everything they need to address their increasingly compact battery-powered designs."

Key Features and Specifications of ISL8205M and ISL8202M

Single-channel 5A and single-channel 3A switching power supplies

Pin compatibility

Up to 95% efficiency

Wide input voltage range from 2.6V to 5.5V

Adjustable output as low as 0.6V with +/- 1.6% accuracy over line,

load and temperature

Adjustable switching frequency from 680kHz to 3.5MHz, with 1.8MHz default

External clock signal synchronization up to 3.5MHz

Selectable light-load efficiency mode and 100% duty cycle LDO mode extend battery life

Dedicated enable pin and power-good flag simplify sequencing of system power rails

Fault protections include input under-voltage lockout, over-temperature, over-current/short-circuit with hiccup mode, over-voltage and negative over-current

Programmable soft-start reduces inrush current, and automatic output discharge ensures a soft stop

Pricing and Availability

The ISL8205M power module is available now in a 4.5mm x 7.5mm, 22-lead QFN package and is priced at $3.79 USD in 1k quantities. An ISL8205MEVAL1Z evaluation can be purchased for $69 USD each. For more information, please visit: www.intersil.com/products/ISL8205m.

The ISL8202M power module is available now in a 4.5mm x 7.5mm, 22-lead QFN package and is priced at $2.79 USD in 1k quantities. An ISL8202MEVAL1Z evaluation can be purchased for $69 USD each. For more information, please visit: www.intersil.com/products/ISL8202m.

The ISL8205M and ISL8202M complement the highly popular dual-channel 3A/single-channel 6A ISL8203M in Intersil's low-voltage product line. They join a comprehensive family of analog and digital power modules that support 1V to 80V input voltage rails and

3A to 80A output current to satisfy a broad range of applications. For more information on Intersil's power module portfolio, please visit: www.intersil.com/powermodules.

TI unveils industry's highest power density 12-V, 10-A, 10-MHz DC/DC converter

Ultra-small SWIFT™ step-down converter features unique topology to achieve four times higher current density

Texas Instruments (TI) (NASDAQ: TXN) today introduced the industry's first 12-V, 10-A, 10-MHz series-capacitor buck converter that achieves more than 50 A/cm3 in current density, which is four times higher than any other 12 V power management component or solution available today. The unique topology of the TPS54A20 SWIFT synchronous DC/DC converter enables high-frequency operation at up to 5 MHz per phase without special magnetics or compound semiconductors, which designers can use for 8-V to 14-V input and 10-A output applications. By using the step-down converter together with TI's WEBENCH® Power Design tool, engineers can get their space- and height-constrained point-of-load (POL) telecom and networking power-supply designs to

market faster. For more information, samples and an evaluation module, visit www.ti.com/tps54a20-pr-eu.

The TPS54A20 features a unique two-phase, series-capacitor DC/DC buck topology that merges a switched-capacitor circuit with a multiphase buck converter. This capacitive conversion technology enables efficient, high-frequency operation and measures as much as seven times smaller than conventional converters. For a quick introduction, watch the video "How to decrease inductor size in a 10-A DC/DC converter design" and read the white paper, "Breakthrough power delivery for space-constrained applications." Read the application note "Introduction to the Series Capacitor Buck Converter" that analyzes the technology and presents example results for a 12-V input, 1.2-V/10-A output application demonstrating higher peak efficiency than a conventional buck converter, while operating at four times higher switching frequency.

TPS54A20 key features and benefits

Tiny solution: Small HotRod™ quad flat no-lead (QFN) packaging and inexpensive, tiny 2- to 5-MHz inductors enable a 131-mm2 solution size that consumes 50 percent less area than similar 500-kHz DC/DC converter designs. Read the blog post, "No small matter: How to reduce voltage regulator size."

Low profile: Measuring less than 2 mm in height, the reduced size, weight and bill of materials (BOM) allows placement of tiny 10-A voltage regulators on the back

side of a printed circuit board (PCB), enabling engineers to take advantage of the small size that the TPS54A20 offers for industrial servers or other space-constrained applications.

Multi-megahertz operation: A 14-ns minimum on-time allows for 4-/7-/10-MHz operation without compromising efficiency or electromagnetic interference (EMI) performance. Download the "Three Different Buck Converter Circuits to Convert 12V to 1.2V at >6A Load Current Reference Design," which includes a 1.2-V output voltage for double-data-rate (DDR) 4 memory applications.

Availability, packaging and pricing
The new DC/DC converter is available in volume now from TI and its authorized distributors. Offered in a 20-pin, 3.5-mm-by-4-mm-by-1-mm thermally enhanced HotRod QFN package, the TPS54A20 is priced at US$3.25 in 1,000-unit quantities. Order the 4-MHz, 10-A TPS54A20EVM-770 synchronous dual-phase converter evaluation module and download the PSpice transient models.

SWIFT™ Power Management
TPS54A20
TEXAS INSTRUMENTS

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Find out more about TI's power-management portfolio

Get more information on TI's high-performance SWIFT DC/DC converter portfolio for any power-supply application.

Search for solutions, get help and share knowledge in the TI E2E™ Community Power Management forum.

Download power reference designs from the TI Designs reference design library.

Ultra-small SWIFT™ step-down converter features unique topology to achieve four times higher current density

Texas Instruments (TI) (NASDAQ: TXN) today introduced the industry's first 12-V, 10-A, 10-MHz series-capacitor buck converter that achieves more than 50 A/cm3 in current density, which is four times higher than any other 12 V power management component or solution available today. The unique topology of the TPS54A20 SWIFT synchronous DC/DC converter enables high-frequency operation at up to 5 MHz per phase without special magnetics or compound semiconductors, which designers can use for 8-V to 14-V input and 10-A output applications. By using the step-down converter together with TI's WEBENCH® Power Design tool, engineers can get their space- and height-constrained point-of-load (POL) telecom and networking power-supply designs to market faster. For more information, samples and an evaluation module, visit www.ti.com/tps54a20-pr-eu.

Figure 1: Size comparison between a 12VIN, 10AOUT buck converter operating at 500kHz (a-right) and a series-capacitor buck converter operating at 2MHz per phase (b-left)

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The TPS54A20 features a unique two-phase, series-capacitor DC/DC buck topology that merges a switched-capacitor circuit with a multiphase buck converter. This capacitive conversion technology enables efficient, high-frequency operation and measures as much as seven times smaller than conventional converters. For a quick introduction, watch the video "How to decrease inductor size in a 10-A DC/DC converter design" and read the white paper, "Breakthrough power delivery for space-constrained applications." Read the application note "Introduction to the Series Capacitor Buck Converter" that analyzes the technology and presents example results for a 12-V input, 1.2-V/10-A output application demonstrating higher peak efficiency than a conventional buck converter, while operating at four times higher switching frequency.

TPS54A20 key features and benefits

Tiny solution: Small HotRod™ quad flat no-lead (QFN) packaging and inexpensive, tiny 2- to 5-MHz inductors enable a 131-mm2 solution size that consumes 50 percent less area than similar 500-kHz DC/DC converter designs. Read the blog post, "No small matter: How to reduce voltage regulator size."

Low profile: Measuring less than 2 mm in height, the reduced size, weight and bill of materials (BOM) allows placement of tiny 10-A voltage regulators on the back side of a printed circuit board (PCB), enabling engineers to take advantage of the small size that the TPS54A20 offers for industrial servers or other space-constrained applications.

Multi-megahertz operation: A 14-ns minimum on-time allows for 4-/7-/10-MHz operation without compromising efficiency or electromagnetic interference (EMI) performance. Download the "Three Different Buck Converter Circuits to Convert 12V to 1.2V at >6A Load Current Reference Design," which includes a 1.2-V output voltage for double-data-rate (DDR) 4 memory applications.

Triple-Channel Universal PMIC Supports Low Power FPGA and SoC Processors

Exar Corporation (NYSE: EXAR), a leading supplier of analog mixed-signal products serving the industrial, high-end consumer

and infrastructure markets, today announced the introduction of the XR77103 Universal PMIC, Exar's first Universal PMIC with three integrated synchronous MOSFET power stages. This integration results in an even smaller solution than was possible before, a tiny, 4mm x 4mm IC which delivers an easy-to-use power management solution for a broad range of FPGAs, SoCs, DSPs and video processors. The XR77103 features an I2C interface allowing customers to control output voltage (from 0.8V to 6V), switching frequency (from 300kHz to 2.2MHz), power sequencing, and current limit. The XR77103 is supported by a new release of PowerArchitectTM 4 design and configuration software.

The XR77103 operates from a 4.5V to 14V input supply and all three outputs are designed for 2A load currents with peak currents up to 3A. Since the device employs a current mode control architecture, outputs can be easily paralleled to provide up to a total of 5A allowing the XR77103 to power a range of low power processors. A selectable Pulse Skipping Mode (PSM) results in improved efficiency at light loads, a key feature in meeting standby energy requirements or extending battery life.

As the device supports up to a 2.2MHz switching frequency and is packaged in a 4x4mm QFN, it requires fewer and smaller external components, saving engineers valuable board space in their next design. This family also includes two versions of the XR77103 which offer a fixed set of features

for designers not requiring the I2C interface. The XR77103ELB-A0R5 and –A1R0 are fixed at switching frequencies of 500kHz and 1MHz, respectively. Both products feature a 0.8V, high accuracy reference (1%) and their output voltages are set by external resistors.

"The XR77103 Universal PMIC with integrated MOSFETs showcases Exar's enhanced integration capability for monolithic power solutions," said Tuomas Hollman, Exar's vice president, power management products. "This extends our portfolio to cover systems that require multiple low current rails in a highly integrated solution, making the XR77103 an ideal fit for applications such as projectors, displays, industrial HVAC systems and home gateways."

Low Loss 3-Phase Ideal Diode Bridge Rectifier Reduces Heat, Easing Thermal Design

Linear Technology Corporation announces the availability of a low loss 3-phase ideal diode bridge rectifier reference design, demonstrated on evaluation board DC2465. Conventional 3-phase rectifiers employ six diodes, but the diodes drop voltage and dissipate significant power at just a few amperes of load current. This requires costly heat sinking and active cooling solutions that

complicate thermal design and increase solution size. The DC2465 design replaces the six diodes with three LT4320 ideal diode bridge controllers, driving six low loss N-channel MOSFETs, dramatically reducing power and voltage losses. This enables the overall system to be specified to operate with a smaller, more cost-effective power supply due to the enhanced power efficiency. Low voltage applications benefit from the extra margin afforded by saving the two diode drops inherent in diode bridges. Compared to traditional approaches, the MOSFET bridge enables a rectifier design that is highly space- and power-efficient.

The DC2465 board rectifies line-to-line AC voltages from 9VRMS to 48VRMS with frequencies up to 400Hz while sourcing a load of up to 25A without forced airflow. Efficiency at 9V input is raised from 84% for a diode bridge to 97% for the active bridge.

The DC2465 evaluation board is available, priced at $125.00 each. The LT4320 ideal diode bridge controller IC is offered in 8-pin MSOP, PDIP, and 3mm x 3mm DFN packages. Evaluation circuit boards are available online or from your local Linear Technology sales office. For more information, visit www.linear.com/demo/DC2465.

Cypress USB-C Power Delivery Solution Helps LeEco Debut the World's First Smartphones with One Port for Data Transmission, Power Charging and Audio

Cypress Semiconductor Corp. (Nasdaq: CY) today announced that LeEco, a leading global technology company, has selected Cypress's USB-C controller solution to implement the USB-C port on its flagship Le Max2 superphone—providing the only physical connector on the phone. The Cypress EZ-PD™ CCG2 controller helps enable the sleek, one-port design of the innovative Le Max2, which is the first phone to remove the ubiquitous audio jack and use the USB-C port for audio, in addition to charging and data. LeEco's Continual Digital Lossless Audio (CDLA) technology delivers true fidelity audio and lossless music experience via the USB-C port. The Le Max2 is also the market's first phone to enable fast charging utilizing the USB Power Delivery (PD) standard, which allows transfer of more than 15W of power over the Type-C connector. The Le Max2 charger uses Cypress's USB-C controller solution to implement USB PD as well.

Optimized for the 2.4-mm thin USB-C connector, the programmable EZ-PD CCG2 controller is capable of fully supporting USB PD and other proprietary charging standard implementations in smartphones, tablets, and mobile chargers. CCG2 provides a complete, robust solution by integrating the USB-C

transceiver, PD protocol and policy layer functions. Available in a 3.3 mm2 20-ball Wafer Level Chip Scale Package (WLCSP), a 14-pin DFN and a 24-pin QFN, CCG2 also includes system-level ESD protection and termination resistors needed for all USB-C applications. Cypress is demonstrating CCG2 and its complete portfolio of USB-C and PD solutions at Computex from May 31 to June 4 at the USB-IF Pavilion in booth M0309a in the Nangang Hall 4F Exhibition Center in Taipei. More information on the CCG2 controller is available at http://www.cypress.com/ccg2.

"LeEco selected the Cypress USB Type-C and Power Delivery solution because of its interoperability performance and robust implementation of the PD protocol for flexible, on-demand PD charging," said Gao Chao, Hardware Director of LeEco. "With Cypress's strong support, we were able to get to market first with faster PD charging in our Le Max2 phone."

"The Le Max2 marks a new generation of smartphones that will use a single USB-C port to connect and charge," said Ajay Srikrishna, vice president of the USB product line at Cypress. "Cypress's programmable EZ-PD controllers enable our customers to bring their innovative designs to market quickly, with the confidence that comes with our USB-IF-certified solutions. The Le Max2 charger is one of only three chargers on the market to be certified as compliant to the USB Power Delivery standard, and the other two are also based on Cypress solutions."

The USB Type-C standard is gaining rapid support with top-tier PC and electronics manufacturers by enabling slim industrial designs, easy-to-use connectors and cables, and the ability to transmit multiple protocols and deliver up to 100W of power. The USB Type-C standard's 2.4-mm-high connector plug is significantly smaller than the current 4.5-mm USB Standard-A connector. In addition to the transport of USB signals, DisplayPort and Thunderbolt signals can be delivered over the same connector via the USB Type-C standard's Alternate Mode capability. More info on Cypress's USB Type-C and PD solutions is available at www.cypress.com/Type-C.

Panasonic Develops Two Types of Connectors for Connecting In-vehicle LED Lamp Modules to Boards

Panasonic Corporation announced today that it has developed two types of connectors for connecting in-vehicle LED lamp modules to control boards. These connectors allow for greater freedom and refinement in designing in-vehicle LED lighting. One of these is a "Board to FPC (Flexible printed circuit) Connector", the first of its kind in the industry*1 that is suitable

for cable connection to daytime running lights (DRLs), which are kept switched on during the daytime, and in rear lamps. The other is a "Board to Wire Connector", the lowest-profile connector in the industry*2 that is suitable for LED headlamp modules.

These new products have the following features:

This connector has a metal terminal connection structure that eliminates the need for FPC contacts for the first time in the industry*1, realizing direct connection between the LED-chip-mounted FPC and the control power board. It requires no relay harness, allowing the use of fewer components and fewer man-hours.

The connector's double-clip structure (clip metal contact structure) ensures its resistance to vibration and temperatures up to 125□, both extremely desirable properties for headlamps.

The connector's inertial lock structure prevents incomplete engagement, thereby offering improved workability.

This connector has an in-house-developed terminal shape that gives the connector a height of only 3.4 mm, the lowest profile of any connector in the industry*2. This low profile connector exerts a minimal effect on the lighting angle of the LED, enabling smaller and low profile LED lamp modules to be easily manufactured.

The connector's unique LED headlamp terminal structure gives it vital vibration resistance as well as heat resistance up to 125□.

The connector is equipped with a lock failure prevention guard that eliminates any failure in locking action, offering improved workability.
*1:On May 27, 2016, it was developed as a two-piece type board to FPC connector (according to research by Panasonic).
*2:On May 27, 2016, it was developed as a connector for in-vehicle LED lamp modules (according to research by Panasonic).
Remarks:
The products will be exhibited at the JPCA Show 2016 held at Tokyo Big Sight from June 1 to 3 this year..

Amphenol Industrial's Max-M12 Expansion

The Amphenol Industrial Products Group has enhanced its Max M12 product line to include board level connectors that mate to a PCB board with straight or right angle solder pins. These new connectors are ideal for high speed data transmission devices found in harsh environments.

The field installable and repairable Max M12 offers discrete connections that seal in harsh environments without requiring overmolds. The Max M12 family of connectors is based on IEC 61076-2-101 and SAE J2839. They are backward compatible and can be mated with any standard M12 connector with the same indexing.

This enhanced Max M12 PCB header mates to an in-line that can withstand connector-to-cable retention forces of 444 N and contact retention forces to 110 N. The in-line mate is housed in an HDM 12 EX impact resistant metal or plastic shell and both are available as 90° right angle or straight versions. The metal version is required for shielding. Both the 4- and 5-pin configurations are available with A, B, D and P polarity codes. Additional pin counts and codes are available upon request.

Hi-Rel industries shift to jackscrew fixings for ultimate connection security

Robotics, Satellites & Motor Sport applications all benefit from Harwin's Datamate J-Tek in high shock and vibration environments

Harwin has announced that several industries – satellites, robotics, motor sport – are now preferring to specify the company's 2mm pitch Datamate family of high reliability connectors with jackscrews, rather than latches or other fixing mechanisms, to ensure secure connection. As well as guaranteeing connector retention and signal integrity, the J-Tek jackscrew fixing is also being used to connect PCBs together in innovative configurations where space is at a premium.

Added security
Comments Scott Flower, Harwin's Global Product Manager for High Reliability Connectors: "As electronics becomes pervasive in harsh environments where high levels of shock and vibration are experienced, customers are demanding fixing solutions that provide the highest confidence levels. Autosport teams, for example, that used to use plastic latches are now moving over to jackscrews for added security. Robotics is another example where repeated mating can lead to the latch wearing, so jackscrews are now commonly preferred."

Harsh conditions
Satellites, especially miniature CubeSats, are relying on jackscrews not only to ensure that the connection survives harsh operation conditions, but also to save space. Flower: "One Datamate customer is using the jackscews to connect four boards in a box section. The boards then become self-supporting and the use of space – always a concern in satellite design – is maximised."

Harwin recommends that users torque Datamate jackscrews to 21 +/- 2 cN/m. This ensures that devices meet EIA specifications for vibration severity. Jackscrews are available with all Harwin's Datamate and Mix-Tek (mixed signal, power and coax) connectors.

Find more information on Datamate and the Datamate J-Tek range, or download the Datamate Jackscrew guide

ON Semiconductor Expands Optical Image Stabilization Portfolio, Bringing Superior Picture Quality to Built-In Camera Applications

ON Semiconductor (Nasdaq: ON),driving energy efficiency innovations, introduces its next generation Optical Image Stabilization (OIS) / Auto Focus (AF) driver, LC898123AXD,to its portfolio, offering a premier digital still camera and video experience for smart phones, tablets, notebooks, and wearables, by using advanced auto-focus, and optical image stabilization technologies to overcome the performance limitations of traditional camera modules.

The LC898123AXD OIS / AF driver integrates a DSP core with multiple analog peripherals for image stabilization, auto-focus control, and H-bridge and constant-current drivers. The addition of on-chip Flash memory provides storage for the DSP program and calibration parameters, thus saving 90% of the overhead time needed to load from conventional memory on startup. This highly integrated solution enables faster implementation of OIS and AF functionality into camera modules while remaining compatible with a wide array of image sensors. Furthermore, the high level of functional integration supports the need for very thin camera modules.

"There is growing demand for enhanced image clarity and quality in the latest smartphone models, as on-the-go consumers expect to derive better and better

user experiences regardless of device size," said Tomofumi Watanabe, Business Unit Leader of the Power Solutions Products in Intelligent Power Solution Division at ON Semiconductor. "The LC898123AXD enables camera module designers to meet these ever demanding requirements".

The LC898123 has best-in-class current consumption, enabling improved battery lifetime. The DSP performance and flexibility allows support for various VCM actuators. The high-performance 32-bit DSP optimized for OIS/AF signal processing covers many functions, such as servo control, gyro data filtering, and host command interface. In addition, the LC898123 offers "High Level Command" function to standardize commands from the main CPU to the camera module, enabling phone developers to use standardized commands for multiple camera modules/actuators without changing CPU software.

Reference designs dedicated to Camera Module Integrators are available, accelerating the OIS/AF evaluation as well as reduce the development workload.

Packaging and Pricing
The LC898123AXD is offered in a Pb-free WLCSP-35 package and is priced at $ 2.18 per unit in 4,000 unit quantities.

Infineon and GoerTek optical sensor solutions deliver precise, ultra-low power heart rate monitoring for smart devices

Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) and GoerTek Inc. (SHE: 002241) launched two high-resolution, highly integrated optical sensors. The optical chips deliver the precise measurement, small size and ultra-low power consumption demanded by ambient light sensing, proximity detection, heart rate and pulse oximetry monitoring applications in smart devices. The sensor solutions offer best-in-class performance for headphones, fitness bands, smart watches and phones. They are integrating three LED outputs, a photodetector, a low-noise analog front-end, a digital interface and a state machine into a single die. For best application results the bare die is either packaged with an infrared or a green LED or can drive up to three external LEDs.

The sensors offer a fully integrated solution for optical heart rate measurement featuring an I²C interface for a programmable sample rate of up to 256 per second. This allows a significantly better signal-to-noise ratio (SNR) than discrete alternatives. Additionally, monitoring algorithms can filter out motion artifacts and deliver precise heart rate and pulse oximetry measurements during exercise. High optical sensor resolution enables accurate measurement across the widest possible variety of skin types, while high optical sensitivity reduces photo diode area and drives down LED power consumption with a typical 300 µA LED current on fair skin. A standby current of just 0.3 µA further reduces power consumption.

Availability

Infineon and GoerTek sensor solutions are available either as bare die or as packaged products with application algorithm fromInfineon's long-term partnerGoerTek. Packages measure just 3.94 mm x 2.36 mm x 1.35 mm. Packaged samples are available now, with volume production targeted in August 2016. In addition to the bare die chips from Infineon, GoerTek is offering starter kits and demonstration boards for designers looking to rapidly evaluate and test the technology for use in their smart applications.

Cadence Next-Generation Virtuoso Platform Deployed by STMicroelectronics for SmartPower Technologies

Cadence Design Systems, Inc. (NASDAQ: CDNS) today announced that STMicroelectronics, a global semiconductor leader serving customers across the spectrum of electronics applications, has qualified and actively deployed the next-generation Cadence® Virtuoso® platform for its SmartPower technologies. The latest Virtuoso platform successfully enabled ST design engineers to improve custom routing quality and performance and significantly reduce block-planning and pin-optimization time using special pin groups and guide constraints.

In addition to its successes in such areas as sensors, microcontrollers and applications for the Internet of Things (IoT), ST is a worldwide leader in BCD (Bipolar, CMOS, DMOS) Smart Power technologies, utilized to develop ICs for automotive, power management, industrial, consumer and healthcare applications. To address the myriad of complex challenges that come with the development of these types of applications, ST turned to the next-generation Virtuoso platform to improve layout design automation without compromising the highest level of quality and reliability. Furthermore, the mixed-signal design interoperability between the Virtuoso platform and the Cadence InnovusÔ Implementation System offers best-in-class floorplanning, pin-optimization and implementation flows that led to a reduction in turnaround time.

In addition to qualifying the next-generation Virtuoso platform for its SmartPower technologies, the ST SmartPower Technology R&D (TR&D) team has also updated its design kits to support the latest Virtuoso platform for production use. This platform also includes the Virtuoso Layout Suite for Electrically Aware Design.

"We have been longtime users of the Virtuoso platform and have a very large user community that trusts the platform to drive the delivery of dozens of production tapeouts each year," said Pier Luigi Rolandi, director of TR&D Smart Power Design Enablement at STMicroelectronics. "Layout design automation needs to be done in a

way that is very seamless to the end user while maintaining highest level of quality, and the next-generation Virtuoso platform does just that. The new platform also enables us to improve designer productivity and effectiveness to ensure that our teams can meet aggressive time-to-market goals."
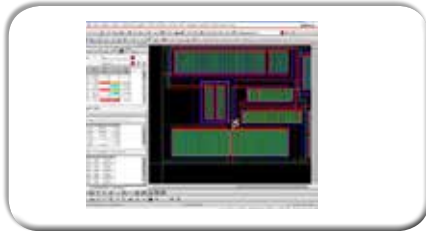
Microchip Announces Graphical User Interface Composer Tool for MPLAB® Harmony

MPLAB Harmony Graphics Composer Allows Engineers to Easily Develop and Design Professional-Looking Graphical User Interfaces

Microchip Technology Inc. (NASDAQ: MCHP), a leading provider of microcontroller, mixed-signal, analog and Flash-IP solutions, today announced the MPLAB® Harmony Graphics Composer (MHGC), a modern and flexible graphical user interface (GUI) composer tool. MHGC is a free development tool for developing GUIs for all PIC32 microcontrollers through Microchip's Harmony Configurator and MPLAB X Integrated Development Environment (IDE). The software allows anyone to create branded content using the Harmony Graphics Library, in conjunction with their custom assets, to create GUIs in

a What-You-See-is-What-You-Get (WYSIWYG) design model, without complex and cumbersome coding. View a short, informative video demonstration of MHGC:.

MPLAB Harmony Graphics Composer takes care of all configuration requirements as well as generating all source code needed for a professional-looking GUI. Users can easily import images and fonts and add them into projects via MHGC's intuitive, user-friendly interface. The tool gives the user the ability to add, delete, move, scale and configure objects within the application. Objects can be interactive, including sliders, dials and buttons without the developer needing to understand graphics code.

"The response from customers has been very positive," continued Hoefle. "We have found the feedback invaluable and created a platform that we believe our customers will find simple, professional and intuitive."

MPLAB Harmony Graphics Composer is integrated with Microchip's MPLAB X and utilizes the graphics libraries in MPLAB Harmony. The software is available now for download by visiting: http://www.microchip.com/harmony

STM32F7 Microcontrollers from STMicroelectronics Expand Ecosystem with New Development Boards to Accelerate Embedded Design

STMicroelectronics has released entry-level, mid-range, and high-end development boards for the latest members of its STM32F7 microcontroller series , which are now entering volume production with up to 2Mbyte of on-chip Flash memory and peripherals that help create rich user interfaces. STM32F7 Microcontrollers from STMicroelectronics Expand Ecosystem with New Development Boards to Accelerate Embedded Design

Providing timely support for design starts, the new development tools include a low-cost STM32 Nucleo-144 board featuring the STM32F767 variant. Also available is a Discovery Kit supporting the STM32F769, which has TFT-LCD and MIPI®-DSI support. In addition, there are highly featured evaluation boards for the STM32F769 and the STM32F779, which has a cryptographic accelerator for security-conscious applications. The evaluation boards and Discovery Kit also come with a 4-inch QWVGA 800×400 MIPI-DSI display featuring a capacitive touchscreen.

Developers using the STM32F7 hardware platforms can take advantage of extensive software support that comprises the STM32CubeMX initialization tool and STM32CubeF7 embedded software package including Hardware Abstraction Layer (HAL)

and middleware components like the FreeRTOS real-time operating system, USB library, and lwIP (lightweight IP) open-source TCP/IP stack.

The STM32F7 ecosystem enables developers to create microcontroller applications with sophisticated user interfaces that formerly required the resources of a Microprocessor Unit (MPU). The MCU devices, which are based on the 216MHz/462DMIPS/1082 CoreMark®ARM®Cortex®-M7 core with double-precision floating-point unit and DSP instructions, combine enhanced graphics capabilities with extensive connectivity through:

ST's Chrom-ART Accelerator™ and a hardware JPEG accelerator for high-speed graphics rendering;

Support for TouchGFX, which allows high-performance graphics and touch at minimal CPU loading;

Support for Embedded Wizard, which allows high-performance graphics and comes with a PC-based utility that helps build GUIs using graphical tools and drag & drop actions;

STemWin professional graphics library and development tools;

Support for USB2.0 with OTG;

CAN2.0 port and Ethernet with IEEE 1588 time-stamping ideal for industrial applications;

HDMI Consumer-Electronics Control (CEC), a camera interface, and dual-mode Quad-SPI interface to high-speed off-chip memory;

Multiple 16- and 32-bit timers and 12-bit 2MSPS ADCs;

Audio features including 12-bit DACs, I2S (Inter-IC Sound) serial interface with Phase-Locked Loop

(PLL) support, digital filters for a sigma-delta modulator, and an S/PDIF receiver.

The STM32F769I-EVAL and STM32F779I-EVAL evaluation boards are priced at $360, while the $79 Discovery Kit (STM32F769I-DISCO) and the $23 STM32 Nucleo-144 board (NUCLEO-F767ZI) enable extremely low-cost design starts. All are available immediately, and can be ordered directly from ST or distributors.

Cadence Expands OrCAD Solution to Address Flex and Rigid-Flex Design Challenges for IoT, Wearables and Mobile Devices

at CDNLive EMEA, Cadence Design Systems, Inc. (NASDAQ: CDNS) announced the OrCAD 17.2-2016 release with new capabilities for OrCAD® Capture, PSpice® Designer and PCB Designer that address challenges with flex and rigid-flex design as well as mixed-signal simulation complexities in IoT, wearables and wireless mobile devices.This latest release reduces PCB development time by addressing the need to design reliable circuits for smaller, more compact devices.

This OrCAD portfolio includes technology enabled for integrated rigid-flex planning, design and real-

time visualization, as well as built-in translators that enable direct design imports from select EDA vendors. PSpice Designer now supports system-level simulation using C/C++/SystemC and VerilogA, via the new PSpice compact model interface. This enables hardware/software virtual prototyping so that electrical engineers can design and simulate intelligent IoT devices. OrCAD is the only fully scalable PCB design solution available in the market that seamlessly transitions from mainstream to enterprise PCB solution with the Allegro® environment. For more information on the latest OrCAD solution, visit: www.orcad.com/orcad-172-2016-release.

To enable a faster and more efficient flex and rigid-flex design creation critical to IoT, wearables and wireless devices, the OrCAD portfolio uses a new multi-stack-up database capability and extensive in-design inter-layer checks, which helps users avoid errors introduced through manual checking. The OrCAD portfolio also features enhancements targeted towards improving PCB editors' productivity and ease-of-use in padstack editing, constraint management, shape editing and in-design DRCs. To address efficiency needs, the portfolio includes an advanced design differencing engine that enables design review with global teams using state of art visuals. Finally, to give designers more control over their design component annotation process, advanced annotation and auto-referencing capabilities are now available.

"This latest OrCAD release has given us confidence in getting a functional PCB without CAD errors the first time. Prior to this, we were always cautious that our PCB packages would introduce unforeseen errors and we would have to factor one spin of the board that was barely functional," said David Edwards, founder and CEO of Abicom. "Cadence has built tools that are enabling us to develop better designs faster, while giving us a better understanding of expected performance. This advancement has saved us upwards of £3-8K per new board design."

"OrCAD continues to be the clear choice for new and existing companies designing IoT, wearable and mobile products," said Dirk Müller, CEO, FlowCAD EDA-Software Vertriebs GmbH. "The new flex and rigid-flex capabilities allow designers to create faster and smarter products in a timely and cost-effective manner."

"Our customers are demanding solutions that address their broader system-design challenges," said Steve Durrill, senior product engineering group director, SPB Solutions at Cadence. "The latest OrCAD release provides upfront virtual prototyping support in PSpice, support for high-speed interfaces and a comprehensive implementation solution for rigid/flex designs. We are confident this latest release of the OrCAD solution provides the time to market savings our customers require."

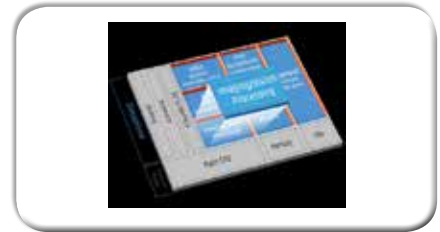## Uurmi Fog Removal Software Now Available on Cadence Tensilica Vision DSPs

Cadence Design Systems, Inc. (NASDAQ: CDNS) and Uurmi Systems today announced that Uurmi's fog removal software targeted for automotive and camera markets is now available on the Cadence® Tensilica® Vision digital signal processor (DSP). By porting their fog removal software to the Tensilica Vision DSP, Uurmi achieved up to 5X higher performance, with 15X less power consumption.

Uurmi's fog removal software eliminates fog present in the photo and applies correction to improve the image. It uses a spatial diffusion filtering-based approach with local contrast enhancement to remove fog during the image post-processing stage. It also offers fog correction for images captured from un-calibrated camera systems. Uurmi's software provides fog correction with scene sharpness preservation and is capable of fog/non-fog region separation. For more information on Uurmi's fog removal software, visithttp://uurmi.com/multi-sensor-fusion-image-system.html.

The Tensilica family of imaging/vision DSPs was designed for the complex algorithms in imaging, video and computer vision applications, including innovative multi-frame image capture, video pre- and post-processing, object and face recognition, low-light enhancement and many other complex tasks. For more information, visitwww.cadence.com/news/Uurmi.

"By porting our fog removal software to the Tensilica Vision DSP, we achieved dramatic improvements in power," said Dr. Swarup Medasani, CTO at Uurmi Systems. "With a quick turnaround time, we achieved significant performance gains with low power consumption, which are critical differentiators in the ever-growing mobile, camera and security applications market."

Infineon and GoerTek optical sensor solutions deliver precise, ultra-low power heart rate monitoring for smart devices

Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY) and GoerTek Inc. (SHE: 002241) launched two high-resolution, highly integrated optical sensors. The optical chips deliver the precise measurement, small size and ultra-low power consumption demanded by ambient light sensing, proximity detection, heart rate and pulse oximetry monitoring applications in smart

devices. The sensor solutions offer best-in-class performance for headphones, fitness bands, smart watches and phones. They are integrating three LED outputs, a photodetector, a low-noise analog front-end, a digital interface and a state machine into a single die. For best application results the bare die is either packaged with an infrared or a green LED or can drive up to three external LEDs.

The sensors offer a fully integrated solution for optical heart rate measurement featuring an I²C interface for a programmable sample rate of up to 256 per second. This allows a significantly better signal-to-noise ratio (SNR) than discrete alternatives. Additionally, monitoring algorithms can filter out motion artifacts and deliver precise heart rate and pulse oximetry measurements during exercise. High optical sensor resolution enables accurate measurement across the widest possible variety of skin types, while high optical sensitivity reduces photo diode area and drives down LED power consumption with a typical 300 µA LED current on fair skin. A standby current of just 0.3 µA further reduces power consumption.

Availability

Infineon and GoerTek sensor solutions are available either as bare die or as packaged products with application algorithm fromInfineon's long-term partnerGoerTek. Packages measure just 3.94 mm x 2.36 mm x 1.35 mm. Packaged samples are available now, with volume production targeted in August 2016. In addition to the bare die chips from Infineon, GoerTek is offering starter kits and demonstration boards for designers looking to rapidly evaluate and test the technology for use in their smart applications.

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ON Semiconductor Expands Low Power Wireless Solutions Portfolio with SIGFOX and ARM for Rapid IoT Deployment

ON Semiconductor (Nasdaq: ON), driving energy efficient innovations, has announced two major strategic developments to enable rapid deployment of Internet of Things (IoT) solutions.

Working in conjunction with SIGFOX, the world's leading provider of dedicated connectivity for the Internet of Things (IoT), ON Semiconductor has confirmed that its AX-SFEU system-on-chip (SoC) is now fully SIGFOX Ready™ certified for optimal two-way communication in Europe with certification underway for the US. Through the AX-SF SoC, plus its accompanying library and development system, IoT developers will be able to easily use SIGFOX's long range, two-way global IoT network – resulting in a low cost, low-power device-to-cloud connectivity solution that is highly optimized for environmental sensors, smart meters, patient monitors, security devices, streetlights and a broad spectrum of other industrial and consumer-oriented applications.

The AX-SF SoC draws under 10 milliamperes (mA) of current when receiving data and has a sensitivity of -129 decibel-milliwatt (dBm) at 600 bits/second (bps) with GFSK modulation. The reference design, which does not require an expensive front-end module, features a 23 dBm transmitter and has only a 220 mA current consumption, enabling designers to markedly extend communication range while maximizing battery life.

ON Semiconductor also announced that it is now an official ARM® mbed™ partner. The NCS36510 2.4 gigahertz (GHz) IEEE 802.15.4 compliant transceiver platform will include the mbed OS and Thread stack. Access to the ARM mbed ecosystem in combination with Thread will again prove highly beneficial for IoT developers, helping them to produce more agile, robust, cost-effective solutions with end-to-end security and lower power budgets that better address their application demands.

"ON Semiconductor was very early to recognize and respond to demands for transceivers that provide extremely low-power, wireless connectivity for the IoT," states Stuart Lodge, Executive Vice President of Global Sales and Partners at SIGFOX. "Our fast-growing operated network, currently in 18 countries including the US and registering over 7 million devices, requires a reliable supply of high performance, low-cost and extremely energy-efficient integrated circuits, and our collaboration with ON Semiconductor helps assure

those solutions will be available to our customers."

"We are committed to delivering a comprehensive portfolio of innovative low power wireless solutions to enable the rapid deployment of IoT devices and solutions. Our AX-SF ultra-low power sub GHz solution gives developers robust and reliable two-way connectivity to the SIGFOX global network," said Ryan Cameron, Vice President and General Manager of the industrial and timing division at ON Semiconductor. "Meanwhile for the LAN environment, our industry leading 802.15.4 platform based on the NCS36510 now provides users access to the ARM mbed ecosystem coupled with the benefits of Thread for security and interoperability. SIGFOX, in combination with Thread, also has great potential for use cases where multiple connectivity solutions can be mixed to create new user experiences.

To learn more about ON Semiconductor's expertise in IoT technology you can attend a series of presentations that company representatives will be giving at IoT World (10th – 12th May, Santa Clara Convention Center, Santa Clara, CA).

NXP Introduces New High Performance GaN RF Power Transistors for Cellular Base Stations

NXP Semiconductors N.V.(NASDAQ:NXPI), today announced an expansion to its portfolio of 48V Gallium Nitride (GaN) RF power transistors optimized for Doherty power amplifiers for use in current and next-generation cellular base stations. The four new transistors collectively cover cellular bands from 1805 to 3600 MHz, meeting the needs of wireless carriers for superior performance at higher frequencies.

With the wireless spectrum shortage, wireless carriers are exploring higher frequencies to accommodate the exponential annual increases in traffic. These networks require RF power transistors and amplifiers that deliver higher performance over wider signal bandwidths, as well as higher efficiency and ruggedness, higher output power and smaller footprints.

The four new NXP GaN transistors are specifically designed to meet these challenges. The transistors have high efficiency and gain, and are extremely rugged, with the ability to deliver their rated performance with an impedance mismatch (VSWR) greater than 10:1. These transistors, designed for use in Doherty power amplifiers, are optimized for seamless integration with digital predistortion linearization systems.

The new products introduced today are:

A2G22S251-01S: Ultra wideband symmetrical Doherty two device solution covering 1805 to 2170 MHz (365 MHz bandwidth). In a symmetric Doherty, it delivers an average RF output power of 71 W (450 W peak), gain of 16.5 dB, and drain efficiency of 46% in concurrent multiband operation at 8 dB back-off configured. The part is housed in a NI-400S-2S air-cavity ceramic package.

A2G26H281-04S: NXP's first in-package Doherty transistor covering 2496 to 2690 MHz, with average RF output power of 50 W (288 W peak), gain of 15.3 dB, and drain efficiency of 57% configured in a NI-780S-4L air-cavity ceramic package.

A2G35S160-01S and A2G35S200-01S: Two-transistor Doherty amplifier solution covering 3400 to 3600 MHz with 53 W average RF output power (331 W peak), gain of 13.8 dB, and drain efficiency of 46%. Each of these transistors is housed in a NI-400S-2S air-cavity ceramic package.

"Cellular customers are actively pursuing GaN technology especially in higher frequency bands. Given its leadership in the cellular base station market, NXP is committed to being a dominant source of top-quality GaN products," said Paul Hart, executive vice president and general manager of NXP's RF power business unit. "Our new transistors fully harness the inherent strengths of GaN enabling broad bandwidth, efficient and compact solutions."

Imec and Holst Centre Present Multi-Standard Low-Power Wide-Area Radio Chip

The world-leading nanoelectronics research centers imec and Holst Centre (set up by imec and TNO), presented a low-power wide-area (LPWA) multi-standard radio chip today at imec's annual technology forum in Brussels (ITF Brussels 2016). The new radio chip is a best-in-class product, which can operate with a lower level of power consumption than any other radio chip technology released to date for long range connectivity in sensor networks. The sub-GHz radio chip's technology can serve a multitude of protocols including IEEE 802.15.4g/k, W-MBUS, KNX-RF, as well as the popular LoRa and SIGFOX networks, and future cellular IoT for applications such as smart metering, smart home, smart city and critical infrastructure monitoring.

The radio chip operates in industrial, scientific, medical (ISM) and short-range devices (SRD) bands, covering a frequency range from 780MHz to 930MHz. The robust, low-power design combines a large link budget, with state-of-the-art interference rejection and lowest

bill of materials by minimizing external components as compared to of-the-shelf available chips. The radio is implemented as a complete System-on-Chip (SoC) including the RF front end, power management, an ARM processor,160kBytes of SRAM and peripherals like SPI, I2C and UART. It features a targeted sensitivity of -120dBm at 0.1% BER (1kbps) and ultra-low power consumption of 8mW (Rx) and 113mW (Tx) for 13.5dBm output power. The receiver supports a wide gain range to handle input signals from -120dBm to -15dBm, corresponding to a large dynamic range of 105dB. The PA features automatic ramp-up and ramp-down for ARIB spectral mask compliancy. Furthermore, the output power is controllable from <-40dBm up to 15dBm.

"With the foreseen release of the NB-IoT protocol in June 2016 by the 3GPP, it is clear that protocols such as NB-IoT, SigFox and LoRA are here to stay for the coming years," stated Kathleen Philips, program director perceptive systems at imec/Holst Centre. "Our novel sub-GHz radio chip can serve multiple of these protocols and is an ideal solution for long-range wireless connectivity for IoT applications."

Imec's Industrial Affiliation program on the Intuitive Internet-of-Things (IoT) focuses on developing the building blocks for the future. The program explores an intuitive IoT, with sensor systems that can detect and assist with the needs and wants

of people in an unobtrusive way, and can take into account their varied perspectives and surrounding environment. Along with low-power radio chips, imec also develops ultra-small, low-cost, intelligent, and ultra–low power sensors and heterogeneous sensor networks. Interested companies are invited to partner with imec on its varied research initiatives. Companies can also connect with imec to request access to imec's technological advances to further develop their projects through licensing programs with imec.

TI delivers the industry's first RF sampling 14-bit, 3-GSPS analog-to-digital converter

Texas Instruments (TI) (NASDAQ: TXN) introduced the highest level of radio-frequency (RF) sampling performance with the ADC32RF45, the industry's fastest 14-bit analog-to-digital converter (ADC). This dual-channel ADC enables direct RF signal conversion up to 4 GHz, giving engineers access to the highest dynamic range and input bandwidth. The first in a new data converter family in TI's RF sampling portfolio, the ADC32RF45 eliminates up to four intermediate-frequency downconversion stages

in multiband receivers, which simplifies system architecture and reduces board space up to 75 percent.

Experience the interactive Multimedia News Release here: http://www.multivu.com/players/English/7746252-texas-instruments-direct-rf-sampling/

Direct RF sampling meets engineers' requirements for higher integration, better noise performance, wider bandwidth and smaller footprints in radar, software-defined radio, aerospace and defense, test and measurement, wireless communication, and radio astronomy systems. For more information or to order the evaluation module (EVM) today, see www.ti.com/ADC32RF45-pr.

Key features and benefits

Support for RF inputs up to 4 GHz enables direct RF signal conversion in the first, second and third Nyquist zones (including all L- and S-band frequency ranges). This reduces filter complexity, saves board space and decreases component count.

The ADC32RF45 detects even the weakest signals with industry-leading noise-spectral density of -155 dBFS/Hz, 5 dB better than competitive devices. It offers industry-leading signal-to-noise ratio of 58.5 dB at a 1.8-GHz input frequency.

Fastest 14-bit ADC with a 3-GSPS maximum sample rate delivers an instantaneous 1.5-GHz-per-channel bandwidth, enabling engineers to implement wideband in-phase and quadrature-component receivers beyond 2.5 GHz.

The multiband digital downconverter extracts one or two sub-bands per channel, a dramatic digital interface data throughput reduction by up to 92 percent, saving system size, power and processing resources.

Resources to speed design

Available now through the TI store, the ADC32RF45EVM is priced at US$2,499 and the TSW14J56EVM data-capture card is available for US$1,249. Additional support includes TI Designs reference designs and application notes.

Complete high-performance signal chain

To speed development and maximize performance, engineers can design a complete analog signal chain today using the ADC32RF45 with TI's LMH3404 7-GHz dual-channel fully differential amplifier, which supports bandwidths from DC to 1.5 GHz; the LMX2592 9.8-GHz wideband frequency synthesizer; and the LMK04828 JESD204B-compliant clock-jitter cleaner. In addition, the 66AK2L06 processor offers a system-optimized alternative to field-programmable gate arrays (FPGAs). Learn more in the blog post, "How to complete your RF sampling solution."

Availability and pricing

In addition to the ADC32RF45EVM available today, the ADC32RF45 will be in volume production in the third quarter of 2016 in a 72-pin, 10-mm-by-10-mm quad flat no-lead (QFN) package for US$2,495 in 100-unit quantities.

RF sampling resources

Read the 10-part RF sampling blog series.

Watch RF sampling videos at the High Speed Signal Chain University.

Experience the ADC32RF45 at International Microwave Symposium 2016, booth 419.

TI is a global semiconductor design and manufacturing company that develops analog integrated circuits and embedded processors. Learn more at www.ti.com.

SOURCE Texas Instruments.

NXP Partners with Wayv to Unveil the World's First Handheld Portable, Battery-Operated RF Cooking Appliance

NXP Semiconductors (NASDAQ:NXPI), and Wayv, today unveiled the world's first battery operated, handheld portable cooking appliance, the Wayv Adventurer. Designed to be compact, rugged, and light-weight, the Wayv Adventurer is intended to give people the flexibility to efficiently and conveniently heat food anytime and anywhere. It can serve a number of on-the-go cooking needs including heating nutritious meals quickly and easily, at the workplace, to support people affected by disasters or personnel at military bases and in the field. The Adventurer is ideal for preparing meals outdoors during leisure activities such as camping, hiking, or fishing.

The new appliance demonstrates

NXP's leadership in driving compelling new product innovations into the smart cooking market through solid state RF technology. NXP RF technology offers maximum power transfer with controllable energy to the food with less wasted heat. Making it better for the planet. "NXP's leading RF power output, high efficiency, and industry leading expertise has provided the platform to enable us to develop the Wayv Adventurer," said Paul Atherton, CEO and Founder at Wayv. "Delivering innovative RF cooking appliances that provide more convenient and healthier food and beverage heating options to consumers are benefits we hope to bring to the marketplace. NXP technologies helps us deliver on those fronts. We're proud to partner with NXP on driving this new product into the market."

NXP's RF module solution, which delivers 250W of RF power at high efficiency, combined with Wayv's RF antenna, helps deliver excellent cavity efficiency for effective power transfer to the food. Since battery operated appliances currently have limited electrical power, the best possible efficiency is essential. NXP's RF module solution delivers high efficiency power combined with Wayv's high efficiency antenna solution which allows for multiple heating cycles before recharge. The technology platform includes NXP's MKW40Z Kinetis microcontroller (MCU) with a 2.4 GHz signal generator, a MMA25312 pre-driver, MHT1008 driver and MHT1004 final stage amplifier into a single, integrated closed-loop module.

"The new Wayv Adventurer takes on-the-go smart cooking experiences to a new level," said Dan Viza, director of product marketing for RF cooking at NXP. "We're excited to work with Wayv and unveil this new innovation into the market."

Demonstration

The Wayv Adventurer was demonstrated this week at NXP FTF 2016. For more information visit nxp.com/Wayv..

Analog Devices' Silicon Switch Reduces Size and Power Consumption in Cellular Radio RF Front Ends

Analog Devices, Inc. (ADI) today introduced a high power (44 watts peak) single-pole, double-throw (SPDT) silicon switch that enables designers to reduce hardware size and bias power consumption in cellular radio systems. As the next generation of communications infrastructure trends toward higher data capacity, cellular radio front ends must scale down in size and provide faster speeds to meet the demands of increased data usage. ADI's ADRF5130 switch meets these requirements through a high level of integration that eliminates the need for external components. The switch also reduces power consumption to more efficient levels by operating on a single low-voltage supply with extremely low current

consumption compared to existing pin-diode-based solutions. The ADRF5130 is manufactured using silicon technology, and is housed in a small 4 mm × 4 mm LFCSP SMT package.

View product page, download data sheet, order samples and evaluation boards: http://www/analog.com/ADRF5130

Learn about Analog Devices RF switches portfolio:http://www.analog.com/en/products/rf-microwave/rf-switches.html

Connect with engineers and ADI product experts on EngineerZone®, an online technical support community: https://ez.analog.com/community/rf

The ADRF5130 is specified at 0.7-GHz to 3.5-GHz frequency band with typical 0.6-dB insertion-loss, high isolation of 50 dB, excellent linearity of +68 dBm and peak power handling of 44 watts during continuous operation mode. The device features robust 2000-V electro-static-discharge (ESD) protection on all device pins. It also incorporates a fast CMOS-compatible control interface with switching time less than 1 us. Additionally, a symmetrical circuit architecture allows the RF inputs to be used interchangeably in high power applications.

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[i] See datasheet for suggested application circuit.
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